3D Stacked Buck Converter with $SrTiO_3$ (STO) Capacitors on Silicon Interposer

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Outline

Introduction

- Fine-grained voltage engineering
- 3D stacked DC-DC (buck) converter

Silicon Interposer

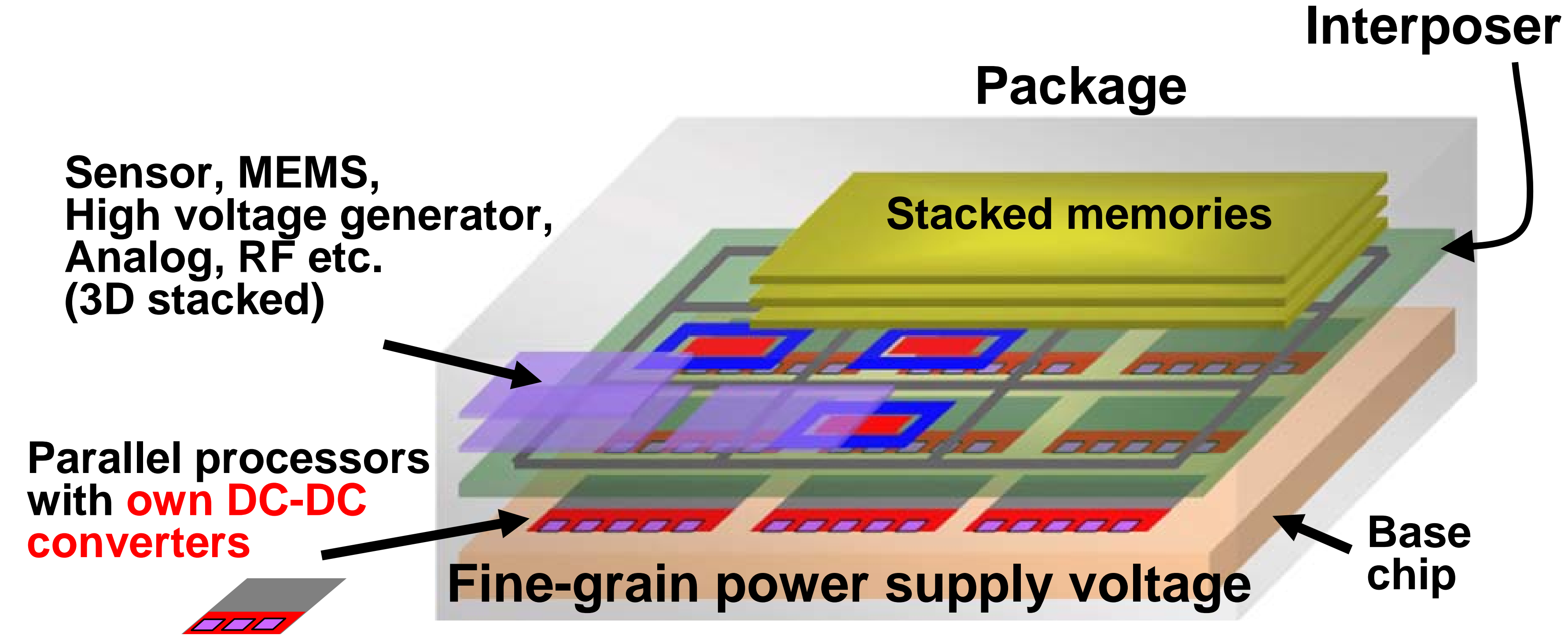
- 1.5μF/cm^2 $SrTiO_3$ (STO) capacitor
- 15μm thick inductor

Measured Efficiency of Buck Converter

Summary

Power Supply for High-Performance 3D-LSIs

- Heterogeneous integration ⇒ Various power supplies
- Low-power and high-performance
  ⇒ Fine-grained voltage engineering

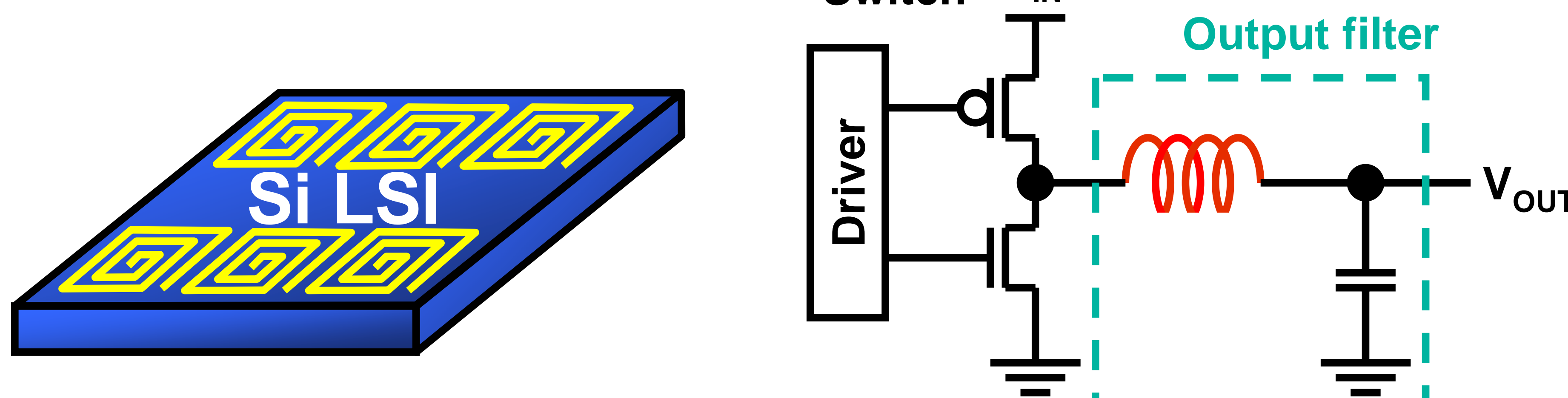


On-chip DC-DC (buck) converters are essential for 3D LSIs.

On-Chip Buck Converters

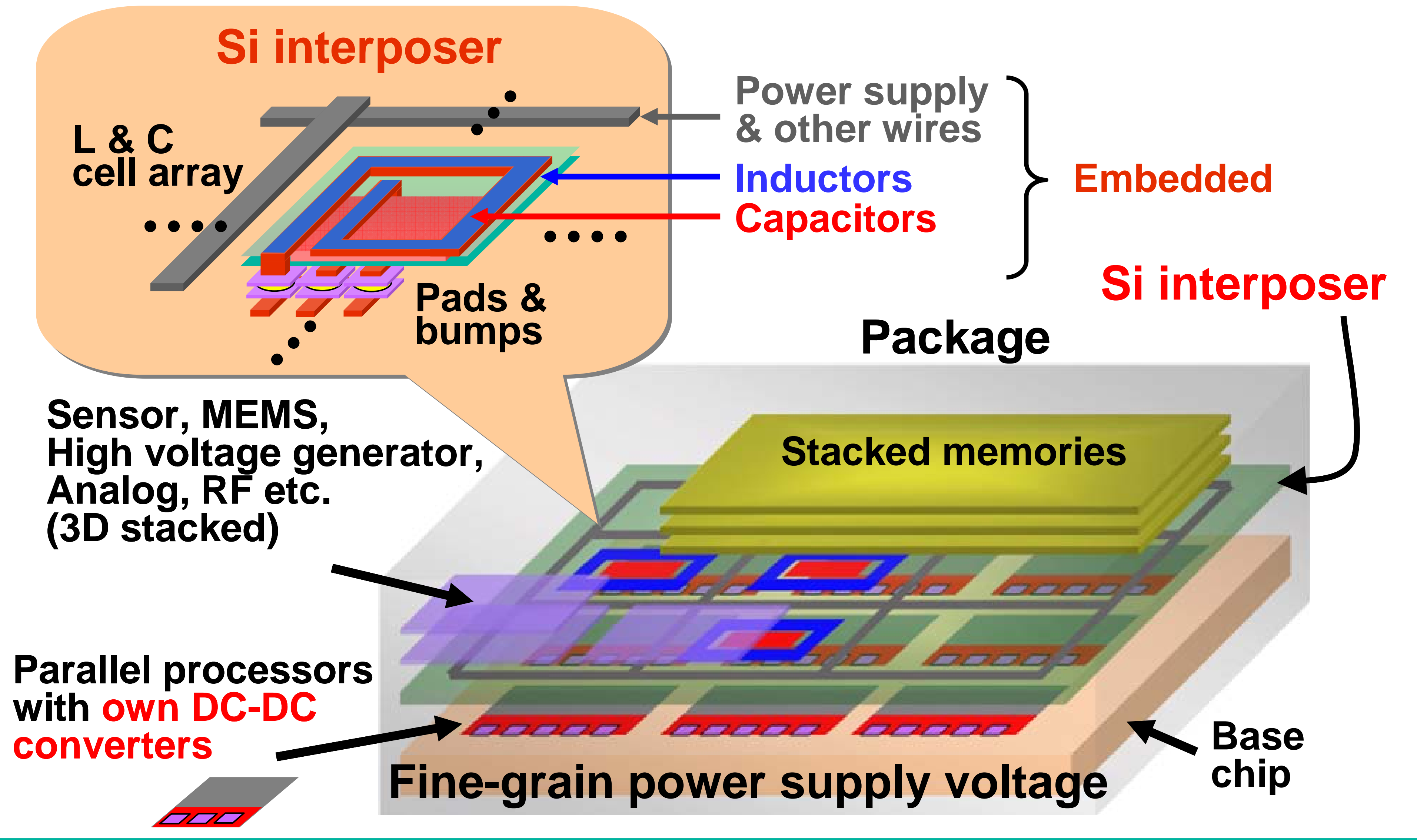
Disadvantages of on-chip inductors

- Smaller inductance < 10 nH
- Area penalty
- Parasitic resistance due to thin conductors



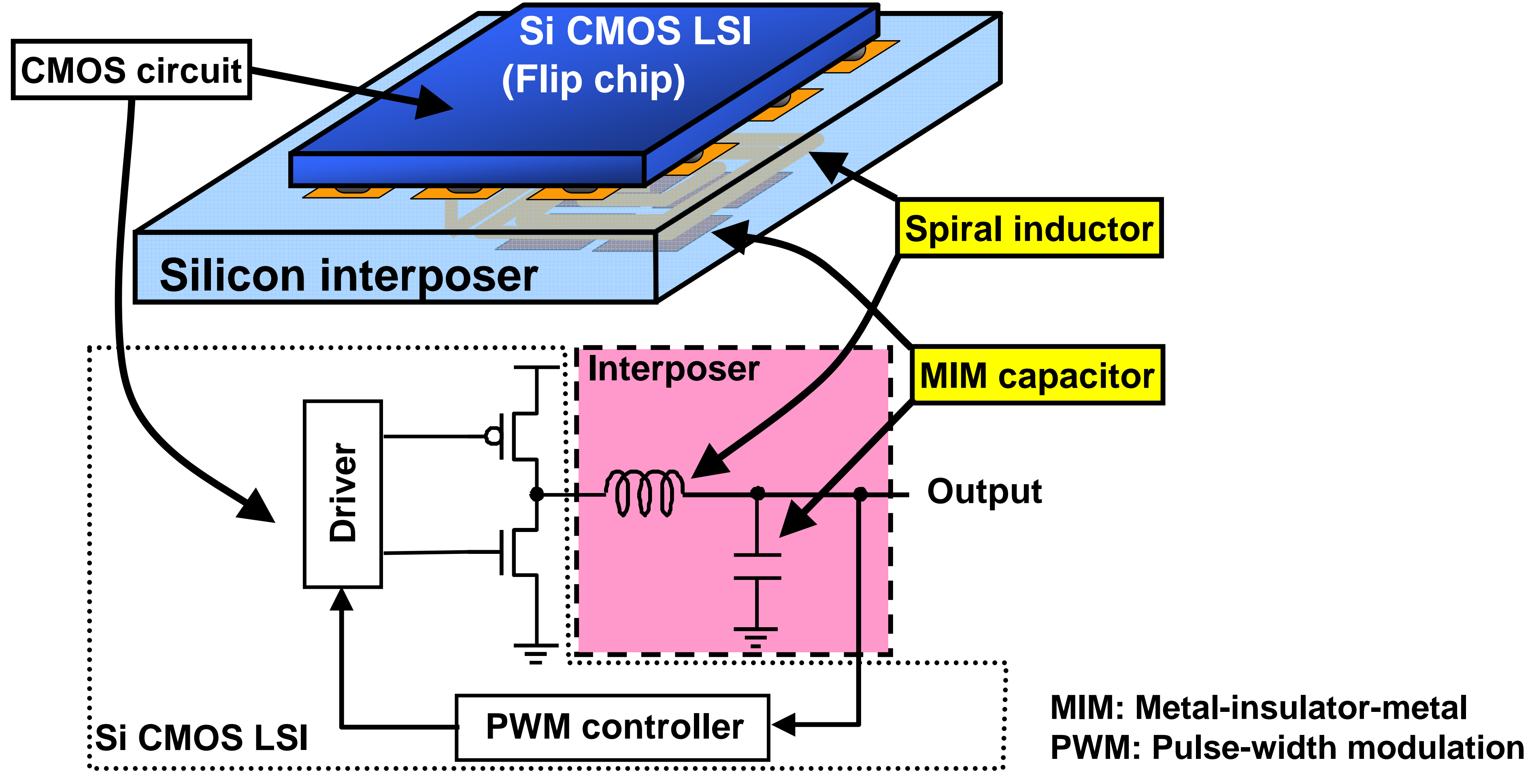
Inductors should be thick and separated from a Si chip.

Concept of 3D Stacked Distributed Power Supply



Output LC filters is embedded into a Si interposer.

Proposed 3D Stacked Buck Converter



MIM: Metal-insulator-metal
PWM: Pulse-width modulation

Area penalty and parasitic resistance will be small.

K. Takemura, K. Ishida, Y. Ishii, K. Maeda, M. Takamiya, T. Sakurai, and K. Baba, "Si Interposers with Thick Spiral Inductors for 3D Stacked Buck Converters," ICEP, TA4-1, Apr. 2011.
K. Ishida, K. Takemura, K. Baba, M. Takamiya, and T. Sakurai, "3D Stacked Buck Converter with 15um Thick Spiral Inductor on Silicon Interposer for Fine-Grain Power-Supply Voltage Control in SiP's," IEEE International 3D System Integration Conference, pp. 1-4, Nov. 2010.

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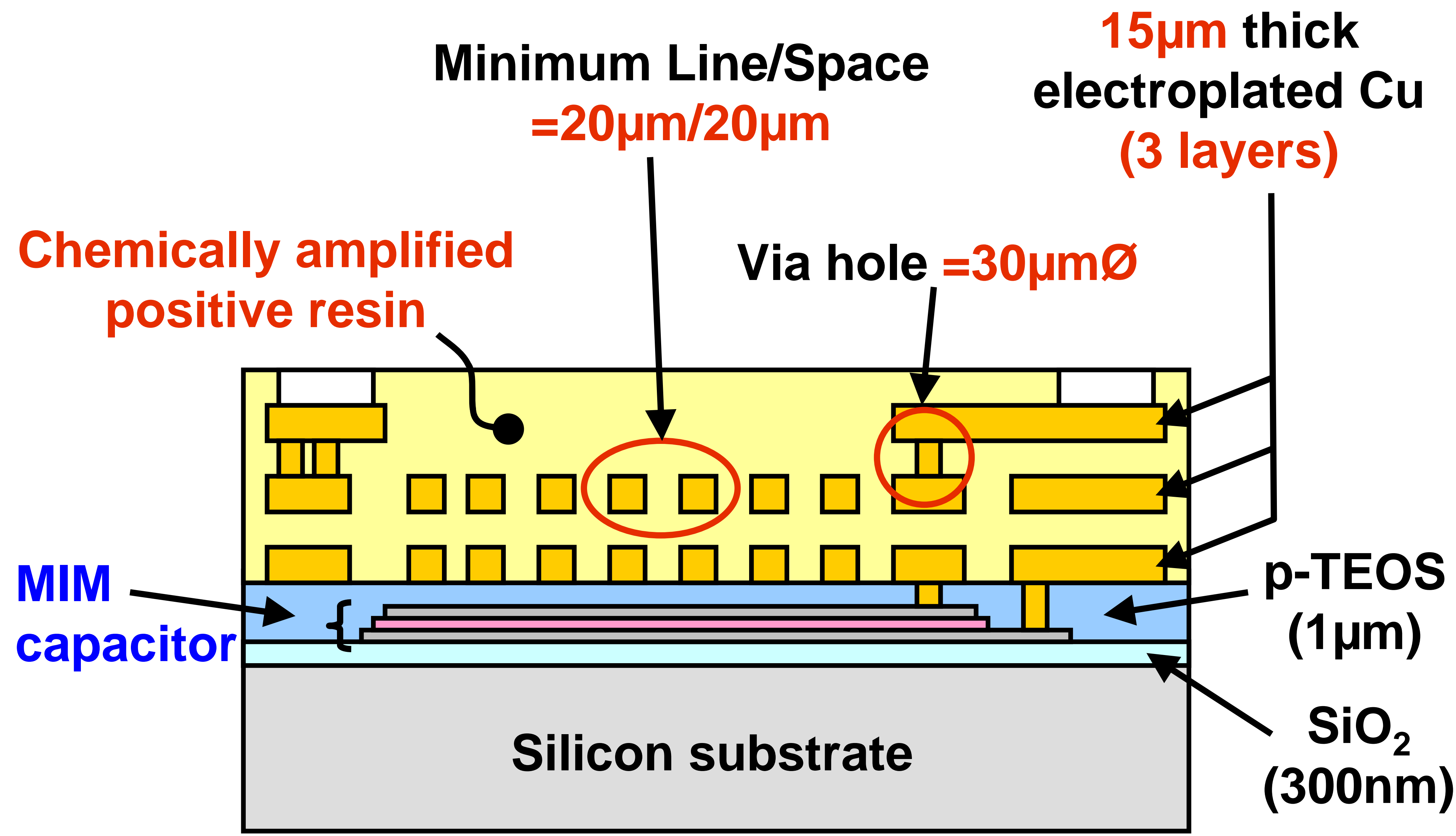
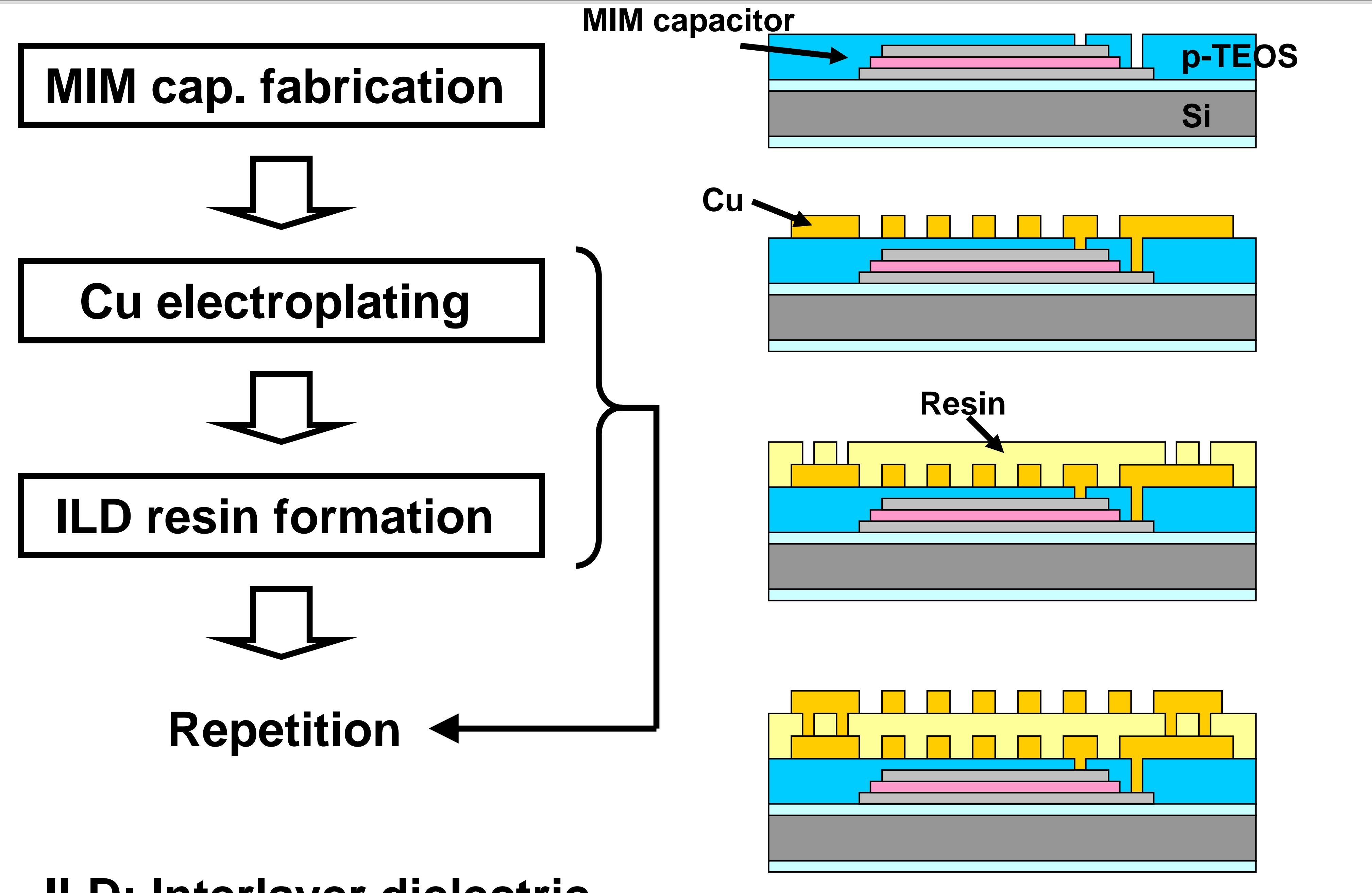


Fabrication Process of Silicon Interposer



ILD: Interlayer dielectric

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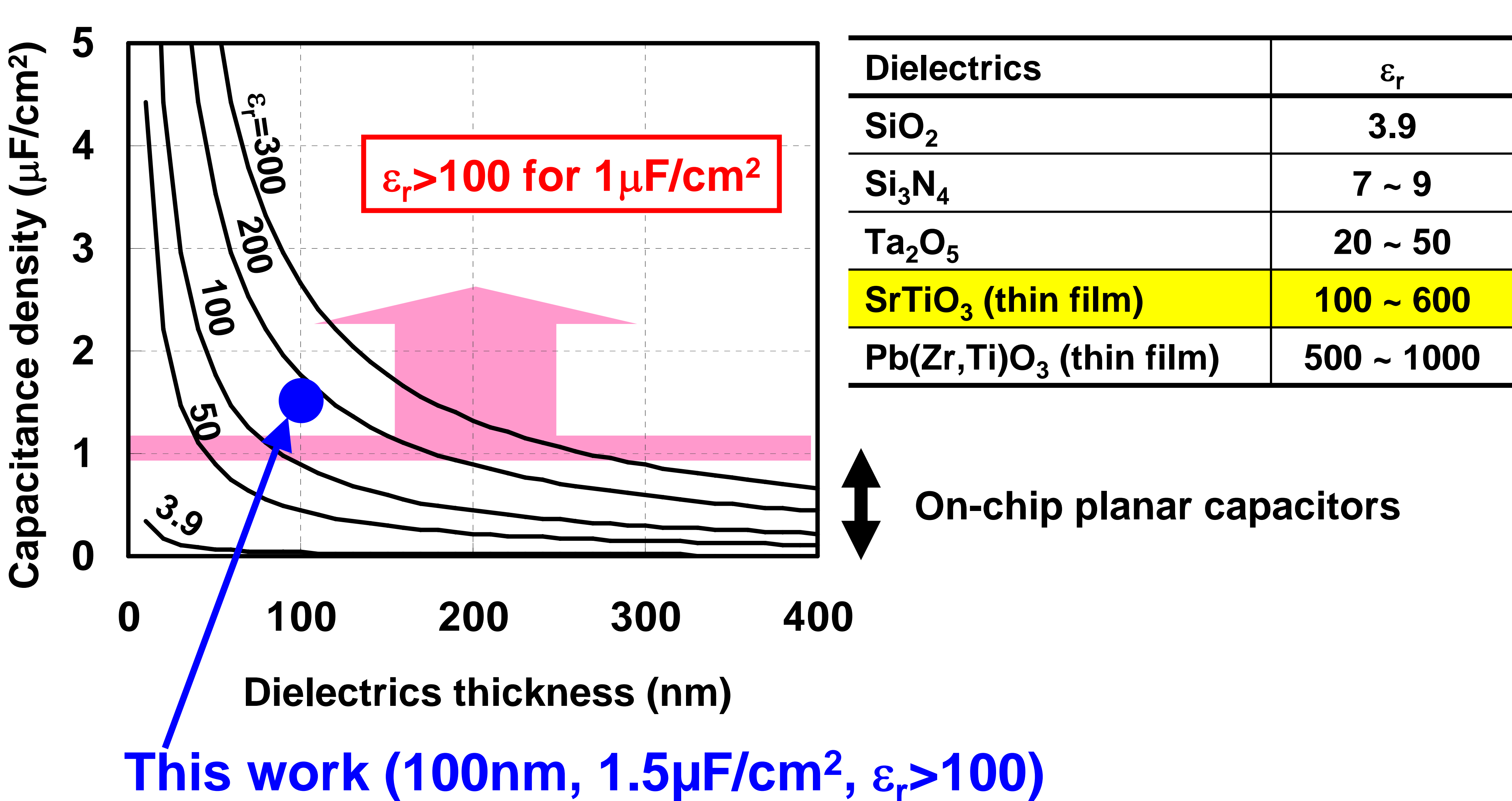
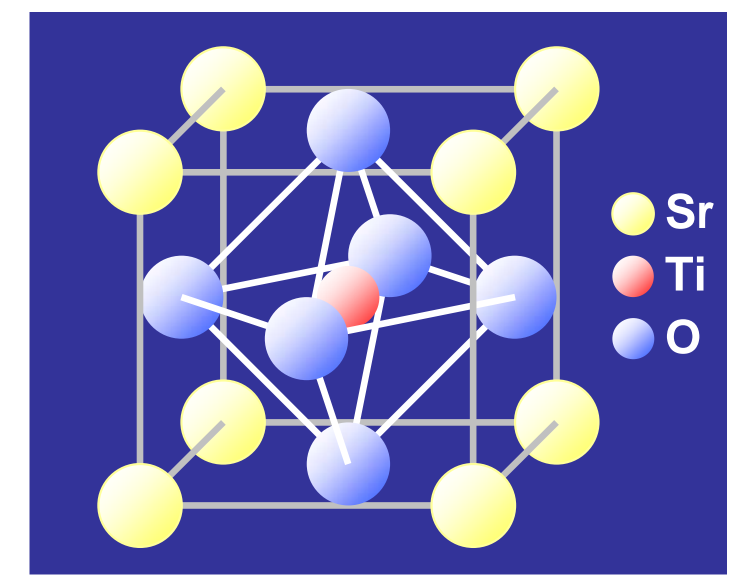
Capacitor Dielectrics

When the target capacitance density is higher than 1μF/cm², ferroelectric and related oxides are preferable.



Dielectrics	ε_r
SiO_2	3.9
Si_3N_4	7 ~ 9
Ta_2O_5	20 ~ 50
$SrTiO_3$ (thin film)	100 ~ 600
$Pb(Zr,Ti)O_3$ (thin film)	500 ~ 1000

$SrTiO_3$ Thin Film Capacitor Fabrication



- **Advantages**
  - Low crystallization temperature
  - Ease of composition control

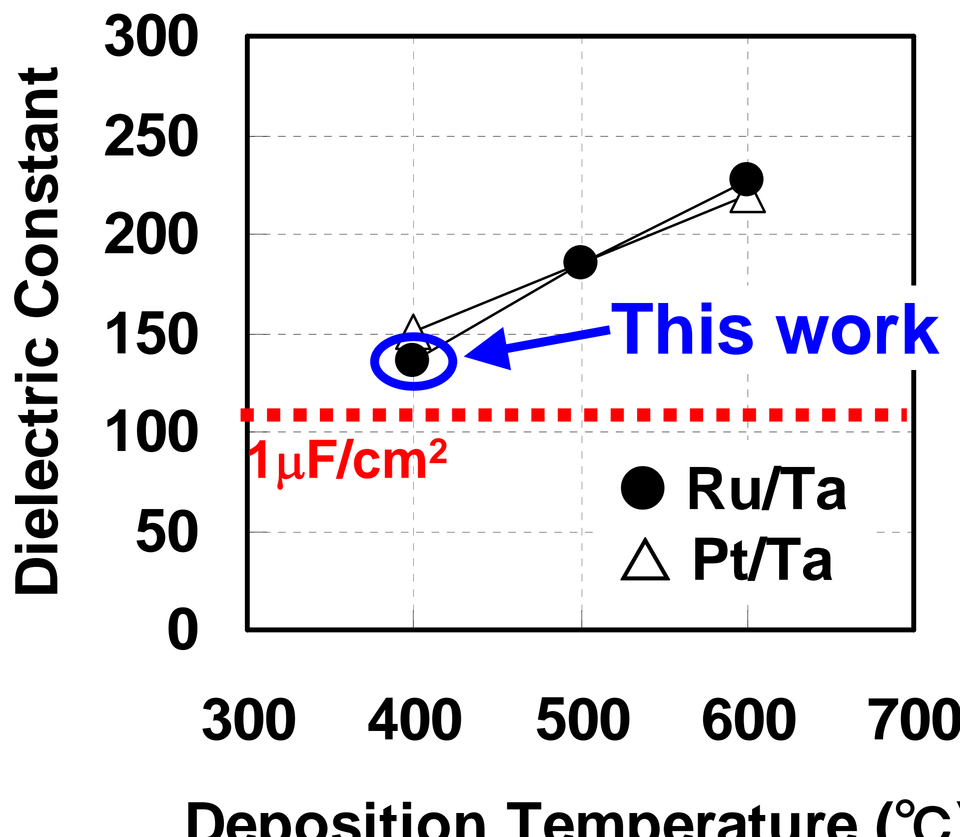
- **Examples of STO capacitor applications**
  - DRAM cell capacitor (on-chip)
  - GaAs MMIC (on-chip)
  - Polyimide-based flexible capacitor (discrete)

Reactive sputtering conditions

Target	$SrTiO_3$ ceramics
Sputtering Gas	80% Ar - 20% O_2
Deposition Temp.	400°C
Bottom Electrode	Ru/Ta
Top Electrode	Ru

Properties for Sputtered STO Thin Films

Higher ε_r than 100, and good insulating properties



Capacitor size: 100μm x 100μm
STO thickness: 100nm

K. Takemura, A. Ohuchi, and A. Shibuya, "Si Interposers Integrated with SrTiO3 Thin Film Decoupling Capacitors and Through-Si-Vias," IEEE 9th VLSI Packaging Workshop in Japan, pp. 127-139, 2008.

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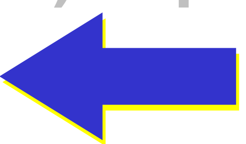
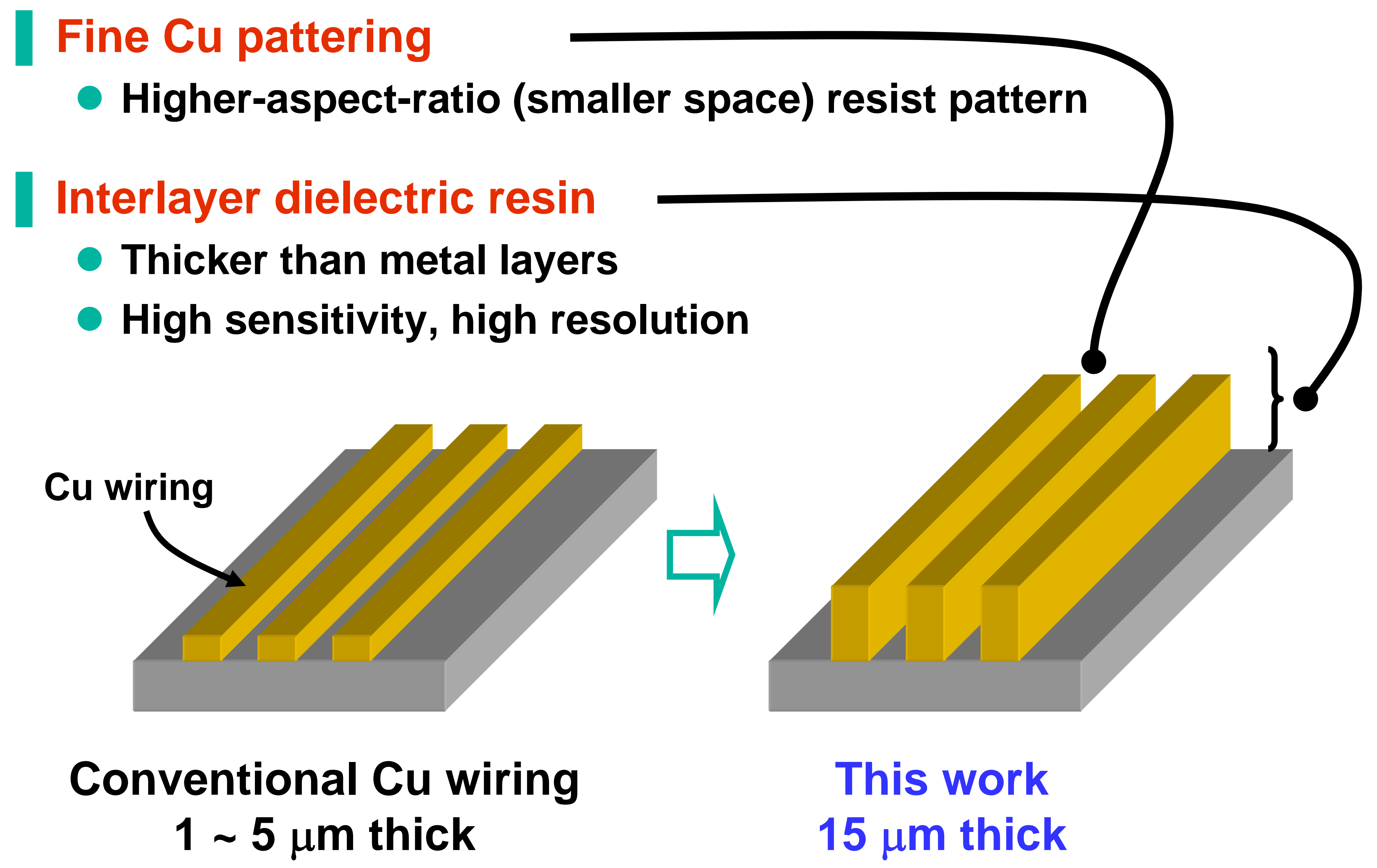
- **15μm thick inductor** 

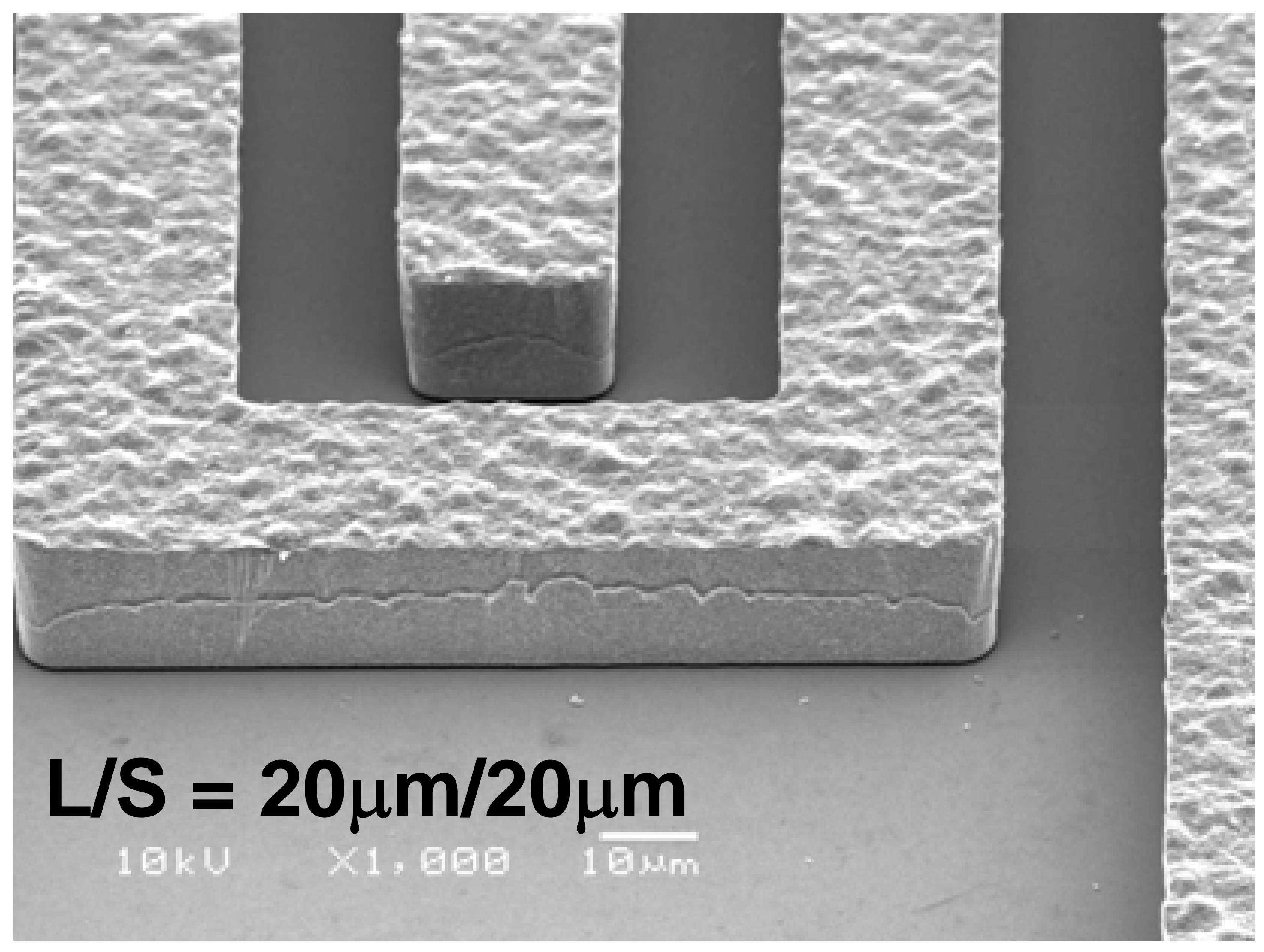
Measured Efficiency of Buck Converter

Summary

Process Issues for 15-μm-Thick Cu Wiring

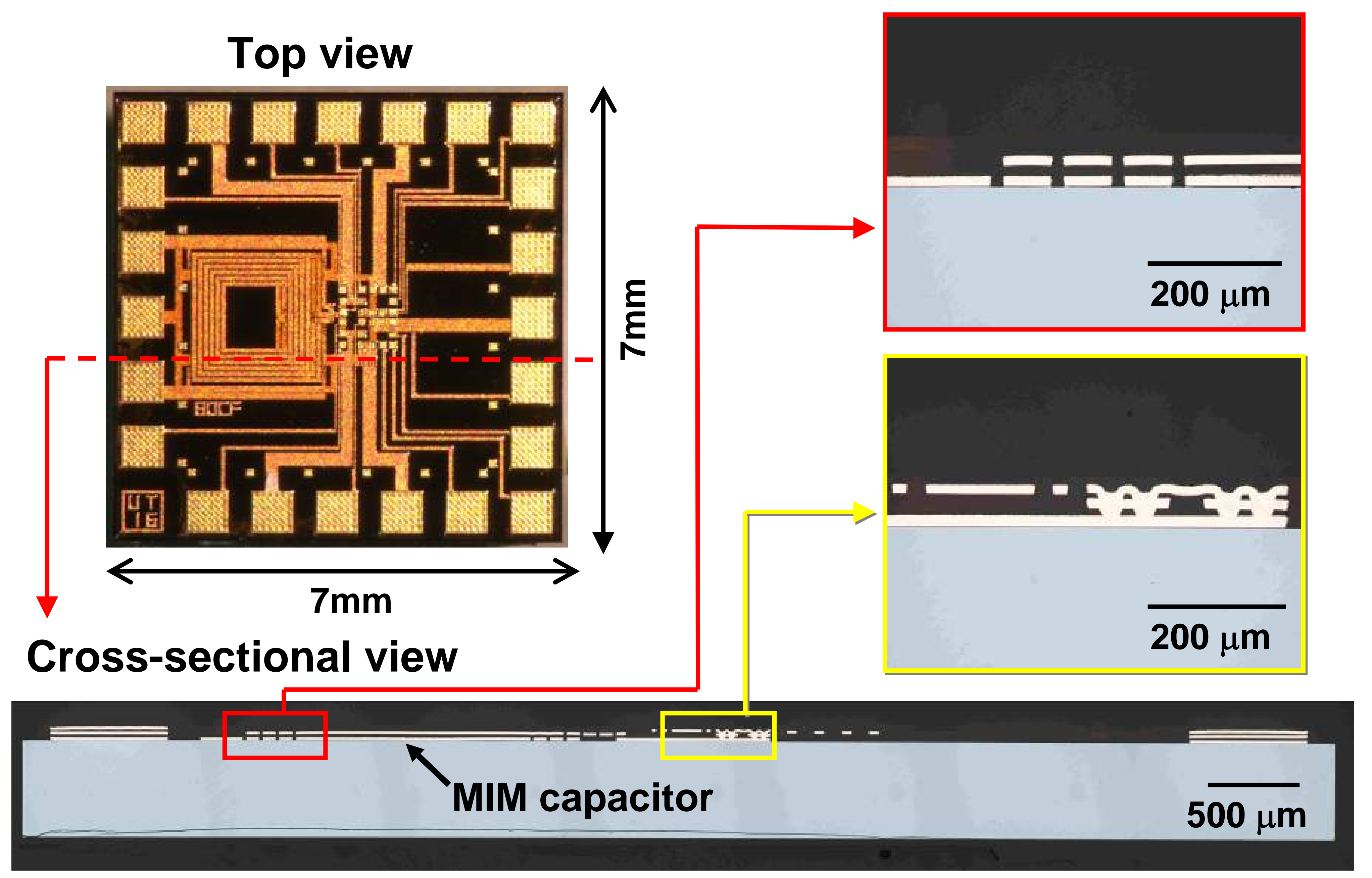


Fabricated 15-μm-Thick Cu Wiring



15μm thick, Line/Space = 20μm/20μm

Photographs of Fabricated Si Interposer (1)

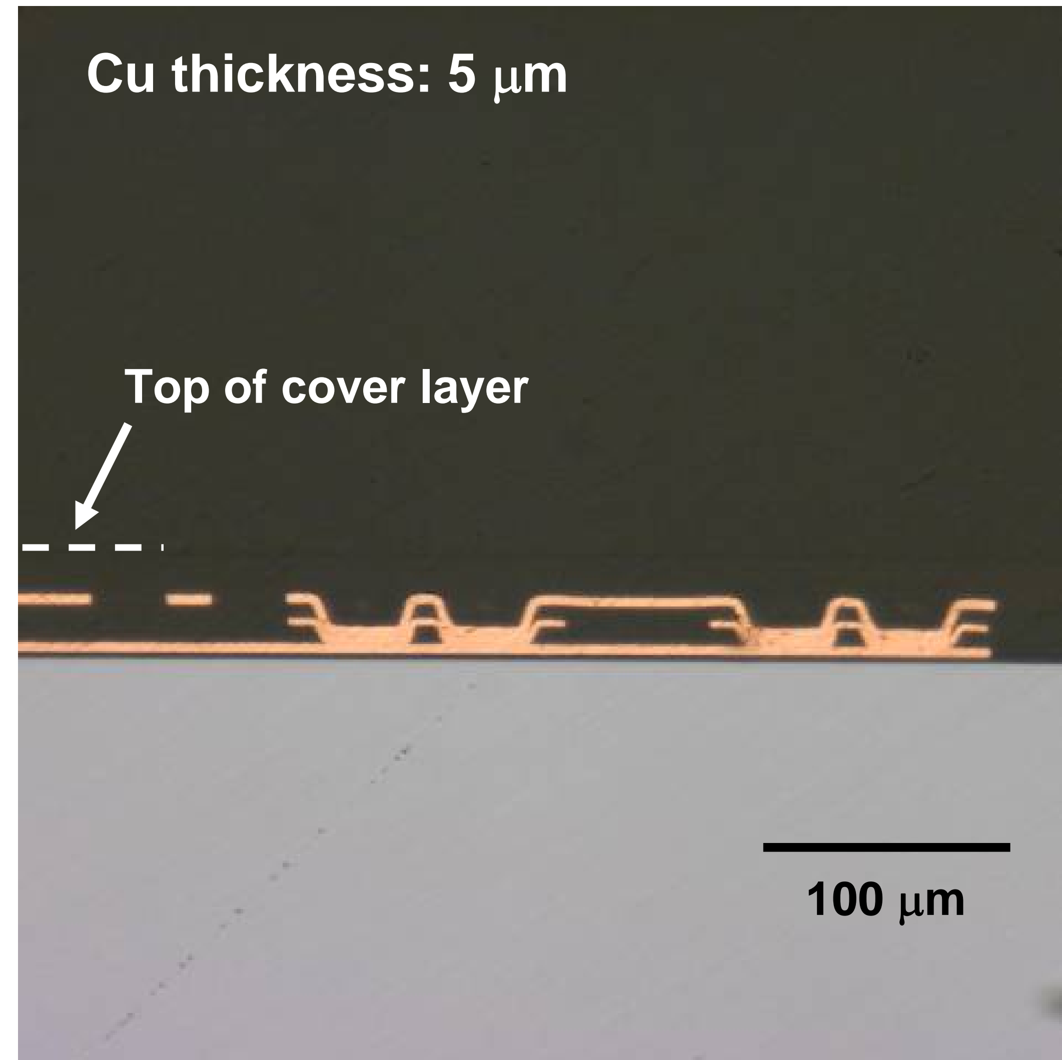


Photographs of Fabricated Si Interposer (2)

Cu thickness: 15 μm

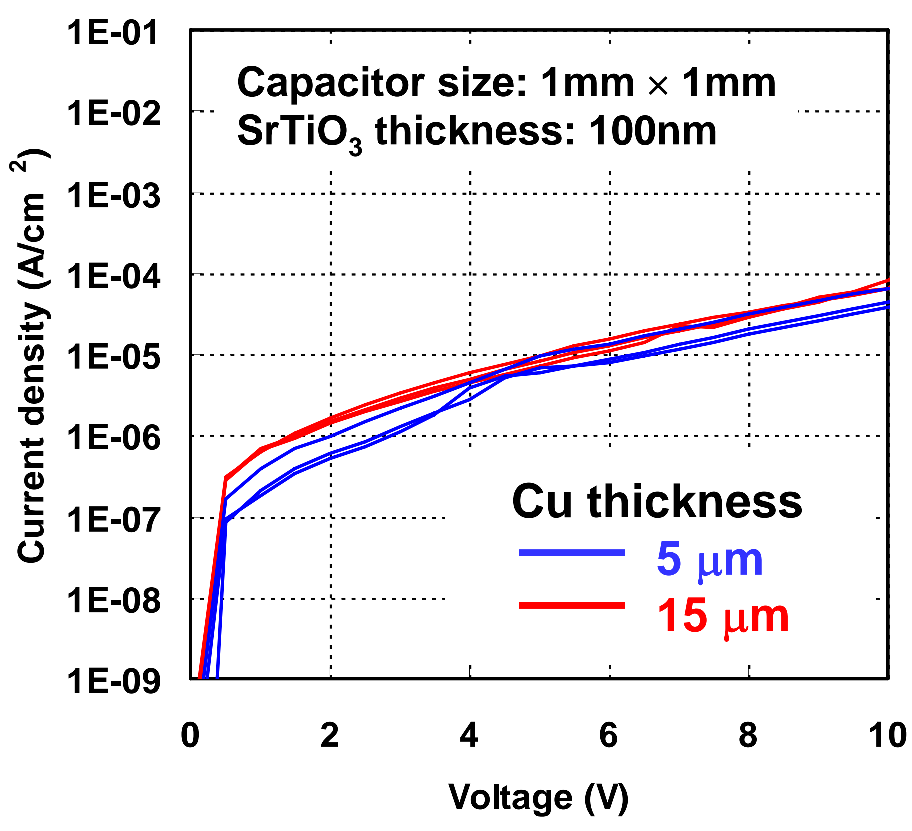
Top of cover layer

100 μm

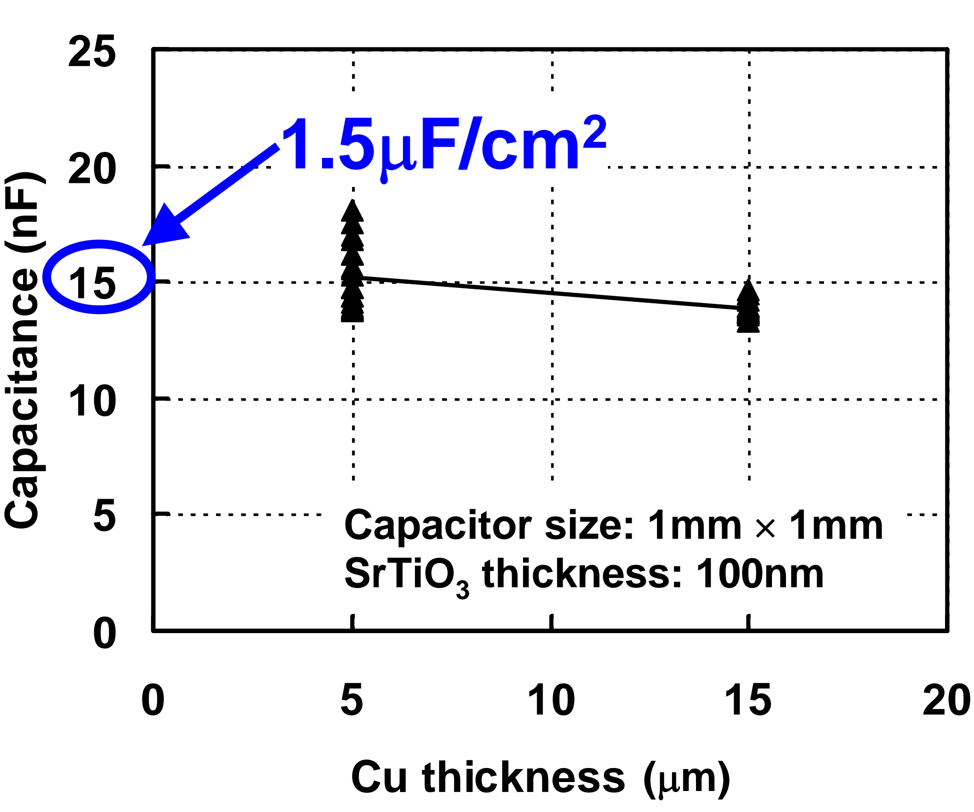


Properties for Embedded $SrTiO_3$ Capacitors

Leakage current



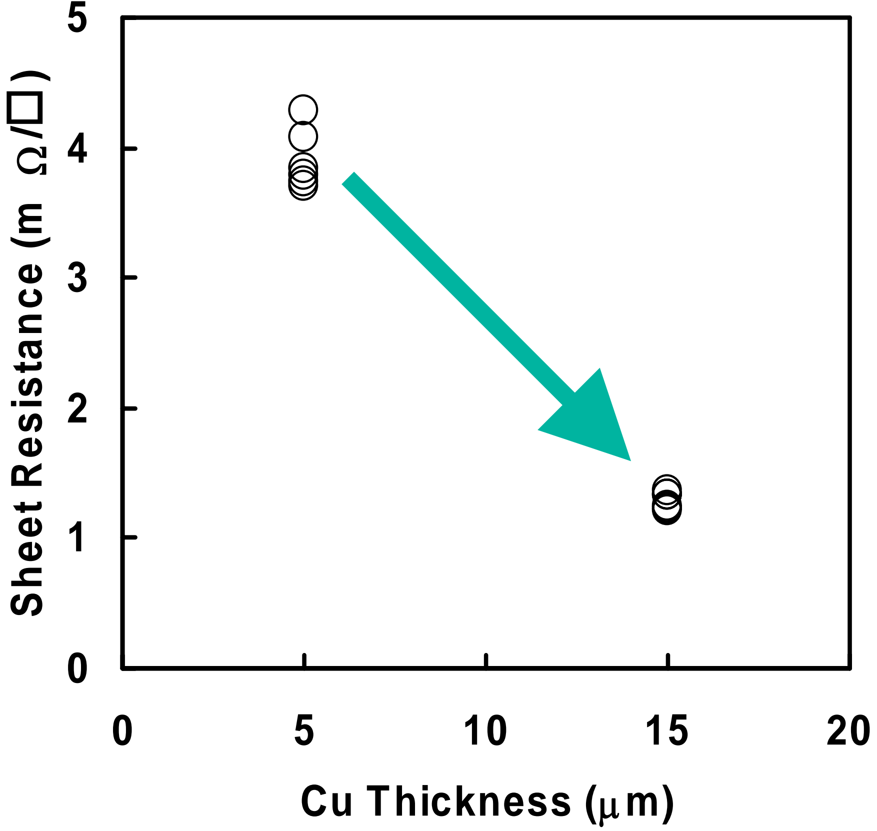
Capacitance



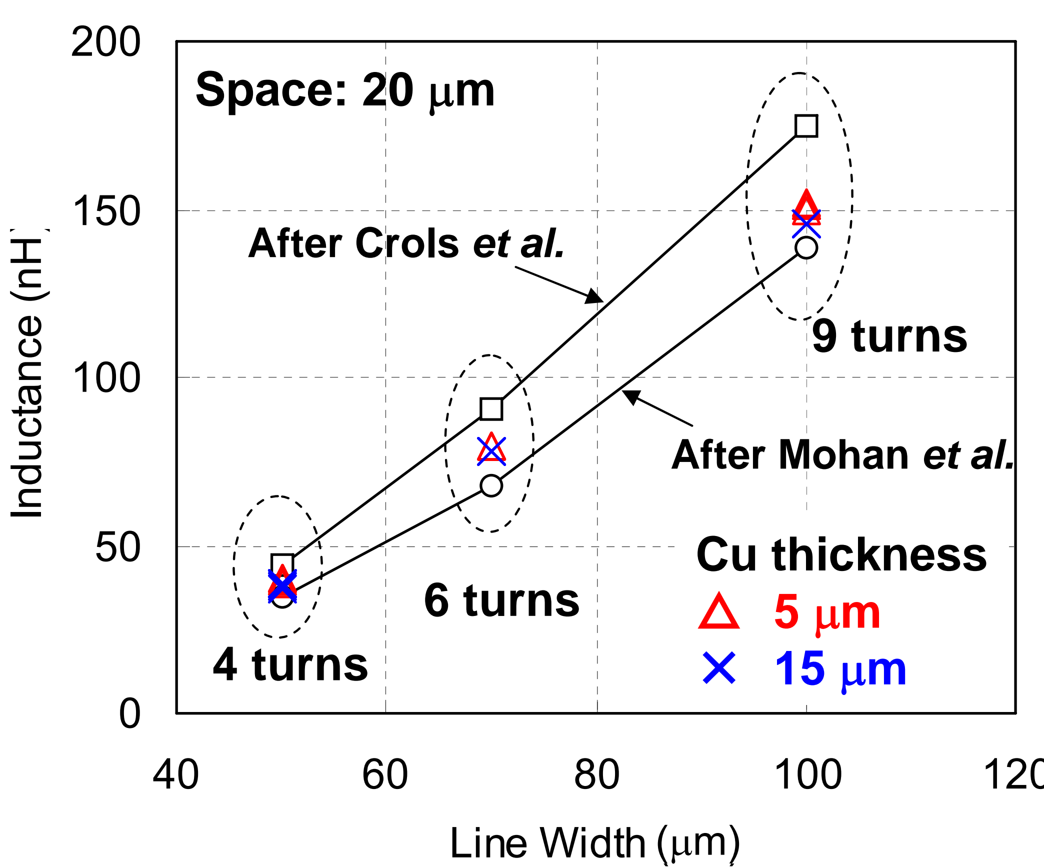
Capacitor properties are not affected by Cu thickness.

Properties of Cu Wirings and Spiral Inductors

Sheet resistance



Inductance



According to Cu thickness, only sheet resistance reduces.

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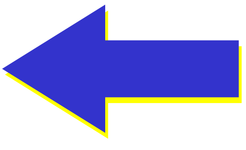
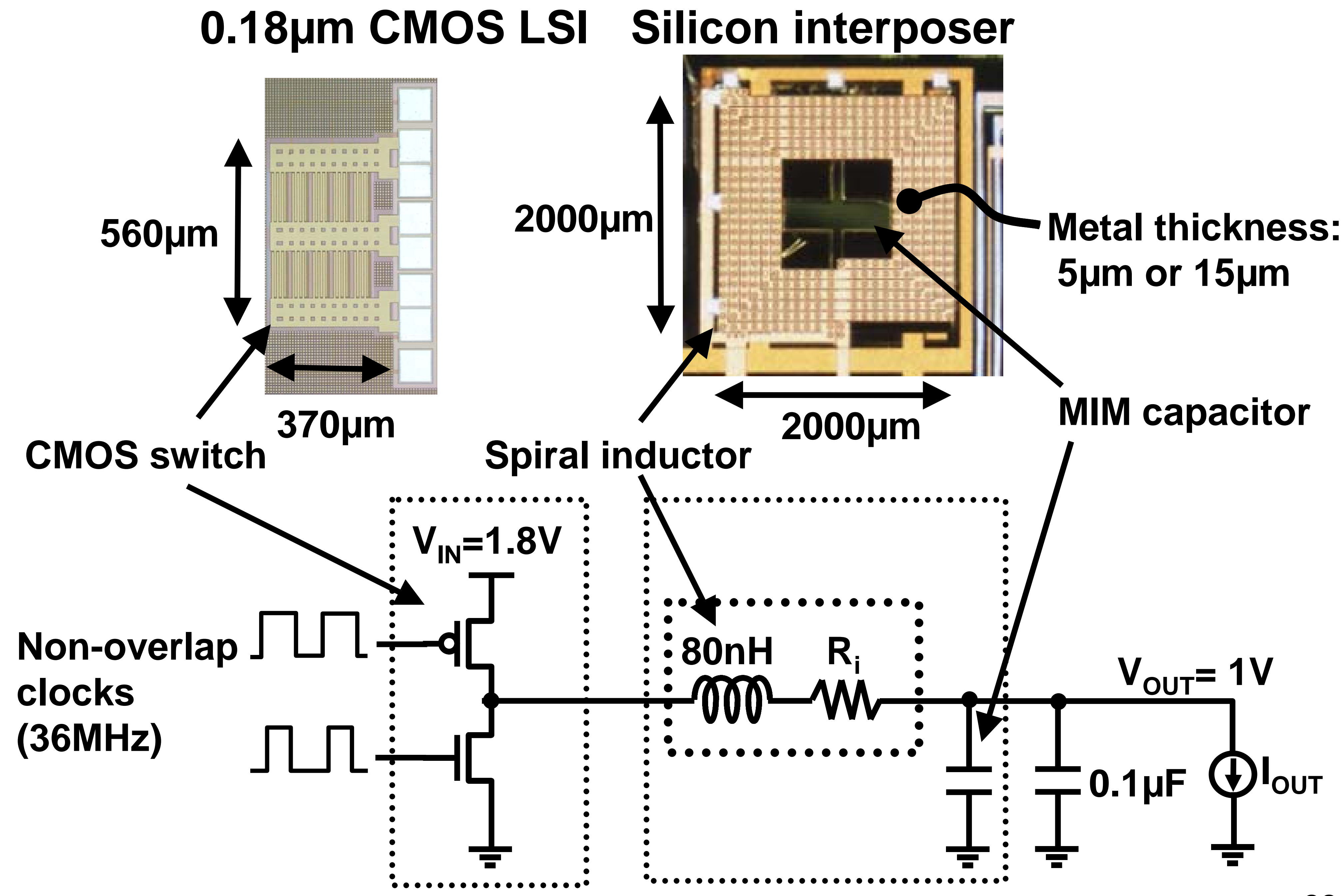
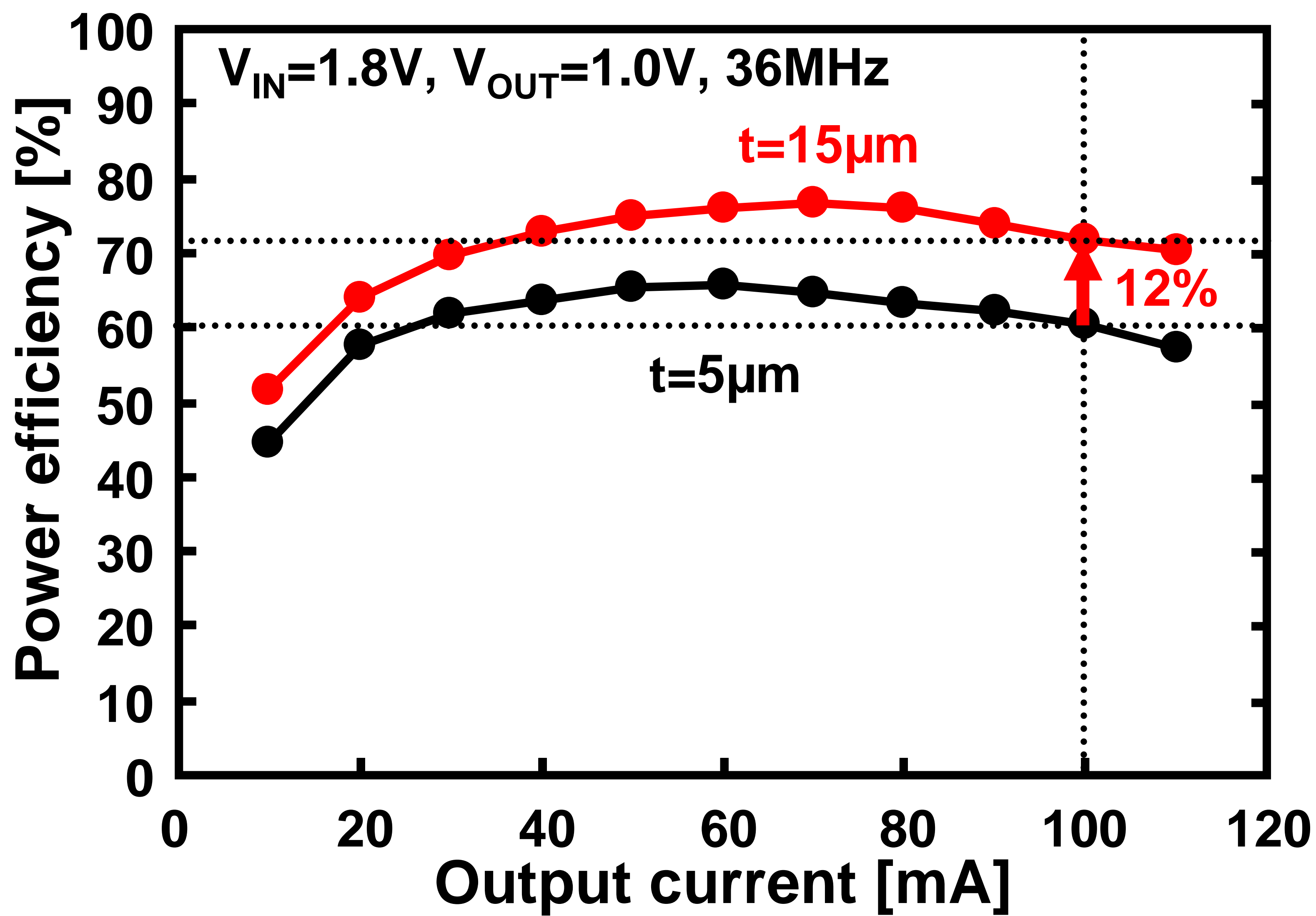
- **Measured Efficiency of Buck Converter** 
- **Summary**

Fabricated Buck Converter



Measured Efficiency of Buck Converter



A 15-µm-thick inductor improves power efficiency by 12 %.

Summary

- **3D stacked buck converter with C and L on Si Interposer**

- **1.5μF/cm² $SrTiO_3$ (STO) capacitor**
  - **100nm**
  - **ε_r>100**

- **15μm thick inductor**
  - **2mm x 2mm**
  - **80nH**

- **Si interposer with a 15-μm-thick inductor improves power efficiency of the buck converter by 12 %.**

Acknowledgement

This work was entrusted by NEDO “Development of Functionally Innovative 3D-Integrated Circuit (Dream Chip) Technology” project that is based on the Japanese government's METI “IT Innovation Program”.