3D Stacked Buck Converter with SrTiO$_3$ (STO) Capacitors on Silicon Interposer

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Outline

Introduction
- Fine-grained voltage engineering
- 3D stacked DC-DC (buck) converter

Silicon Interposer
- 1.5μF/cm² SrTiO₃ (STO) capacitor
- 15μm thick inductor

Measured Efficiency of Buck Converter

Summary
Power Supply for High-Performance 3D-LSIs

- Heterogeneous integration $\Rightarrow$ Various power supplies
- Low-power and high-performance $\Rightarrow$ Fine-grained voltage engineering

On-chip DC-DC (buck) converters are essential for 3D LSIs.
On-Chip Buck Converters

Disadvantages of on-chip inductors

- Smaller inductance < 10 nH
- Area penalty
- Parasitic resistance due to thin conductors

Inductors should be thick and separated from a Si chip.
Concept of 3D Stacked Distributed Power Supply

Output LC filters is embedded into a Si interposer.

Sensor, MEMS, High voltage generator, Analog, RF etc. (3D stacked)

Parallel processors with own DC-DC converters

Fine-grain power supply voltage

Stacked memories

Si interposer

L & C cell array

Pads & bumps

Power supply & other wires

Inductors Capacitors

Embedded

Package

Si interposer

Base chip
Proposed 3D Stacked Buck Converter

Area penalty and parasitic resistance will be small.

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Summary
Silicon Interposer

- Silicon substrate
- MIM capacitor
- Chemically amplified positive resin
- Via hole = 30µmØ
- Minimum Line/Space = 20µm/20µm
- 15µm thick electroplated Cu (3 layers)
- p-TEOS (1µm)
- SiO₂ (300nm)
Fabrication Process of Silicon Interposer

MIM cap. fabrication

Cu electroplating

ILD resin formation

Repetition

ILD: Interlayer dielectric
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Summary
Capacitor Dielectrics

When the target capacitance density is higher than $1\mu$F/cm$^2$, ferroelectric and related oxides are preferable.

<table>
<thead>
<tr>
<th>Dielectrics</th>
<th>$\varepsilon_r$</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_2$</td>
<td>3.9</td>
</tr>
<tr>
<td>Si$_3$N$_4$</td>
<td>7 ~ 9</td>
</tr>
<tr>
<td>Ta$_2$O$_5$</td>
<td>20 ~ 50</td>
</tr>
<tr>
<td>SrTiO$_3$ (thin film)</td>
<td>100 ~ 600</td>
</tr>
<tr>
<td>Pb(Zr,Ti)O$_3$ (thin film)</td>
<td>500 ~ 1000</td>
</tr>
</tbody>
</table>

$\varepsilon_r$>100 for $1\mu$F/cm$^2$

This work (100nm, 1.5$\mu$F/cm$^2$, $\varepsilon_r$>100)
SrTiO$_3$ Thin Film Capacitor Fabrication

- **Advantages**
  - Low crystallization temperature
  - Ease of composition control

- **Examples of STO capacitor applications**
  - DRAM cell capacitor (on-chip)
  - GaAs MMIC (on-chip)
  - Polyimide-based flexible capacitor (discrete)

### Reactive sputtering conditions

<table>
<thead>
<tr>
<th>Target</th>
<th>SrTiO$_3$ ceramics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sputtering Gas</td>
<td>80% Ar - 20% O$_2$</td>
</tr>
<tr>
<td>Deposition Temp.</td>
<td>400°C</td>
</tr>
<tr>
<td>Bottom Electrode</td>
<td>Ru/Ta</td>
</tr>
<tr>
<td>Top Electrode</td>
<td>Ru</td>
</tr>
</tbody>
</table>
Properties for Sputtered STO Thin Films

Higher $\varepsilon_r$ than 100, and good insulating properties

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Summary
Process Issues for 15-μm-Thick Cu Wiring

- **Fine Cu patterning**
  - Higher-aspect-ratio (smaller space) resist pattern

- **Interlayer dielectric resin**
  - Thicker than metal layers
  - High sensitivity, high resolution

**Conventional Cu wiring**
- 1 ~ 5 μm thick

**This work**
- 15 μm thick
Fabricated 15-μm-Thick Cu Wiring

L/S = 20μm/20μm

15μm thick, Line/Space = 20μm/20μm
Photographs of Fabricated Si Interposer (1)

Top view

Cross-sectional view

MIM capacitor

200 μm

500 μm
Photographs of Fabricated Si Interposer (2)

Cu thickness: 15 \( \mu \text{m} \)

Cu thickness: 5 \( \mu \text{m} \)

Top of cover layer
Properties for Embedded SrTiO₃ Capacitors

Leakage current

Capacitor properties are not affected by Cu thickness.
According to Cu thickness, only sheet resistance reduces.
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Summary
Fabricated Buck Converter

0.18µm CMOS LSI  Silicon interposer

CMOS switch

Non-overlap clocks (36MHz)

Vin = 1.8V

Spiral inductor

80nH

Ri

Metal thickness: 5µm or 15µm

MIM capacitor

Vout = 1V

0.1µF

Iout
A 15-μm-thick inductor improves power efficiency by 12%.
Summary

- 3D stacked buck converter with C and L on Si Interposer
- 1.5µF/cm² SrTiO₃ (STO) capacitor
  - 100nm
  - εᵣ > 100
- 15µm thick inductor
  - 2mm x 2mm
  - 80nH
- Si interposer with a 15-µm-thick inductor improves power efficiency of the buck converter by 12%.
Acknowledgement

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