Silicon, GaAs and GaN Technologies for Monolithic DC-DC Power Converter ICs

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• David Anderson – Texas Instruments
• Peter Wright – Tri-Quint
Outline

• Device FOM
• Power Converter ICs
  – Si
  – GaAs
• GaN Integration
• Summary
Power Supplies For Portable Electronics

System Trends
- Point of Load power conversion
- IC Voltage Scaling
- Slow Battery Capacity Increase
- Miniaturization

Power Electronics
- Low V – High I
- Higher Switching Frequency, Bandwidth
- Integration / System on Chip

Envelope Tracking
Power Switching Figure of Merit

\[
FOM = R_{ON} \times Q_G = R_{ON,SP} \frac{L_{CH}}{\mu_{CH} Q_{CH}} + \frac{L_D}{\mu_D Q_D} + R_{EXT}
\]

Increase Mobility

\( R_{EXT} \): Interconnects

Reduce Channel length
  
  Scaling

Reduce \( L_D \)
  
  Compromises breakdown voltage
  
  High Bandgap Materials

Ideal Drift Electric Field

Critical Electric Field

\[ \text{Area} = \text{Breakdown Voltage} \]

\[ \text{Drain (SUPPLY)} \]

\[ \text{Gate (OFF)} \]

\[ L_D \]
## Comparison of Device Technologies

<table>
<thead>
<tr>
<th>Device</th>
<th>HEMT</th>
<th>LDD NMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Structure</strong></td>
<td>![HEMT Diagram]</td>
<td>![LDD NMOS Diagram]</td>
</tr>
<tr>
<td><strong>Technology</strong></td>
<td>AlGaAs/InGaAs/AlGaAs</td>
<td>AlGaN / GaN</td>
</tr>
<tr>
<td>$\mu_{CH}$ ($cm^2V^{-1}s^{-1}$)</td>
<td>(~6000)</td>
<td>(~1800)</td>
</tr>
<tr>
<td>$\mu_D$ ($cm^2V^{-1}s^{-1}$)</td>
<td>(~6000)</td>
<td>(~1800)</td>
</tr>
<tr>
<td>$\frac{E_C,Lat}{R_{Ext}}$</td>
<td>\ (~25V/\mu m)</td>
<td>\ (~150V/\mu m)</td>
</tr>
<tr>
<td>$R_{Ext}$</td>
<td>\ (~0.2 \Omega.mm)</td>
<td>\ (~0.2 \Omega.mm)</td>
</tr>
</tbody>
</table>
| **Features** | • Highest Mobility  
• Intermediate Bandgap  
• Suited for (5-40V) | • Widest Bandgap but for low BV, it makes less impact for FOM  
• Ideal for high voltages (>40V) | • Lower parasitics, more conducive to scaling  
• Ideal for low voltages (<5V) |

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**PowerSoC**  
November 15, 2012  
T.P. Chow
To take advantage of Wide Bandgap for low voltage devices, extremely small scaling rules are required.

GaAs has the best (smallest) FOM for <20V for 0.1µm feature size or above.

Phase Shedding/Segmentation

- Operation phases/segments are switched ON/OFF depending on different load conditions.
- Maintain constant efficiency at different loads.
  - Easy to extend the load current range by adding more phases.
- Drawbacks:
  - Require larger inductor value or variable switching frequency when reducing phases.
  - Output ripple may be large: large output cap is required.
  - Require digital control blocks: ADC, etc.
Inductor Coupling in Output Network

- Negative coupled inductors bring better efficiency at two-segment & four-segment operation:
  - Larger equivalent inductance.
  - Ripple cancellation.

You might want to add equations to prove this.
Circuit Implementation

Phase 0°, Segment 1

Phase 0°, Segment 2

Phase 180°, Segment 3

Phase 180°, Segment 4

Cascaded Delay Chain with Automatic Duty Ratio Correction Loop

Hysteresis Controller
Circuit Implementation

- HS and LS switches are sized at 5V-to-2.5V conversion ratio and 0.5 A load current.
  - PMOS: 40 mm, NMOS: 15 mm.
- Combined HS-LS resonant gate driver with partially shared inductance is adopted.
  - Energy distribution is changed and stored in resonant inductor.
  - Soft switching is realized by deliberated designed gate signals.
Resonant gate driver design

- Energy distribution is changed and stored in resonant inductor.
- Soft switching is realized by modifying the gate signals.
- Tradeoffs between gate driver loss and main switch’s switching loss.
Coupled inductor design

- Coupled inductors are implemented on PC-Board.
- 1 oz, 20 μm thick copper layer.
- Min. 2.7 mil spacing between layers.

<table>
<thead>
<tr>
<th></th>
<th>Positive Coupled Ind.</th>
<th>Negative Coupled Ind.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area (mm²)</td>
<td>2.58 × 2.37</td>
<td>3.4 × 4.35</td>
</tr>
<tr>
<td>Width (μm)</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>Spacing (μm)</td>
<td>120</td>
<td>200</td>
</tr>
<tr>
<td>Turns</td>
<td>2.5</td>
<td>1.5</td>
</tr>
<tr>
<td>L (nH)</td>
<td>6.27</td>
<td>6.48</td>
</tr>
<tr>
<td>$R_{dc}$ (mΩ)</td>
<td>32</td>
<td>32</td>
</tr>
<tr>
<td>$k$</td>
<td>0.799</td>
<td>0.397</td>
</tr>
<tr>
<td>Q @ 100MHz</td>
<td>37</td>
<td>45</td>
</tr>
</tbody>
</table>
Feedback control loop

• Hysteresis controller for fast transient response and large close loop bandwidth.

• Synchronization between two phase operation:
  – 0.5T delayed signal produced from voltage controlled delay cells.
  – Unbalanced duty ratio will cause current sharing problem.
  – Automatic duty ratio corrector.
Eight cascaded delay cells, each producing 0.625 ns delayed signal with 1.7 V control voltage.
Measurement results

- Implemented in 0.5 μm CMOS technology with 6 Metal layers + 1 distribution layer
- Flip clip package. Vias footprint: 5 X 6
- 4 layer PCB.
- Load capacitor: 47 μF
- Feedback network:
  - $R_f: 1K\Omega$, $C_f: 2.7$ pF
Measurement results

Output transient response with \( V_{\text{in}} = 4 \, \text{V}, \, V_{\text{out}} = 2.3 \, \text{V} \). Voltage ripple is 50 mV.

Tracking model results with sinusoidal reference signal.
Efficiency vs. output voltage at two-phase four-segment operation with resonant gate drivers

Phase shedding/segmentation results with Vin = 4 V, Vout = 2 V.
## Results summary and comparison

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.5 μm CMOS, 5 V &amp; 1.8 V devices</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Switching frequency</strong></td>
<td>100 MHz</td>
</tr>
<tr>
<td><strong>Die area</strong></td>
<td></td>
</tr>
<tr>
<td>CMOS die</td>
<td>7.78 mm²</td>
</tr>
<tr>
<td>Positive cou. ind.</td>
<td>6.61 mm²</td>
</tr>
<tr>
<td>Negative cou. ind.</td>
<td>15.3 mm²</td>
</tr>
<tr>
<td><strong>Supply voltage</strong></td>
<td></td>
</tr>
<tr>
<td>Power stage</td>
<td>4 V</td>
</tr>
<tr>
<td>Comparator</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Num. of phases/ segments</td>
<td>2 / 4</td>
</tr>
<tr>
<td>Peak Output</td>
<td>3 V/1.86 A</td>
</tr>
<tr>
<td>Output voltage ripple</td>
<td>50 mV</td>
</tr>
<tr>
<td>Peak efficiency</td>
<td>77.4 %</td>
</tr>
</tbody>
</table>
## Comparison with Prior Art

<table>
<thead>
<tr>
<th>Ref</th>
<th>Tech.</th>
<th># Phases</th>
<th>In/Out Voltage V/V</th>
<th>Output Current (A)</th>
<th>Sw. Freq. (MHz)</th>
<th>L (nH)</th>
<th>Peak Eff. (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel JSSCC’05</td>
<td>90 nm CMOS</td>
<td>4</td>
<td>1.2/0.9</td>
<td>0.3</td>
<td>233</td>
<td>6.8</td>
<td>82.5</td>
</tr>
<tr>
<td>RPI APEC’07</td>
<td>0.18 µm BiCMOS</td>
<td>2</td>
<td>1.8/0.9</td>
<td>0.5</td>
<td>200</td>
<td>2.14</td>
<td>64</td>
</tr>
<tr>
<td>ISSCC ‘08</td>
<td>0.25 µm BiCMOS</td>
<td>1</td>
<td>3.6/3.1</td>
<td>0.62</td>
<td>130</td>
<td>110</td>
<td>83</td>
</tr>
<tr>
<td>Trans. PE 2012</td>
<td>0.25 µm BiCMOS</td>
<td>1</td>
<td>3.6/2.2</td>
<td>0.33</td>
<td>200</td>
<td>51</td>
<td>77</td>
</tr>
<tr>
<td>ECCE’09</td>
<td>65nm CMOS</td>
<td>1</td>
<td>1.2/0.85</td>
<td>0.08</td>
<td>100</td>
<td>11</td>
<td>87.5</td>
</tr>
<tr>
<td>JSSCC’07</td>
<td>0.35µm CMOS</td>
<td>1</td>
<td>3.3/2.3</td>
<td>0.06</td>
<td>200</td>
<td>22</td>
<td>86</td>
</tr>
<tr>
<td>This work</td>
<td>0.18 µm CMOS</td>
<td>2</td>
<td>4/3</td>
<td>1.8</td>
<td>100</td>
<td>5</td>
<td>77.4</td>
</tr>
</tbody>
</table>
Comparison with Prior Art

This work, fully integrated switches, drivers, control circuits and integrated air-core inductors.
Intrinsic Device ON Resistance

Gated Hall Measurements

100μm pHEMT Layout

Output Characteristics

- Intrinsic Specific $R_{ON} = 1.46 \, \Omega \cdot \text{mm}$
- TLM Measurements show that 64% of the resistance is from contact and access Resistance
ON Resistance: Interconnect Metallization Scheme

Unit Cell ON Resistance due to Metal Interconnects

<table>
<thead>
<tr>
<th>Gate Width (mm)</th>
<th>Specific ON Resistance (Ω·mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1</td>
<td>1.0</td>
</tr>
<tr>
<td>1</td>
<td>1.3</td>
</tr>
<tr>
<td>10</td>
<td>2.0</td>
</tr>
</tbody>
</table>

- Model
- Measured

Flip Chip Bonding using Cu Bumps

Flip Chip Interconnect Scheme

Unit Cell: Layout for Flip Chipped Device

PowerSoC  November 15, 2012  T.P. Chow
22 and 32V GaAs pHEMTs Figure of Merit

**Characterization Results**

<table>
<thead>
<tr>
<th>BV</th>
<th>Gate Width</th>
<th>Current</th>
<th>$R_{ON}$</th>
<th>$Q_G$</th>
<th>FOM</th>
</tr>
</thead>
<tbody>
<tr>
<td>22</td>
<td>5 mm</td>
<td>0.5 A</td>
<td>268 mΩ</td>
<td>44 pC</td>
<td>12 mΩ.nC</td>
</tr>
<tr>
<td>32</td>
<td>5 mm</td>
<td>0.5 A</td>
<td>303 mΩ</td>
<td>58 pC</td>
<td>18 mΩ.nC</td>
</tr>
</tbody>
</table>

**Breakdown Voltage vs FOM**

**22V GaAs pHEMT vs Silicon**

**32V GaAs pHEMT vs Silicon**
pHEMT DC-DC Converter: Output Stage Prototype

- **Specifications**
  - Target Application: Envelope Tracking in RF Amplifiers
  - Switching Frequency = 100MHz
  - Buck Type, 4.2-11V in, 1.5-3.5V Out
  - Peak $P_{OUT} = 6.6W$
  - Target tracking bandwidth: 10MHz
  - pHEMT “Dummy CMOS” Controller
Converter Efficiency

**Efficiency vs Power**

- Efficiency vs Power
- V_{OUT} = 3.375V
- V_{OUT} = 2.25V
- V_{OUT} = 1.125V

**Effect of Synchronous Rectification**

- Synchronous Rectifier
- Diode Rectifier
- \( V_{IN} = 4.5\) V
- \( R_{LOAD} = 3.3\) \(\Omega\)
- Freq = 100MHz

**Power Loss Components**

- \( V_{OUT} = 3.375, \) Efficiency = 87%
- \( V_{OUT} = 2.25, \) Efficiency = 75.4%
- \( V_{OUT} = 1.125, \) Efficiency = 50.9%

- Inductor: 0.4%, 6.4%, 5.2%
- Gate Drive: 1.8%, 5.2%, 9.5%
- High Side Switch: 12.3%, 12.6%, 5.2%
- Rectifier: 11.9%, 0.0%, 0.1%
- Other: 0.8%

- At low power, the power losses are dominated by gate drive
- GaAs pHEMT drivers consume static power
- Can be improved by CMOS drivers
DC-DC Converter Performance

**Efficiency vs Voltage Rating**

- Power Efficiency vs Voltage Rating (V)
- This work

**Efficiency vs Switching Frequency**

- Power Efficiency vs Switching Frequency (MHz)
- This work

- Discrete MOS
- 0.35um CMOS
- 0.25um CMOS
- 0.18um CMOS
- 130 nm CMOS
- 90nm CMOS
- 65nm CMOS
- GaAs VFET
- GaAs HBT
- GaAs MESFET
GaAs p-HEMT Resonant Gate Driver

Single phase GaAs converter with low side resonant gate driver.

GaAs single phase converter with conventional gate drivers
GaAs single phase converter with low side resonant gate driver

Efficiency (%)

Gate Driver Loss/Total Power Loss (%)
Monolithic Integration

SL-ERC Project S1.3.1:
- Start date: July, 2010
- Duration: Through June, 2018

Objective:
- Develop a process to enable monolithic integration of LEDs, control logic and power transistors. This IC will have the full spectrum of smart lighting features for a wider variety of applications due to reduced package size and cost and improved reliability.
RPI MOS Channel-HEMT

MOS Channel-HEMT on Si

- $BV = 350V$
- $R_{on,sp} = 4.0\text{mOhm-cm}^2$
- $V_T = 0.3V$
- $L_{ch} = 0.3\text{um}$
- $L_{drift} = 8\text{um}$

Z. Li and T.P. Chow, ISPSD 2012
The ability to use Silicon as a substrate for LEDs will lead to a lower overall cost. To prepare for this paradigm shift, we have included research on GaN-MOS-HEMTs built on a Silicon substrate.

Left to Right: MOS-HEMT structure for GaN on Silicon, Current LED structure, Proposed GaN-CMOS structure.

GaN controls and power FETs will enable high frequency and high efficiency switching for data and power conversion applications.
**Integration Approaches**

*First:* Grow wafers with necessary EPI layers, use subtractive etching to make components

- **Starting EPI**
  - P-GaN
  - InGaN-GaN QW Lay
  - N-GaN
  - P-GaN
  - GaN
  - $\text{Al}_{0.21}\text{GaN}$
  - $\text{Al}_{0.05}\text{GaN}$
  - Buffer

- **MOS-HEMT Etch**
- **CMOS Etch**
  - N-FET
  - P-FET
- **LED Etch**

**Advantages**
- High temperature steps of layer growth complete before processing

**Risks**
- Thermal budget of processing may be incompatible
- Highly non-planar, lithography obstacle
- Larger thermal path for cooling LEDs
- Need selective or high controlled etch to hit depth
ACCOMPLISHMENTS

Monolithic Integration

LED structure successfully grown on HEMT-structure

- Initial tests show functioning LEDs
- Evaluation of HEMT structure underway via MOS-capacitors

Collaboration with Wetzel (S1.2.2) gives flexibility to grow LEDs on HEMT structure without degrading 2DEG (2D electron gas)
Process compatibility

Monolithic Integration
- LED epi selectively etched to fabricate MOS capacitors on HEMT structure
- Etch depth controlled to prevent removal of GaN Cap (20nm thick despite ~800nm etch)
- $C\Delta V$ yields charge required to deplete 2DEG
- Growth cycle of LED epi did not compromise concentration of 2D electron gas (2DEG)
  - 2DEG of Original epi: $3.2 \times 10^{12}$/cm$^2$
  - 2DEG of HEMT/LED epi: $3.0 \times 10^{12}$/cm$^2$
References

Thank You!

Any Question?
Output Network

• Positive coupling (k1):
  – Larger k1 generates larger effective inductance.

• Negative coupling (k2):
  – Ripple reduction is correlated with duty ratio.

![Graph showing current ripple reduction factor vs k1 with k2 = 0.75]
Effect of Coupling

$k_1 = 0.8$

Ripple reduction factor for $k_2 > 0$

Ripple reduction factor for $k_2 \leq 0$
Efficiency at Higher Freq.

- Most of the losses coming from transistor.
- Diode and gate drive losses negligible.
Simulation

• SiC Simulation
  – Switching at 600V, 10A: Power ~6kW
  – Gate Drive: 0 to 20V

• GaN Simulation
  – Switching at 600V, 10A: Power ~6kW
  – Gate Drive: 0 to 5V (Gate turns on for Vg>5V)
Efficiency Comparison

- Most of the losses coming from transistor.
- Diode and gate drive losses negligible.
Efficiency

![Graph showing efficiency versus frequency for different types of transistors: SiC, EPC, EPC with 3X Ron, and MOSC HEMT. The graph demonstrates a decrease in efficiency with an increase in frequency.](image-url)