International Workshop on Power Supply on Chip 2012

Session 2: Power Semiconductor Technologies
“PMIC technologies for integrated DC-DC converters”

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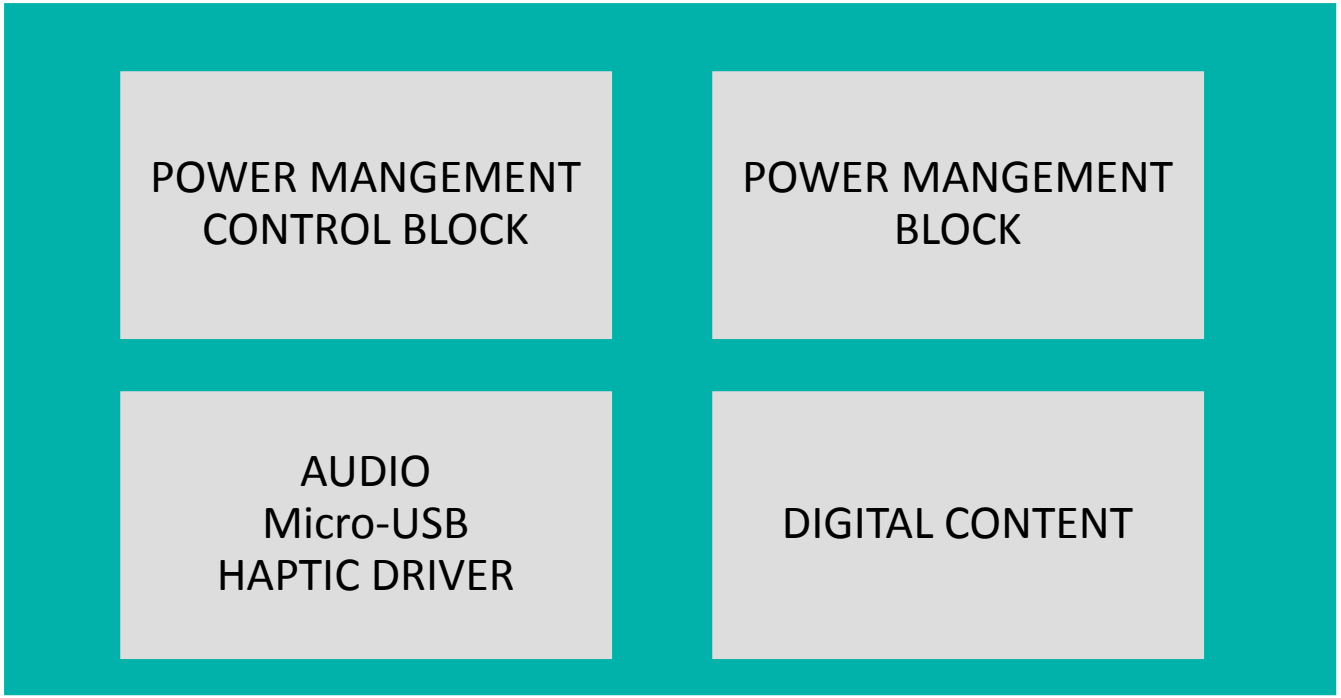
Outline

- Application Overview
- Technology Node impact
- Device level innovation
- Summary

PMIC – building blocks

- Power management ICs are used to manage the accurate power flow in portable and handheld devices
- Power Management block is the biggest size hog on the IC and requires the most aggressive techniques to improve as we move ahead



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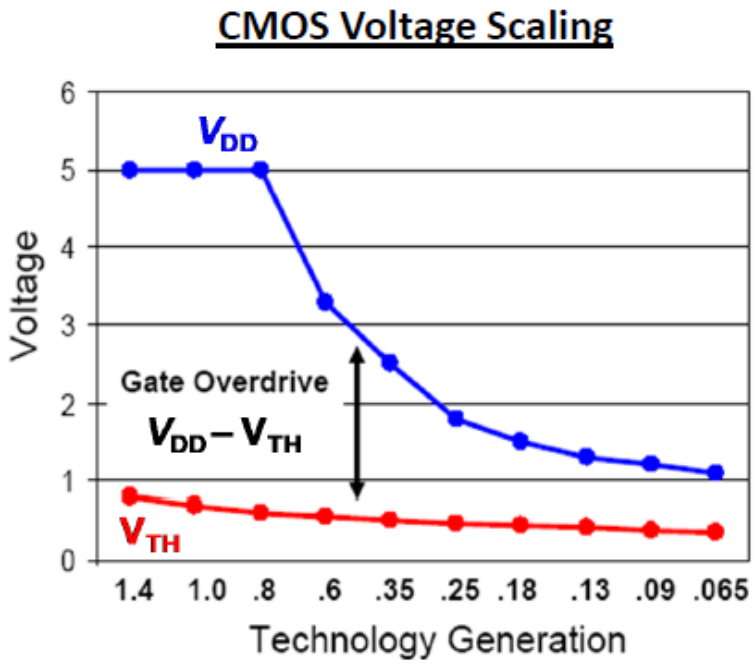
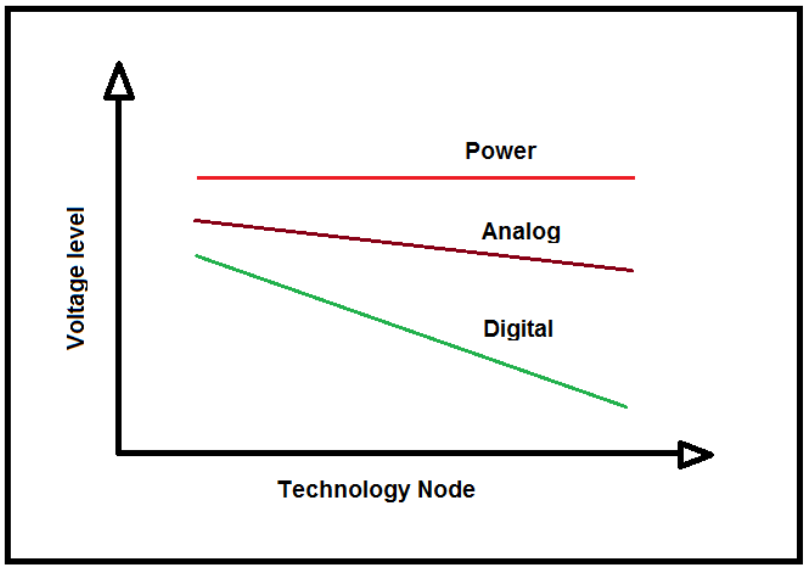
Impact of technology node

- Digital footprint has seen a significant reduction as smaller technology node has a significant impact on individual transistor size
- A big factor which enables such a transition is the scaling of supply voltage which does not hold true of Power transistors



Source: P. Packan (Intel),
2007 IEDM Short Course



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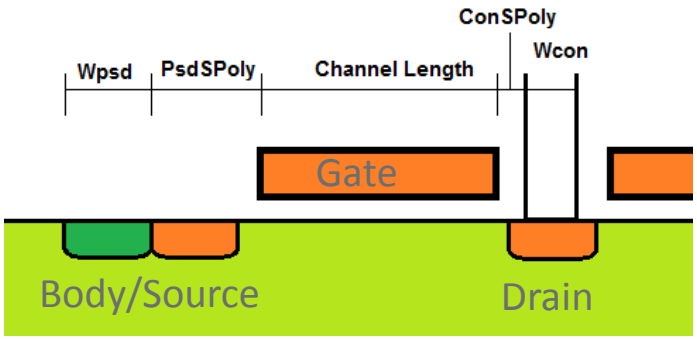
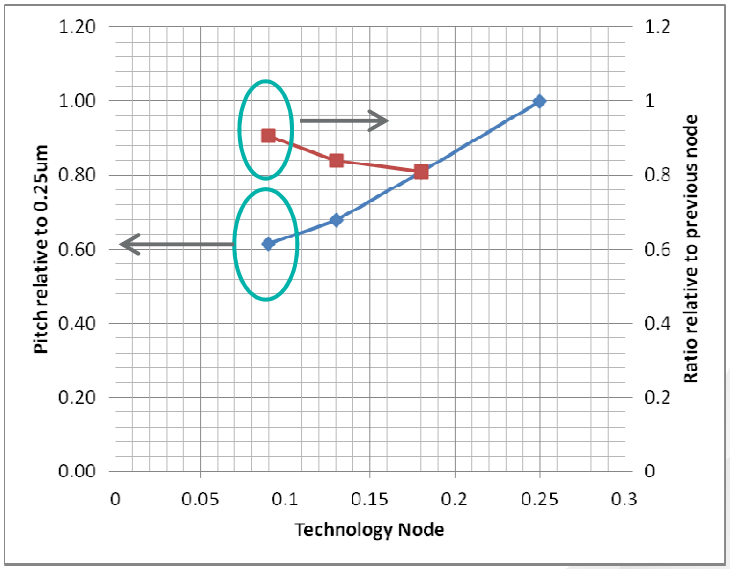
Comparison across technology node - PowerFET

- Taking the example of a standard 5V symmetric MOSFET over multiple technology, the pitch of the device does shrink with smaller technology node
- The minimum channel length does not shrink along with technology as the voltage requirement is fixed and reduction is a by product of other design rules
- There is something to be gained by transitioning to smaller technology nodes for consumer technologies which are utilize such FETs very extensively





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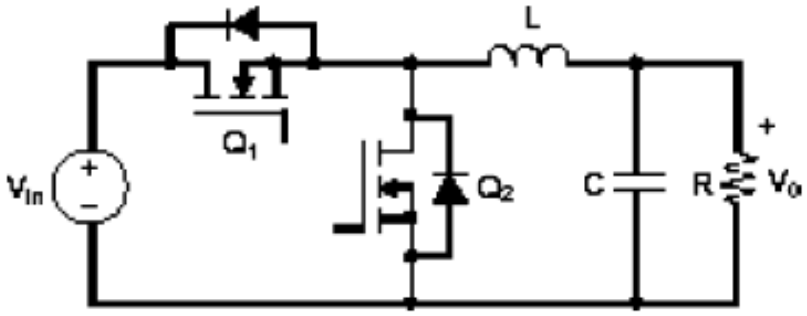
Power Loss of MOSFETs

Synchronous Buck Converter



Power loss for Control FET Q1:

$$P_{Q1}=P_{COND}+P_{SW}+P_{GD}+P_{OSS}$$

$$P_{COND}=I_{rms}^{2}R_{DS(ON)}$$

$$P_{SW}=\frac{I_O}{I_G}Vin(Q_{gs}/_2+Q_{gd})f_s$$

$$P_{GD}=Q_gV_gf_s$$

$$P_{OSS}=\frac{1}{2}V_{in}Q_{OSS}f_s$$

Power loss for Synchronous FET Q2:

$$P_{Q2}=P_{COND}+P_{GD}+P_{OSS}+P_{Qrr}$$

$$P_{COND}=I_{rms}^{2}R_{DS(ON)}$$

$$P_{GD}=Q_gV_gf_s$$

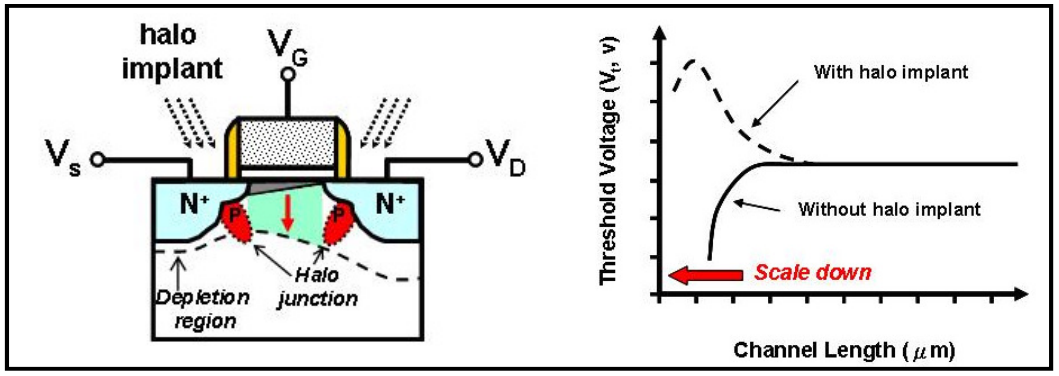
$$P_{OSS}=\frac{1}{2}V_{in}Q_{OSS}f_s$$

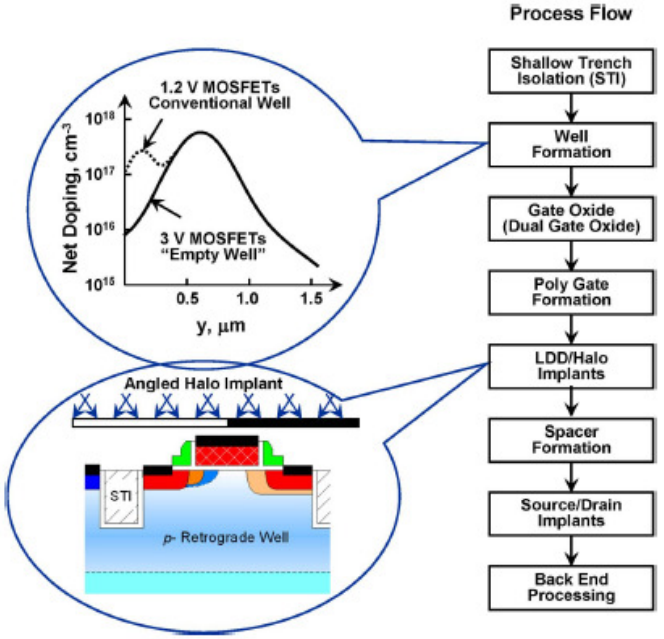
$$P_{Qrr}=V_{in}Q_{rr}f_s$$

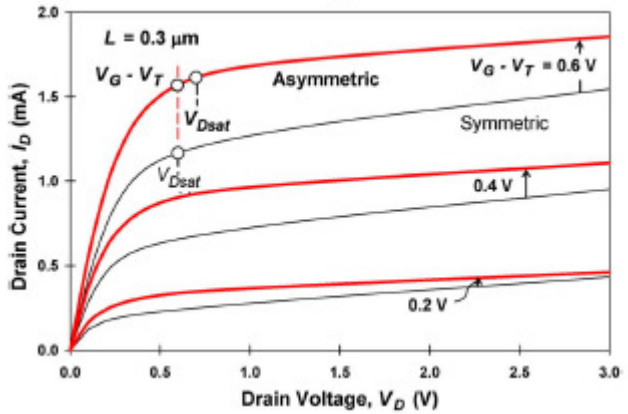
- ►R_{on} dominates total power loss at low frequencies
- ►Q_g begins to dominates total power loss at high frequencies such as multi-megahertz
- ►FOM=R_{on} × Q_g can be a simple indicator of converter efficiency
- ►Both R_{on} and Q_g need to be minimized to achieve maximum efficiency

Innovative structures for improved performance

- Moving to smaller technology nodes (0.18um and below) also brings with it some additional implants which are required for CMOS devices
- Such additional layers are viewed as a hindrance to migration to smaller nodes, but it also opens the door to innovative device designs
- One such asymmetric MOSFET developed is shown on right which utilizes Halo implants normally reserved for CMOS devices



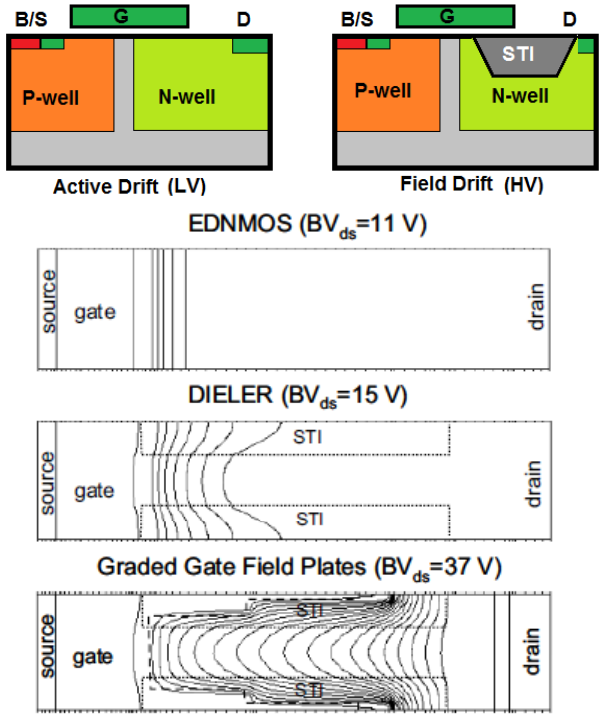


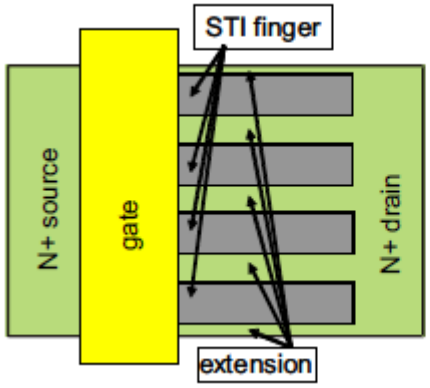


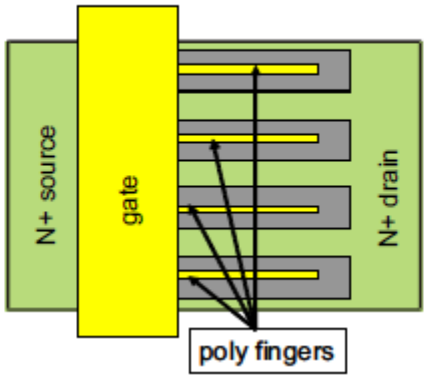
"Physics, Technology, and Modeling of Complementary Asymmetric MOSFETs" IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 57, NO. 10 OCTOBER 2010

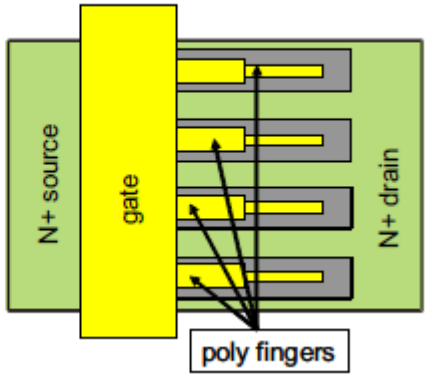
Utilizing small feature sizes – 90/65nm

- This novel structure details the path forward for PowerFET design in future BCD technologies
- The structure where active drift region is sandwiched between Shallow trench isolation (STI) islands is shown to achieve more than 35V breakdown without any added processing steps
- This structure can only be built in 90nm technology or below which allow small active-active spacing





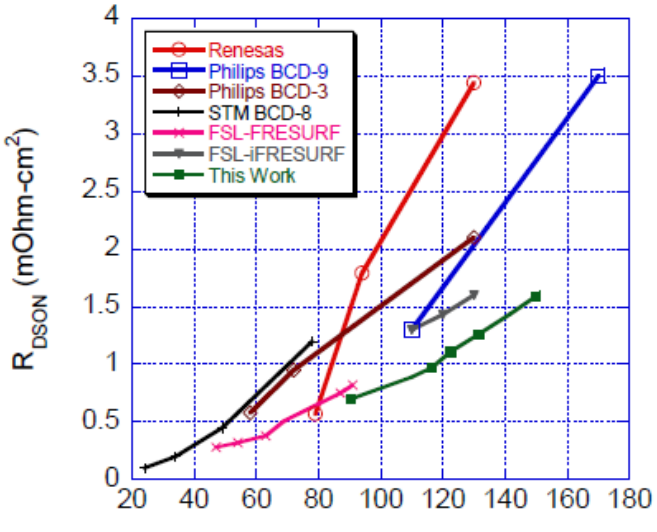


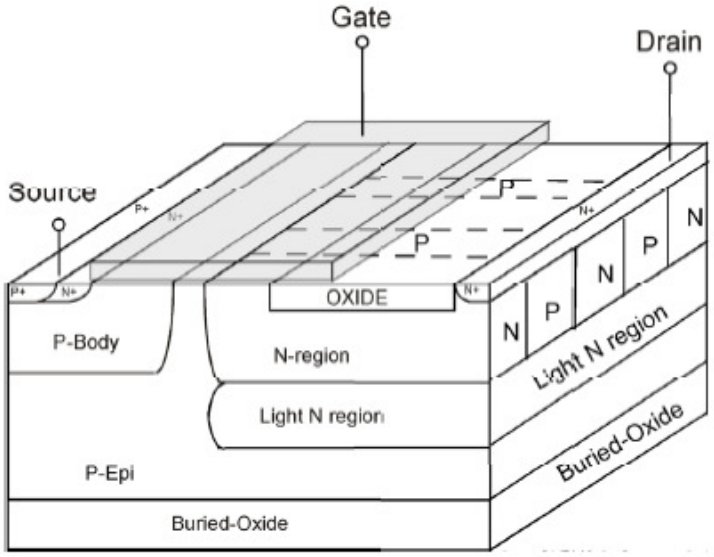


"Innovative lateral field plates by gate fingers on STI regions in deep submicron CMOS " Proceedings of the 20th International Symposium on Power Semiconductor Devices & IC's

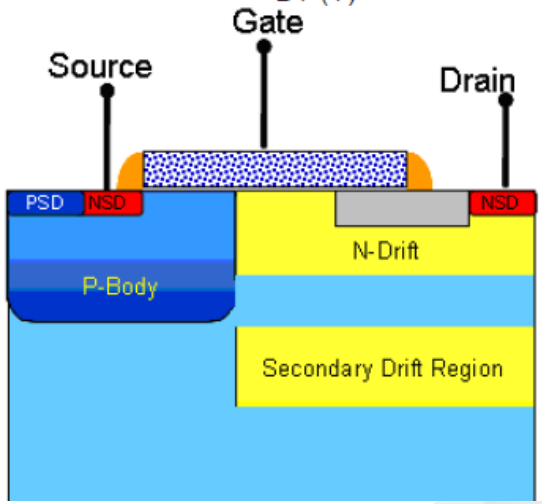
Structural Innovation for HV LDMOS

- For higher voltage devices, the on-resistance is drift-region dominated and there is lesser impact of smaller dimensions
- Above 50V, we enter a regime where novel structures such as Super-junction LDMOS can be explored, which require tighter misalignment control in lateral structures





Superjunction LDMOS

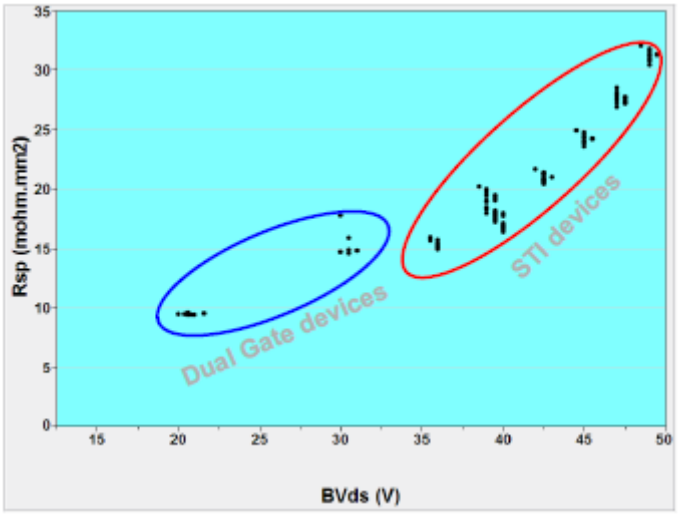


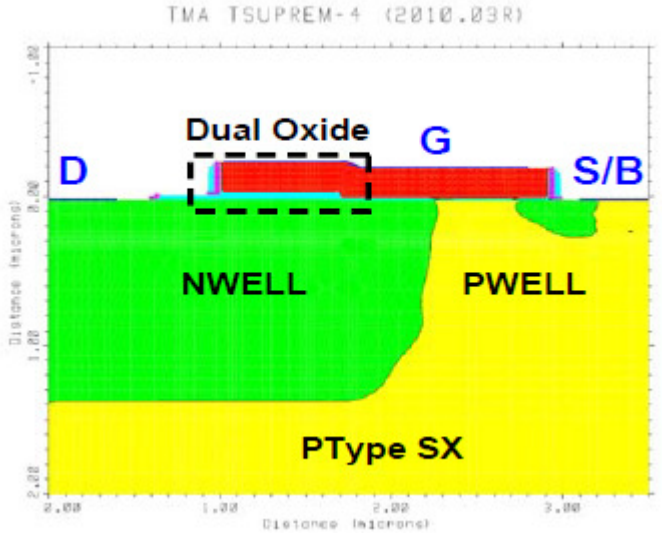
CLAVER LDMOS

"Combined Lateral Vertical RESURF (CLAVER) LDMOS structure" International Symposium on Power Semiconductor Devices & IC's, 2009
" A High Voltage Super-Junction NLDMOS Device Implemented in 0.13µm SOI Based Smart Power IC Technology " 2010

Structural improvement in Qg

- Several structures have been developed to minimize Qg (especially Qgd) in LDMOS design to reduce switching losses
- For field-drift LDMOS devices, the solutions range from floating field plates to utilizing source field plate to minimize gate poly area
- For active drift devices, specifically LV FETs, stepped gate structure is an attractive candidate to minimize capacitance



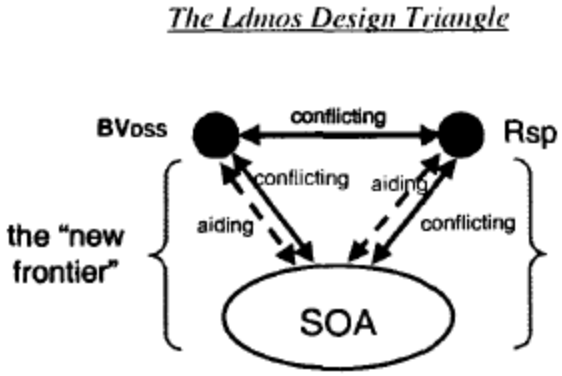


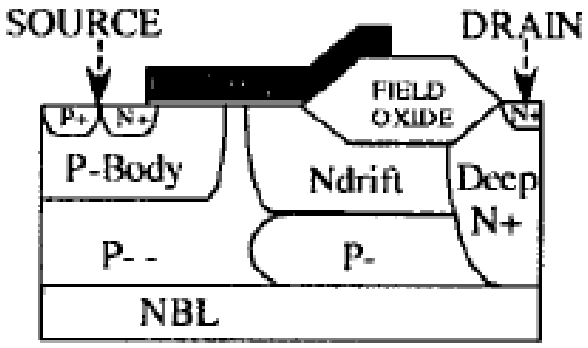
Stepped gate structure

"Planar Dual Gate Oxide LDMOS Structures in 180nm Power Management Technology" International Symposium on Power Semiconductor Devices and Ics 2012

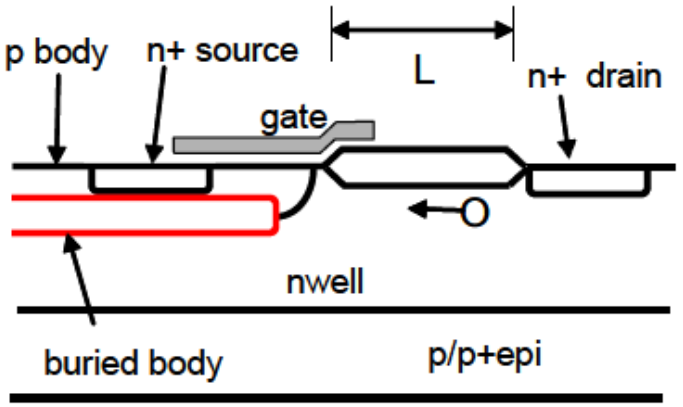
Safe Operating Area of LDMOS devices

- Efficient switching and robustness are key requirements of LDMOS devices integrated into BCD technologies
- To improve robustness of LDMOS devices, key feature is to degrade the parasitic bipolar which exists in parallel to the PowerFET
- The standard approach is to opt for a heavily doped body to reduce the base resistance and delay the triggering of this bipolar
- Another approach is drain side engineering to reduce Kirk-effect related SOA degradation





Drain-side engineering



Source-side engineering

ISPSD 2002 (Motorola) ISPSD 2005 (Texas Instruments)

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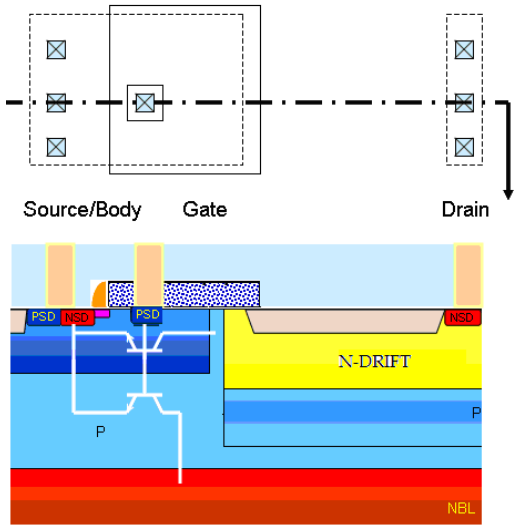
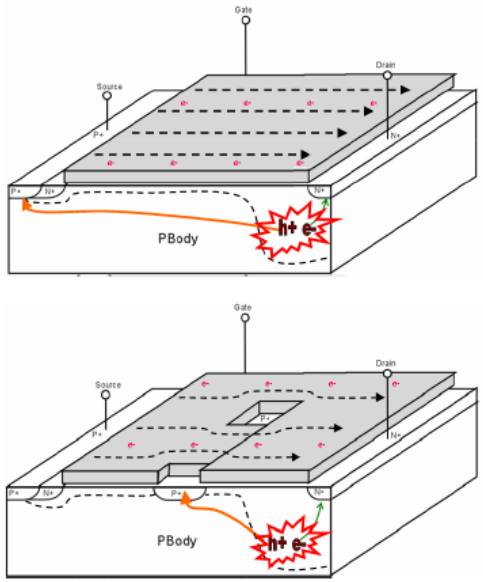
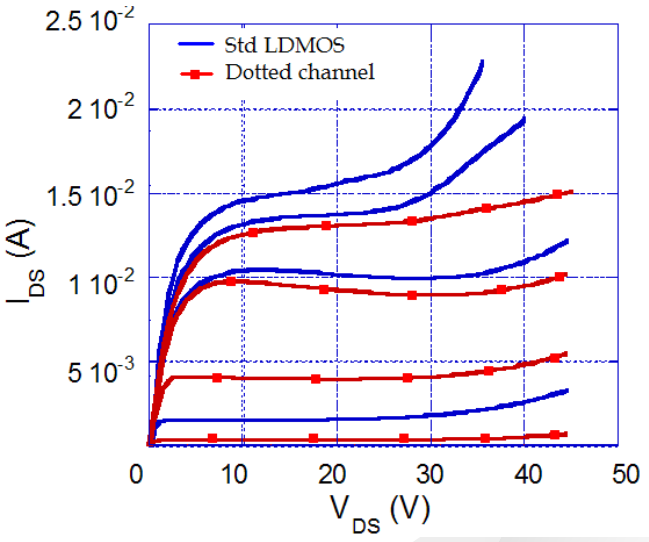
SOA improvement for next generation

- To minimize additional processing steps to improve SOA of LDMOS devices, such as buried body implant, structural solution can be utilized to the same effect
- The dotted channel structure becomes an attractive candidate as we go to a smaller technology node with smaller contact size and design rules







Dotted channel length structure

"Rugged Dotted-channel LDMOS structure" International Electron Devices Meeting 2008

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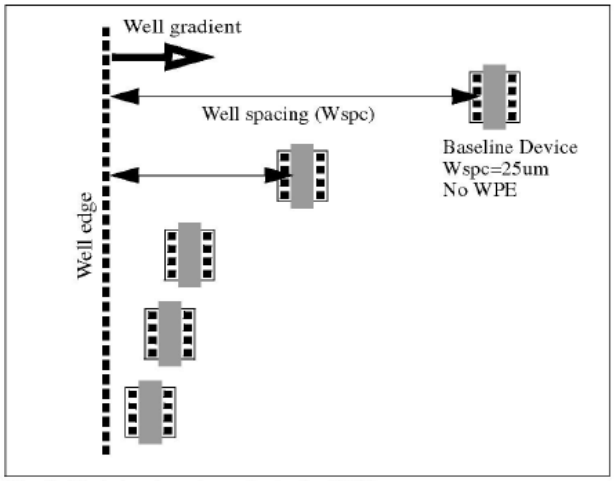
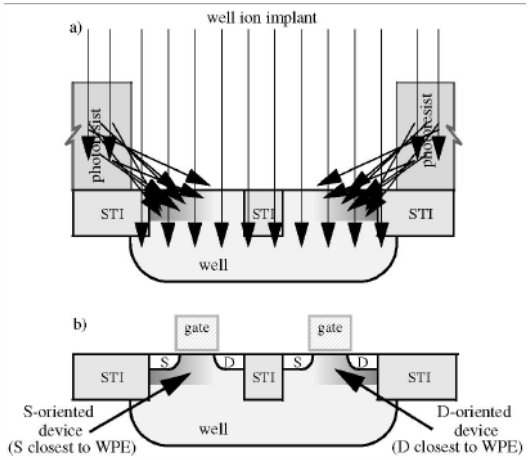
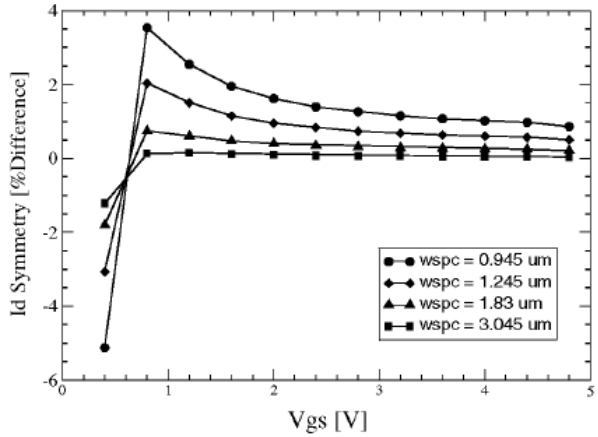
Integration Issues – Well Proximity Effect

- With significant space being utilized by analog FETs, merging of devices is of great importance to achieve significant footprint reduction
- Reduced well enclosures work well for digital CMOS devices but cannot be used as-is for analog application due to well enclosure effects

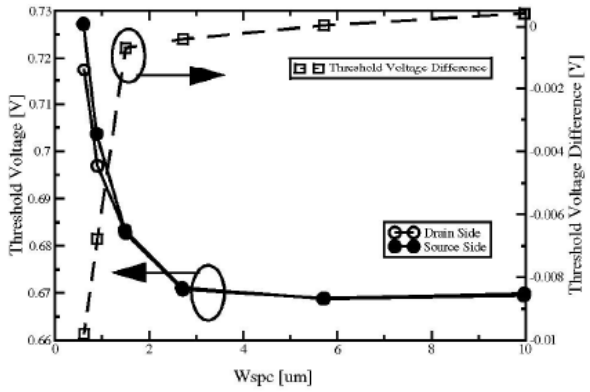


Test structure to evaluate the WPE.





S/D Id asymmetry for a W/L=24um/1.2um 3.3V nMOS device on a 0.13um technology in the saturated region (Vds=3.3V)



IEEE CICC 2006, Freescale Semi

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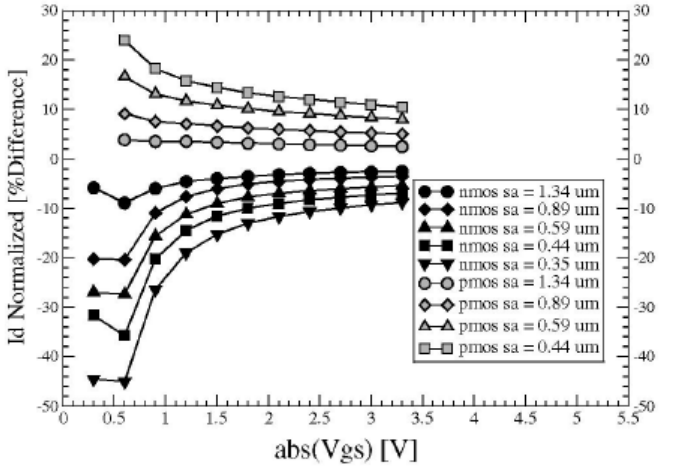
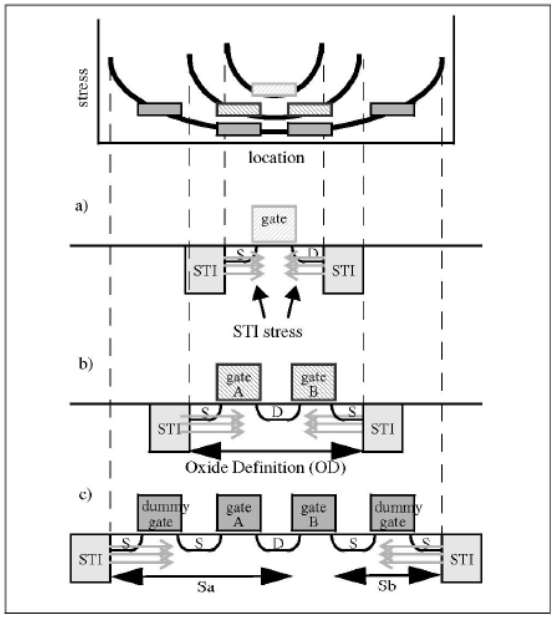
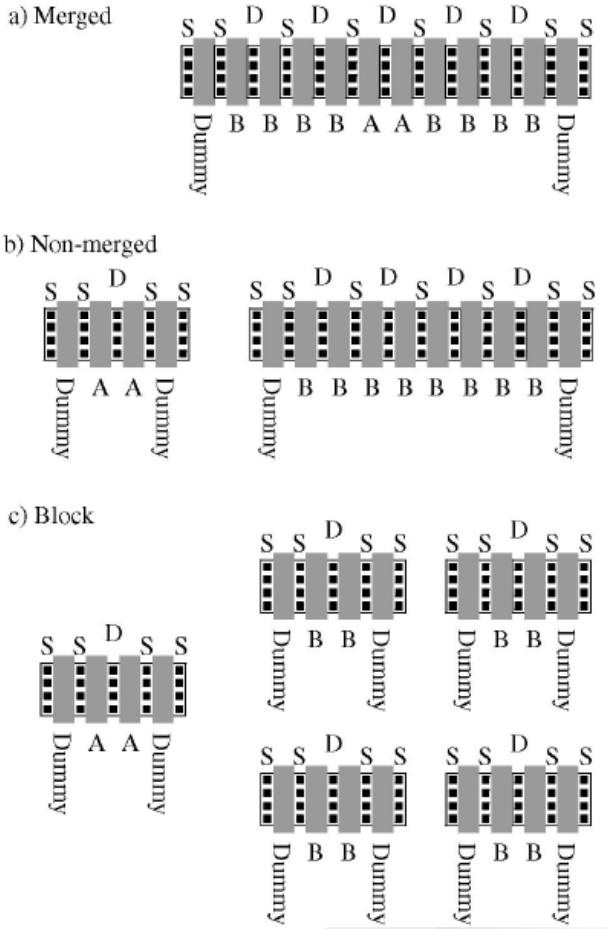
Integration Issues – STI proximity effect

- Another drawback of deep submicron technologies with STI defined active under non-uniform stress
- STI induces stress has shown to affect both V_T and $I_{D,sat}$ of MOSFETs and special care must be taken for matched pairs with multiple schemes possible



The impact of STI stress on normalized drain current for W/L=24um/0.6um 3.3V nMOS and pMOS devices in a 0.13um technology. Sa=Sb in all curves.





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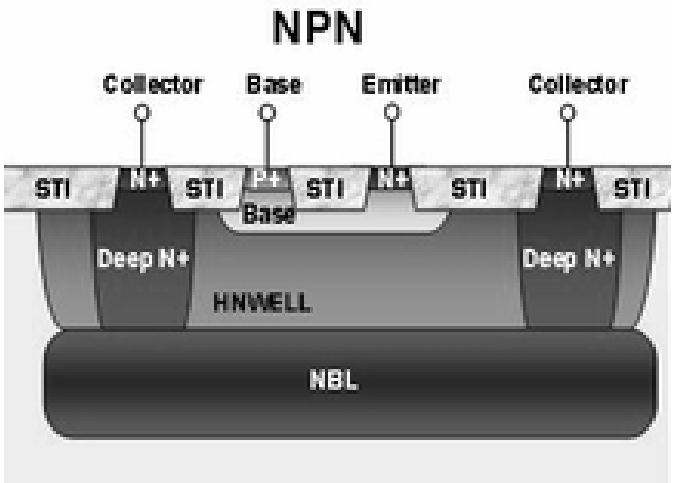
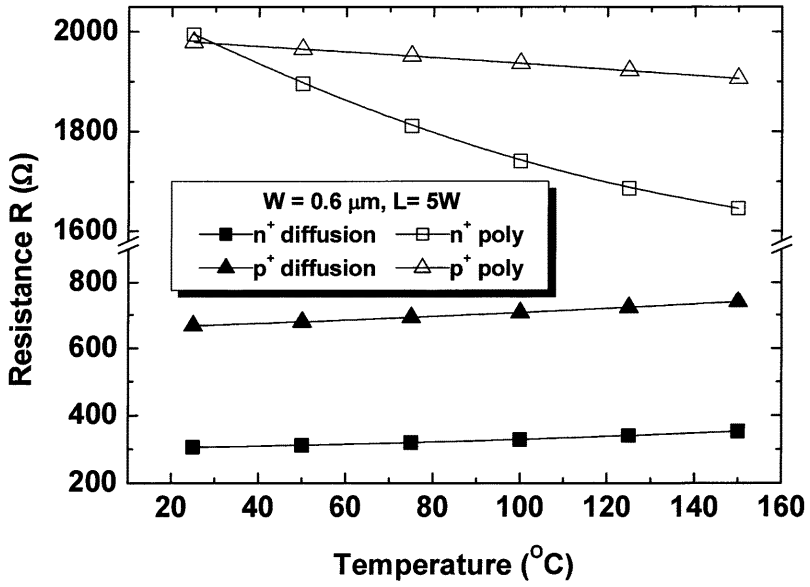
Other components - Bipolars

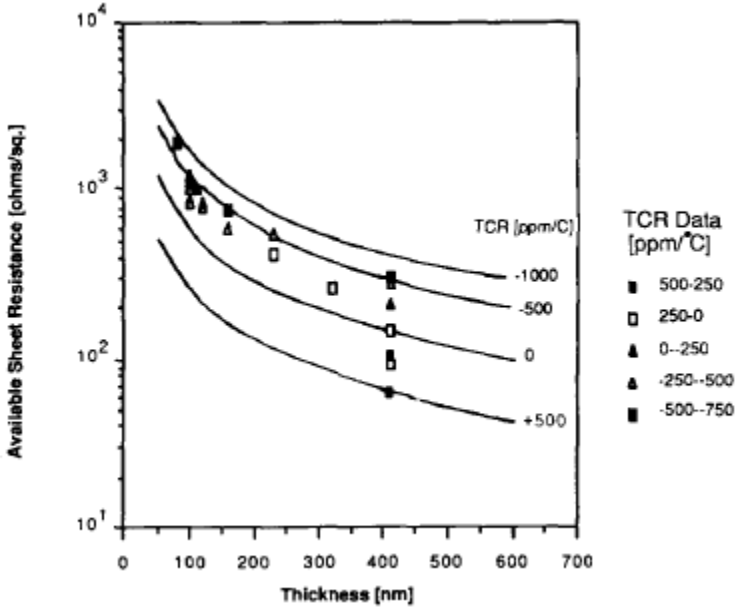
- Bipolar transistors are still heavily used in precision analog circuits where matching between pairs is of critical importance
- The devices are usually built out of available processing steps and are parasitic structures with no dedicated processing steps
- Gain of bipolars is crucial from application perspective with most of the latest technologies providing numbers ranging from 50-100



Other components - Resistors

- Resistors are very heavily utilized in analog and power circuits
- High sheet-rho, low temperature coefficient (T.C.) and good matching are key design parametric for these components
- Diffused well resistors are used for good matching applications while poly resistors are good for zero T.C. design





IEEE TED 2003 (NCK Univ Taiwan),

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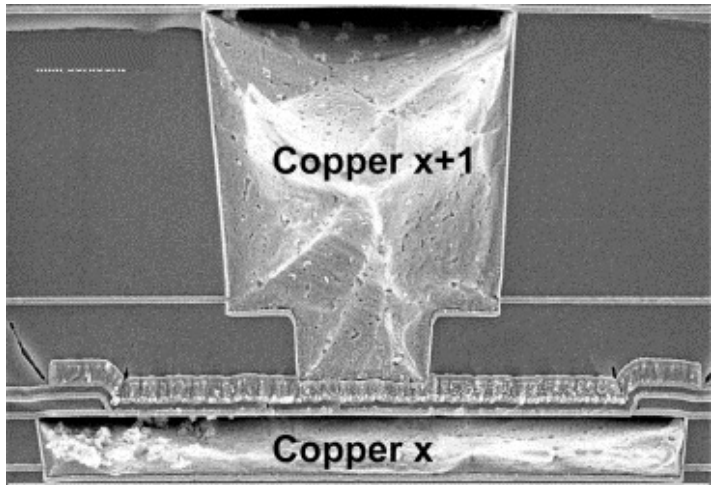
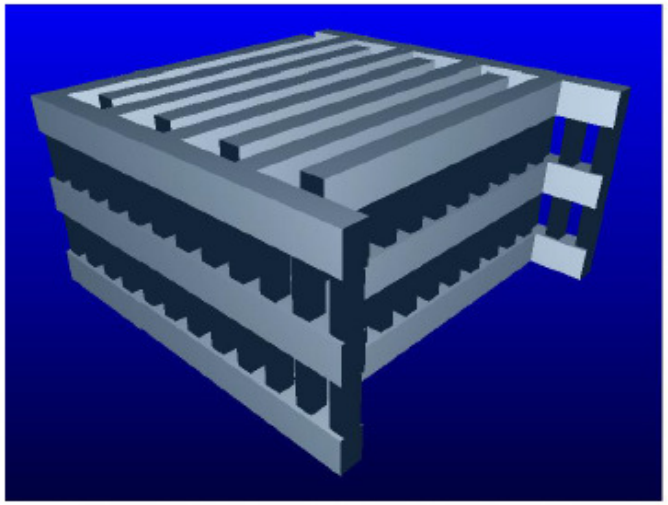
Other components - Capacitors

- Capacitors can occupy significant footprint on PMICs and multiple options are offered in technologies depending on trade-off vs. added cost
- Good linearity MIM caps have superior performance (density, voltage coefficient) vs. other options but they come with additional cost of dedicated processing steps
- One inexpensive alternative is the MOM cap which has lower density but is free of cost. The density is improving with each technology node with density approaching 1fF/um^2 in latest technology node (90nm)



MIM cap



Schematic 3-D view of 25V interdigitated MOM capacitor

The path forward

- With innovations in technology, significant reduction has been achieved for die footprint. Going to a smaller technology node can be justified with an increase in digital content on-chip which has the most significant impact of such a move
- A large chunk of area is now occupied by external passives where higher switching freq & on-die integration will make a much more significant impact
- Shrink in analog/power blocks is always challenging but with innovative structures (e.g. zero channel length, DIELER), additional cost of processing steps can be offset with improved performance