High-frequency LDMOS in 0.18um BCD Technology for Power Supply-On-Chip

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Introduction

• DC/DC converter market requires high efficiency and high current driving capability

• Power SOC (Supply-On-Chip) requires
  • high efficiency and fast switching DC/DC converter
  • integrated passives (inductor)

• Fast switching DC/DC converter allows to reduce inductor size and increase the power density per unit volume
Introduction

• High frequency LDMOS achieves
  • low parasitic capacitance
  • fast switching speed realizing low switching power dissipation
  • DC power dissipation might higher than conventional low Rsp LDMOS

• Dongbu HiTek developed high frequency LDMOS with thin gate oxide, short gate length, high breakdown voltage in 0.18um Analog CMOS/BCD technology
Monolithic DC/DC Converter (2002, ETRI)

0.8μm CMOS + DE(Drain-Extended)CMOS Process

Waveforms of FET switching voltage and thin-film inductor current when \( V_i = 3.5 \) V, \( V_o = 6.0 \) V, and the operating frequency was 8 MHz.

Micro inductor: 0.5 ~ 0.6 uH
Magnetic Material; NiFe (2.5μm)

Power Efficiency: 72%
AN180 Process

- Process Modularity
  - To save development time for the process and optimize the mask layer
  - Use 1 process platform and provide several process options
  - Process modularity is the Key feature

* Currently BD180LV (non-epi) version merged into AN180

<0.18um modular technology platform for power management application>
AN180 Process

- **Process Modularity**
  - 5V CMOS baseline
  - HVCMOS and iso CMOS
  - 1.8V CMOS option
  - HSR, MIM option
  - Thick Cu option
  - Mod-density EEPROM
  - High-density EEPROM
  - **High Frequency LDMOS**
    (additional implants)

Process modularity of 0.18um 30V AN180 process
Process Features

- 4 additional implant masks for HF-LDMOS;
  - 2 mask for NLDMOS
  - 2 mask for PLDMOS
  - No additional thermal budget → fully compatible with existing AN180 process
- For fast switching
  - 30Å thin gate oxide for Vgs power scaling
  - 0.26µm channel length
  - Drift implant after gate formation for small gate-to-drain overlap capacitance
- High driving current capability
  - Short channel length even at high drain voltage without punch-through
  - Optimized halo implant at source side
Process Flow

- STI Module
- CMOS Well Formation w/ deep-NWELL
- GATE Module
- N-LDD Module
  - P-Body & N-Drift for NLDMOS LSD/HSD
  - P-LDD Module
    - N-Body & P-Drift for PLDMOS
    - N+SD/P+SD Module
      - Salicide Blocking
      - BEOL Module

Additional implants for HF-LDMOS module
Device Structure

• Dedicated Implant Layers are used
  • 2 layers for P-Body and N-Drift of NLDMOS
  • 2 layers for N-Body and P-Drift of PLDMOS
• PWELL/NWELL extension
  • For the RESURF action, WELL is extended to the middle of drift region
Device Structure

- Single-sided high tilt implant
  - To prevent punch-through breakdown even at high voltage of 20V
  - Source region width is limited by shadowing effect
- Optimized 2-step drift implant
  - At surface region of N-Drift for better HCI immunity
## Summary of Electrical Performance

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
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<tbody>
<tr>
<td></td>
<td>12V nLD LSD</td>
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<tr>
<td>$L_{CH}$</td>
<td>$\mu$m</td>
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<tr>
<td>$V_T$</td>
<td>V</td>
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<td>$I_{D,SAT}$</td>
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<td>$BV_{DSS}$</td>
<td>V</td>
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<td>$R_{SP}$</td>
<td>m$\Omega\cdot \text{mm}^2$</td>
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<td>p$A/\mu m$</td>
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<tr>
<td>$C_{ISS}$</td>
<td>fF/\mu m</td>
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<tr>
<td>$F_{T,MAX}$</td>
<td>GHz</td>
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<tr>
<td>$F_{MAX}$</td>
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12V HF-LDMOS I-V Characteristics

<DC output characteristics at Vgs=0.6V, 1.2V and 1.8V>

- Stable I-V characteristics up to 14V of Vds at 1.8V of Vgs
  - On-state BV: 18.5V, Off-state BV: 20V
- Current capability
  - NLDMOS $I_{dsat} = 500 \mu A/\mu m$ at $V_{gs}=1.8V$ and $V_{ds}=12V$
  - PLDMOS $I_{dsat} = 200 \mu A/\mu m$ at $V_{gs}=-1.8V$ and $V_{ds}=-12V$
12V HF-LDMOS – BVdss & Ft

- Over 20V off-state breakdown voltage with low leakage
- Ft and Fmax characteristics according to Vgs at Vds=6V
  - Ft,max/Fmax = 37.2GHz/66.9GHz for 12V RF NLDMOS LSD
  - Ft,max/Fmax = 12.9GHz/38.4GHz for 12V RF PLDMOS
12V HF-LDMOS – Reliability (HCI)

- Wide electrical SOA enough for operation up to 15V of $V_{ds}$
- Long-term HCI results:
  - $I_{dlin}$ drift 6.7% after 150Ksec stress at $V_{ds}=12V$ and $V_{gs}=1.8V$

<TLP I-V characteristics; pulse width=100ns>  <Long-term HCI test at $V_{ds}=12V$, $V_{gs}=1.8V$>
12V HF-LDMOS – Reliability (HTRB)

- Negligible BV & Off-leakage shift with stress time during Hot Temperature Reverse Biasing stress test
- Customer: product level HTOL (up to 1500 hrs) qualified

<BVdss curve with stress time; stress condition 150°C, Vds=13.2V>
BV vs. Ft comparison

[BVdss vs. Ft](#)

<table>
<thead>
<tr>
<th>This Work</th>
<th>[1] Z. Lee et al., IEEE BCTM, pp.1-4, 2006</th>
</tr>
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</table>
Application – ENPIRIION DC/DC Converter

- Enpirion unveils the **EN2340QI** 4 Amp, **EN2360QI** 6 Amp, **EN2390QI** 9 Amp, and **EN23F0QI** 15 Amp devices further broaden Enpirion’s extensive PowerSoC (power-system-on-chip) portfolio by using **AN180 12V High Frequency LDMOS** and **integrated inductor**
- **EN2340QI** Measurement data (refer to datasheet)
Summary

• 12V HF-N/PLDMOS transistors with 1.8V Vgs have been developed and integrated on Dongbu HiTek 0.18µm Analog CMOS (AN180)/BCD(BD180LV) process
• Each of 2 additional implants are used to make NLDMOS and PLDMOS without adding thermal budget
• Short channel length(0.26um) and small gate-to-drain overlap capacitance are used to achieve high Ft, which can reduce the inductor size of the DC/DC converter system
• BVdss*Ft figure-of-merit
  • 744GHz*V for 12V RF NLDMOS
  • 258GHz*V for 12V RF PLDMOS
Summary (Cont.)

- Enpirion developed DC-DC converter using 12V HF-LDMOS process and integrated controller, power MOSFET, and integrated inductor into one chip realizing Power System-On-Chip (PowerSoC)
- The Enpirion shows high efficiency, highest density and reliability without compromising the performance
Thank You!

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