Fine Grain on-die Integrated Magnetics:

Breaking the power/performance barriers

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– Intel Corporation

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Agenda

- Introduction
- Evolution vs. Revolution
  - Industry trends
  - The CE device trends
- Practical Considerations
- The barriers…
- Summary

To know where your going,

you must know where you have been.

Breaking the power/performance barriers

- *Power is no longer the 'after thought' of system design*
- *The industry has to 'leap forward' to keep up*
- *Power is a customer exposed commodity*
- *Performance used to be how many amps can be delivered for a given cost.*
- *Performance is now how many amps can be delivered in a given size and how many rails can be integrated in that same area…*
  - *This is a major change in how we have been taught to consider power*
- *Power delivery and conversion is moving towards the silicon – not away from it – the two are merging.*

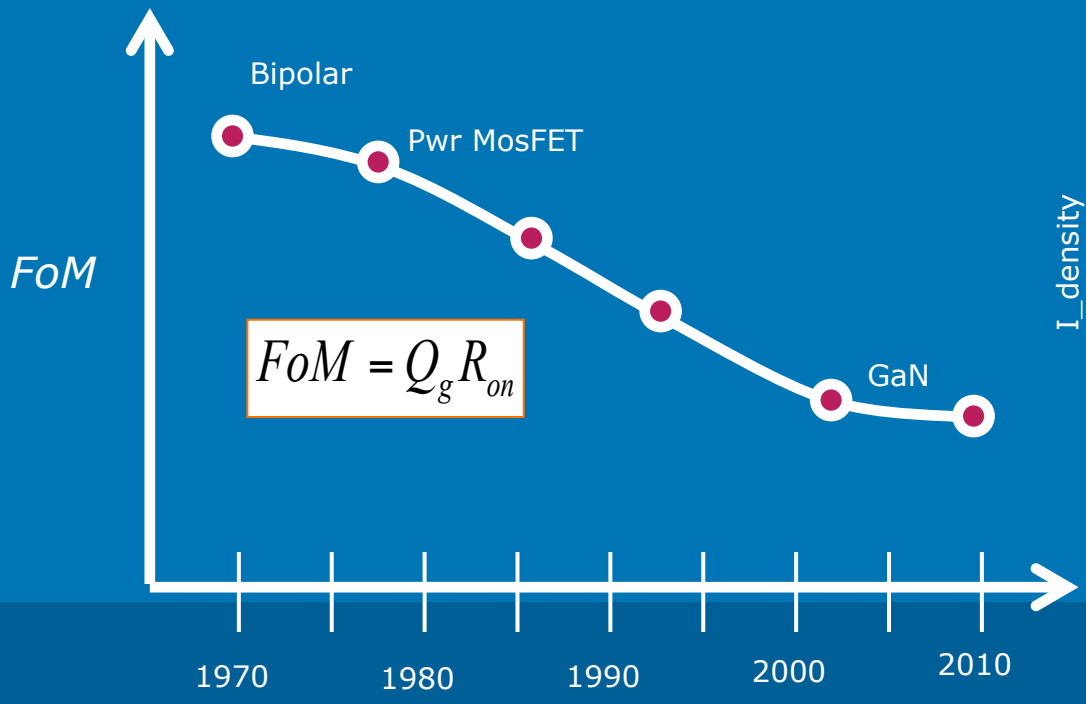
Evolution vs. Revolution

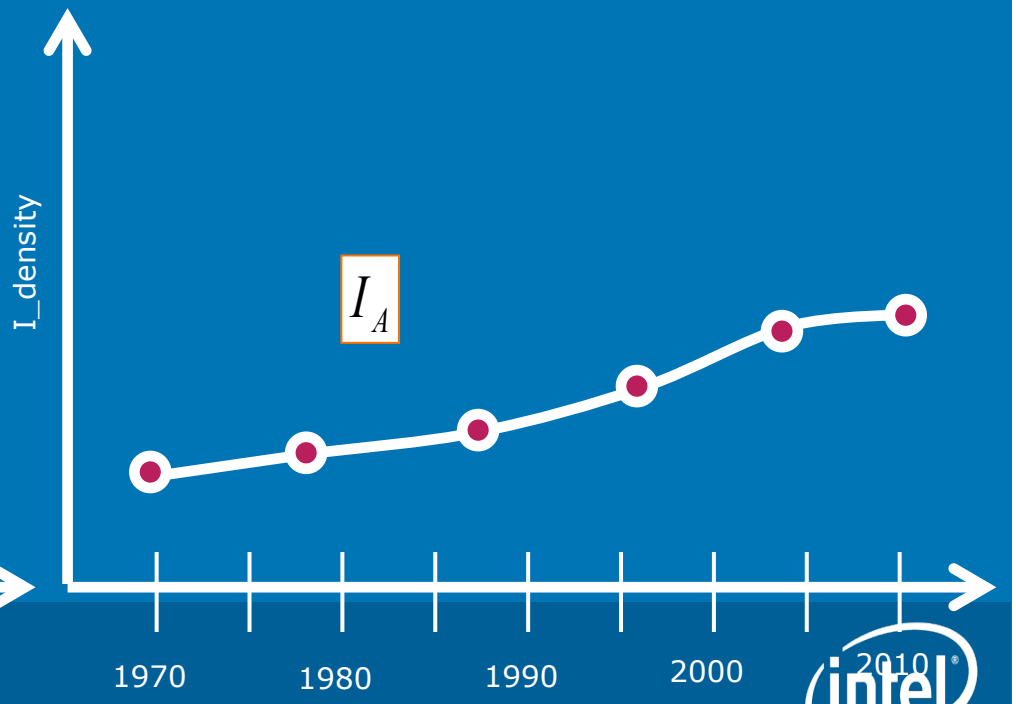
- The components of the power converter for computing devices have been on a generally incremental trend for the past 30 years at least - and though some integration has occurred, and materials have made great leaps, serious integration into silicon has been slow to come…
- The VR converter has been segmented into 4 basic areas
  - Power FET's and Controllers
  - Inductors
  - Capacitors
- And it has been this way for a long, long, time….

Industry Component Trends

- *Power Switch Trends from 70's to now*
- *Power FET current densities from 80's to now*

*References

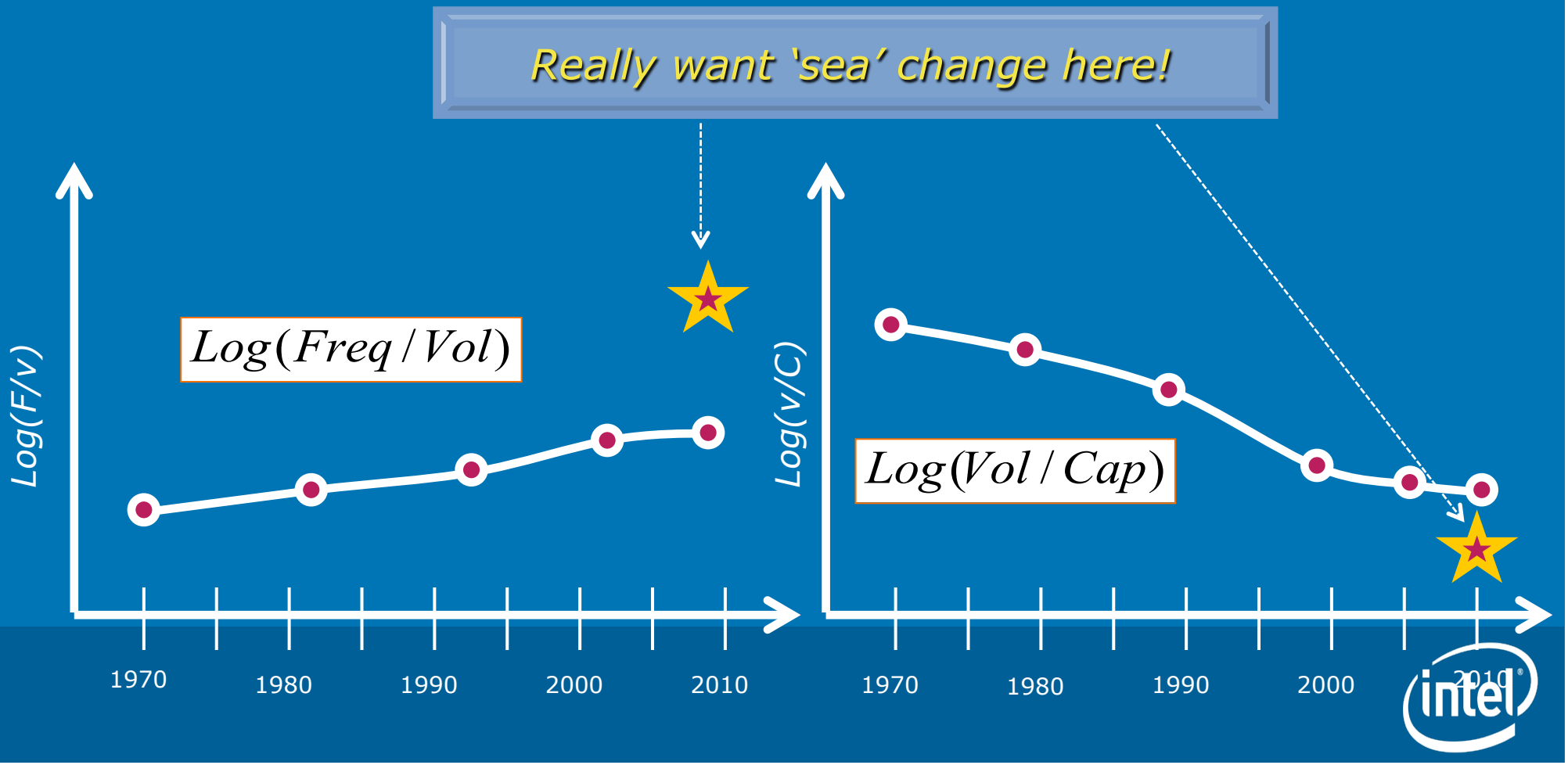




Industry Component Trends

- *Inductor frequencies and densities*
- *Capacitor size and density*

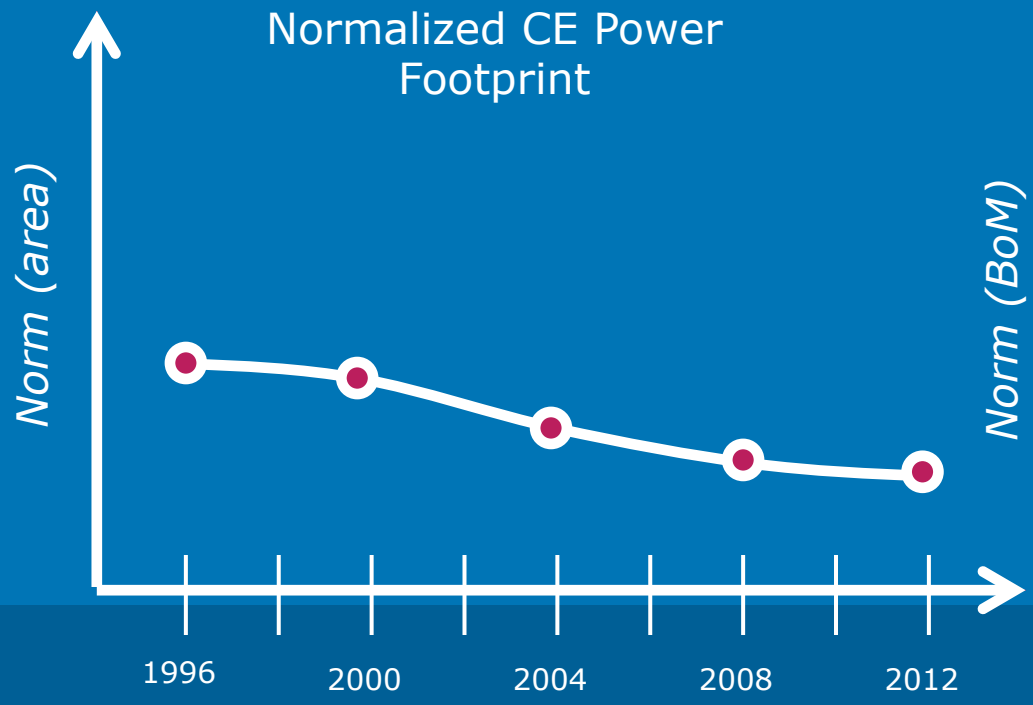
*References

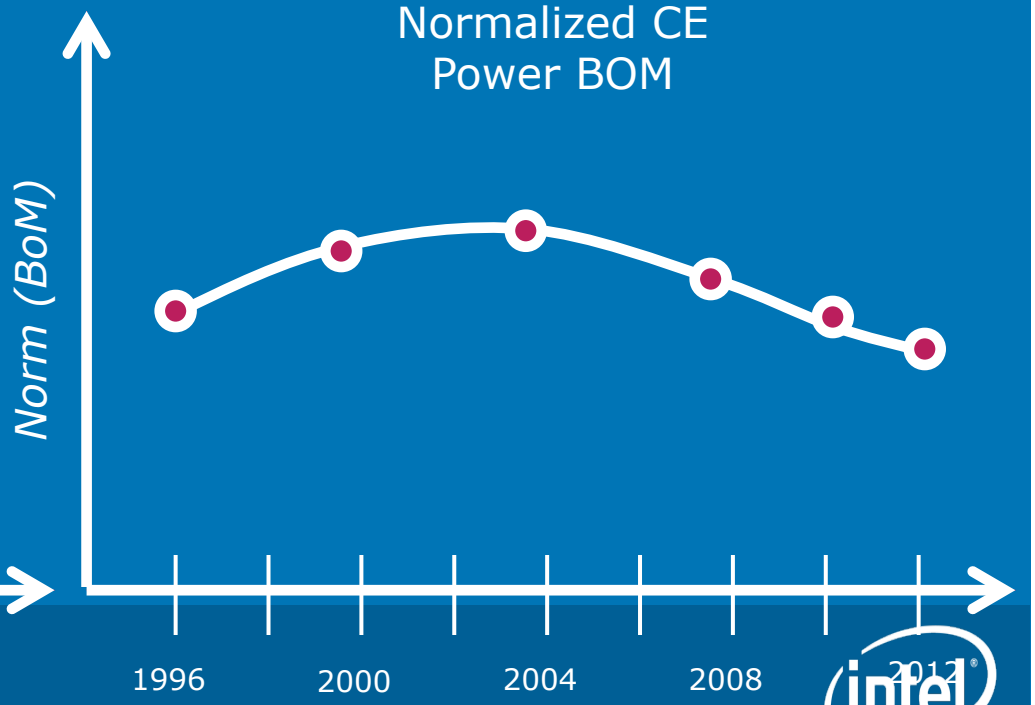


CE Platform Trends

- *Power Footprint (normalized)*
- *Power Components (average)*

*References

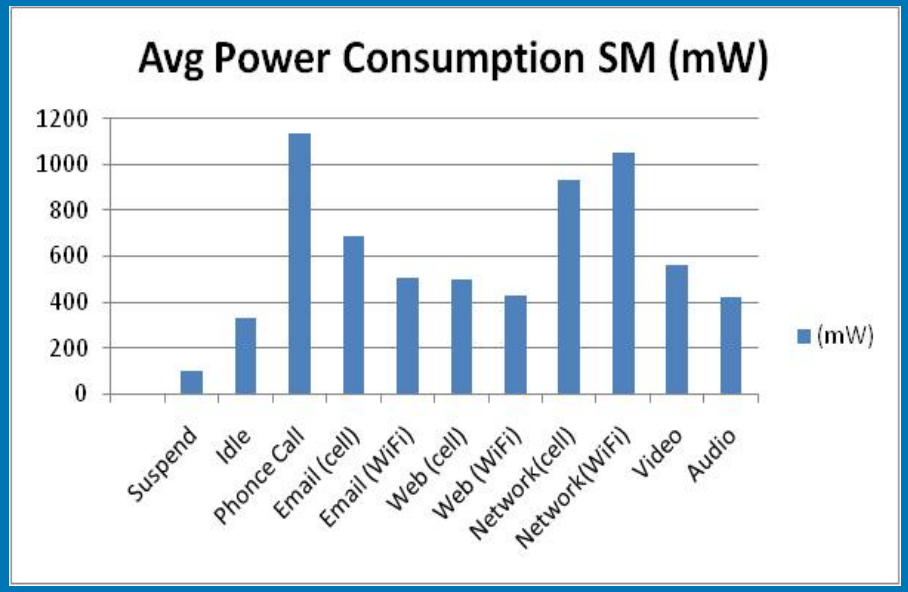




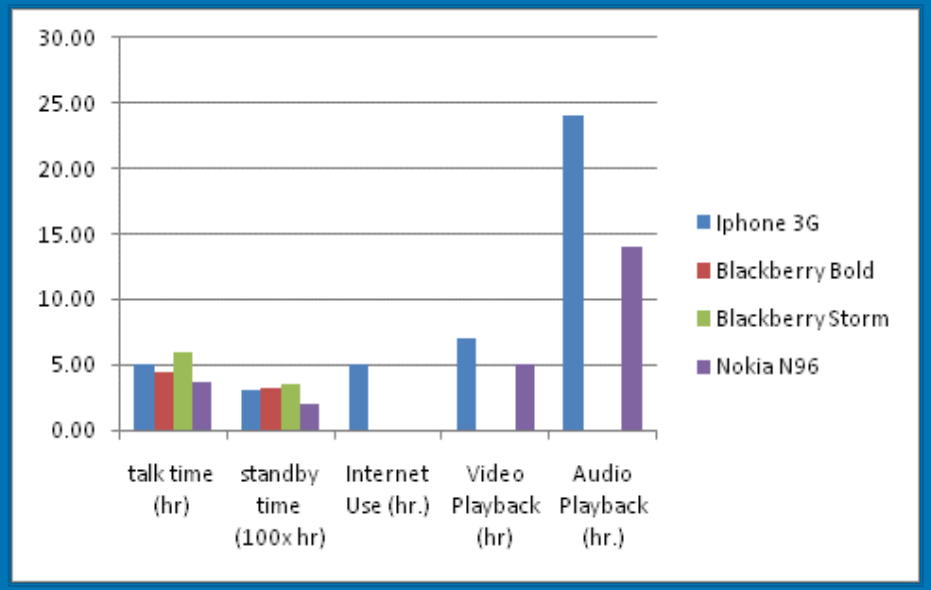
CE Platform Data/Trends

- *Workloads – power loss & time (examples).*

*References



Smartphone Power consumption



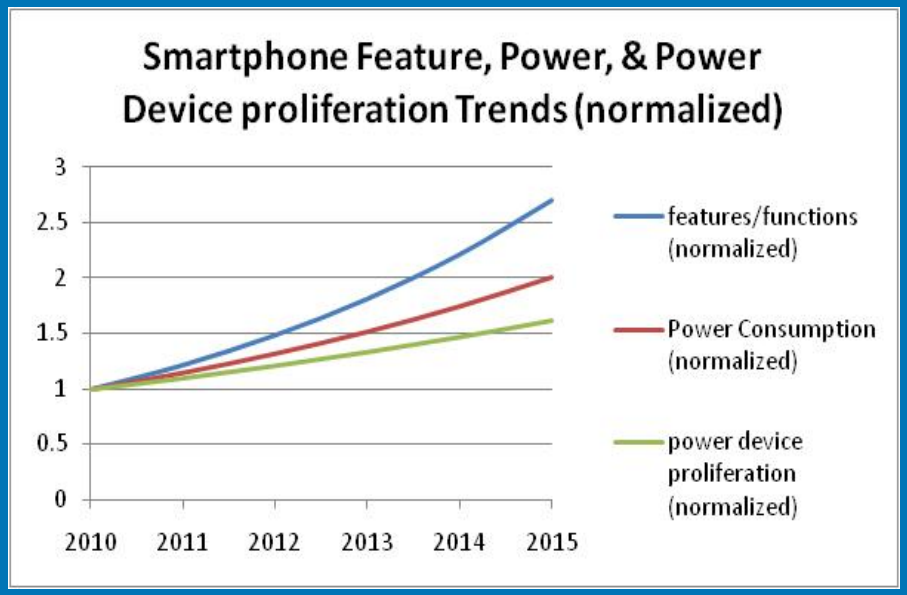
Smartphone data usages

Power usage spread over different devices.
And usage spread over different activities.

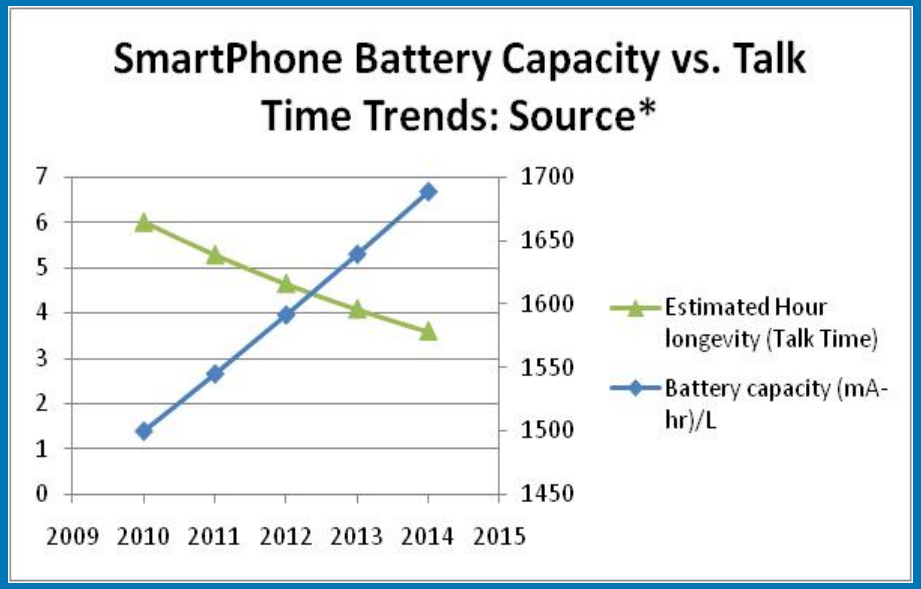
CE Platform Trends

- *Workloads – power loss & time. (*references)*

Features and Functions increasing.



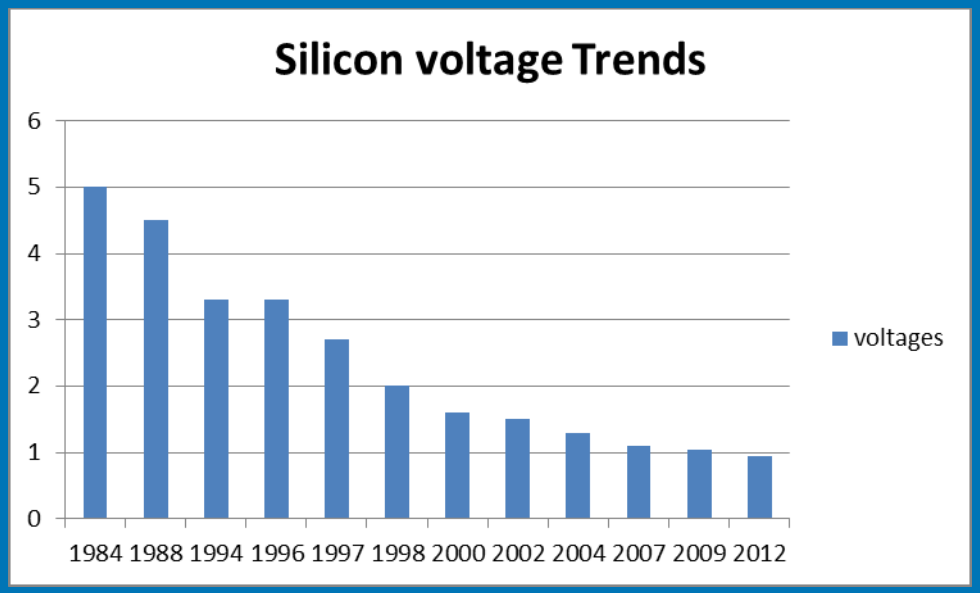
Smartphone data trends

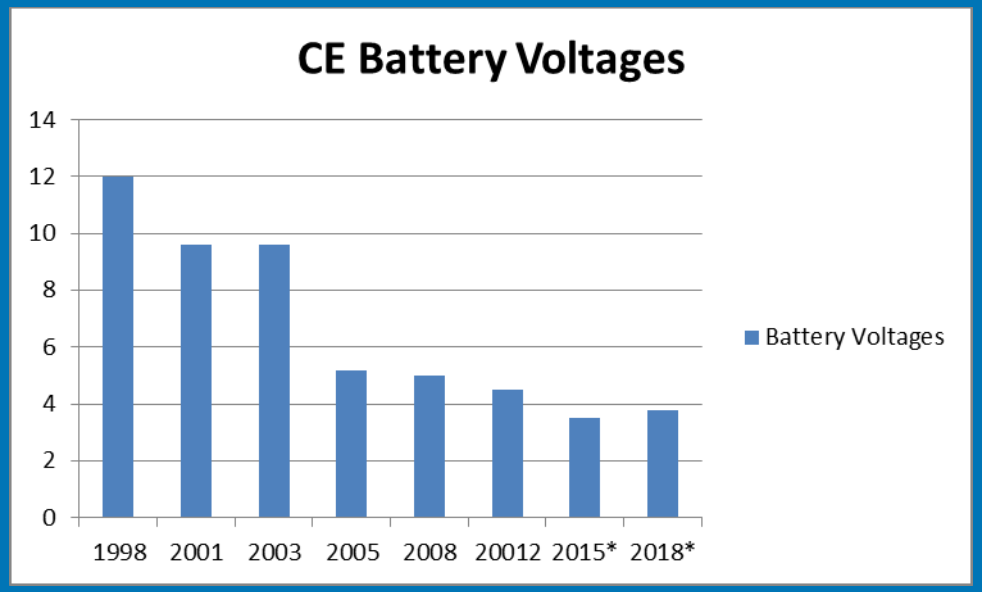


Talk Time Trends

CE Platform Trends

- *Silicon Voltage Trends**
- *Battery Voltage Trends* (*references)*





Trends indicate battery voltages starting to track silicon

So, what does this mean?

- Summing up the past few slides…
- We have questions now to ask here…

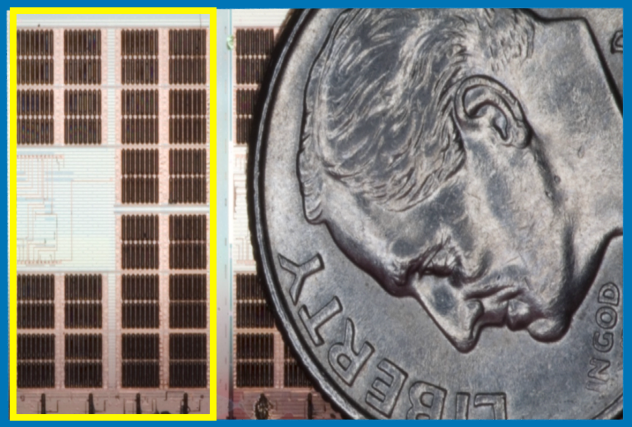
1. Is the industry trending towards a common monolithic power solution – for small consumer electronic devices?
   - Clearly, yes, we have seen this with PMIC's which have grown in popularity for many devices and are now seen in larger systems.
2. Do we see the need yet for consolidating power like we have seen in the past with other silicon devices? E.g. is the world ready for a device that combines both the silicon and the passive elements on a single device?

- We think the answer is yes.

What we need to overcome

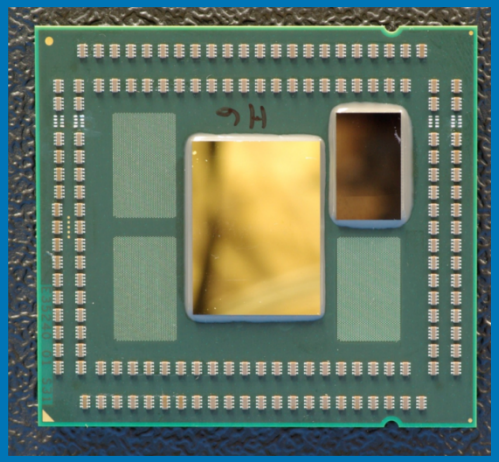
- *Three simple things*
- *Size, Cost, and performance*
- *Size – the solution needs to be at least as small as competing solutions – that is PMIC's and all the external components combined – it must also remove many of these components off the platform.*
- *Cost – it must be better than the existing solutions by a reasonable margin for people to adopt.*
- *Performance – it must be at least parity here and better in the lower power operating ranges since that is the trend.*

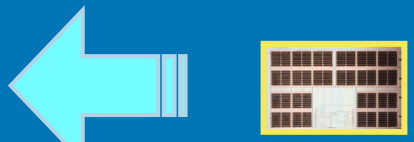
We are going to focus on power and performance here…

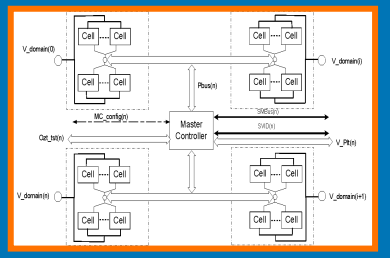


And leave the other metrics for a later discussion…

So, the barriers…







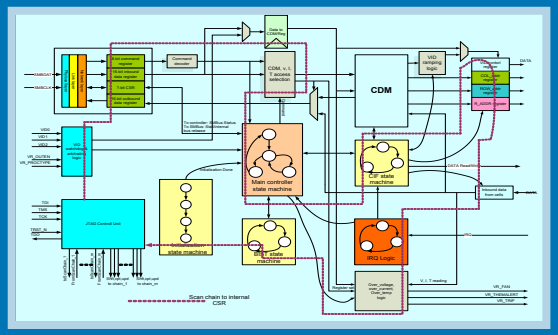
…what we need to overcome

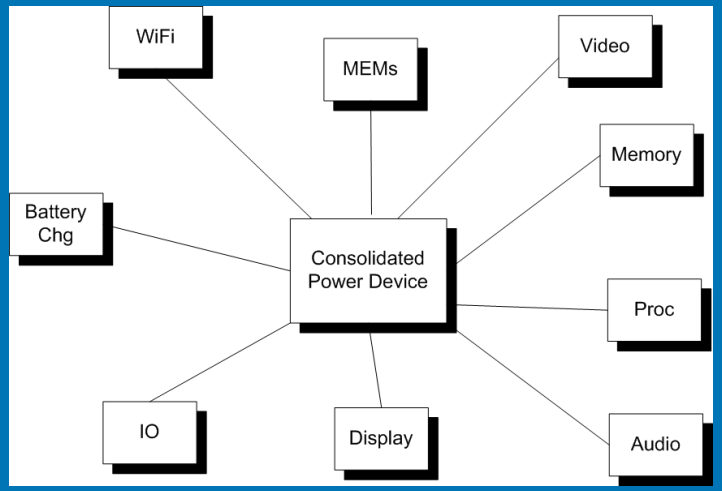
A few Practical Considerations first: we need to work inside-out

- *Architecture*
  - *On-die voltage regulation is NOT the same as on-board voltage regulation!*
  - *More digital, less analog is better*
- *VR Topology*
  - *Voltage levels, frequency, transistors necessitate changes here*
- *For platform component replacement and those that may still be required - must be used judiciously – on-die cap is typically small as are on-die magnetics – size them according to loop-response*
- *System design – since your device is small (whether it is co-located with the silion device, standalone, or on the motherboard) you still need to consider its layout on the platform and board and its proximity to all of the loads.*

The architecture

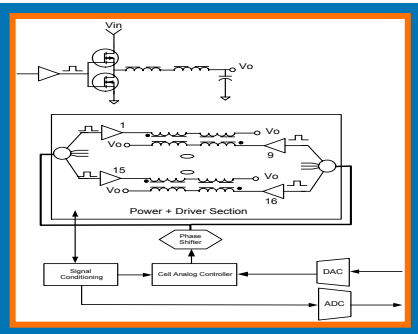
- Design considerations to overcome the barriers…
- Some metrics
  - Power consumption – device should operate in low micro-watt range (or below) as well as in the 10's of watt region.
  - Device should have multiple operation power modes.
  - Device should have many domains to allow for shut down in non-use modes.
  - Leakage should be strongly considered in choosing your process for device.
- Mixed analog/digital noise mitigation techniques should be used throughout.

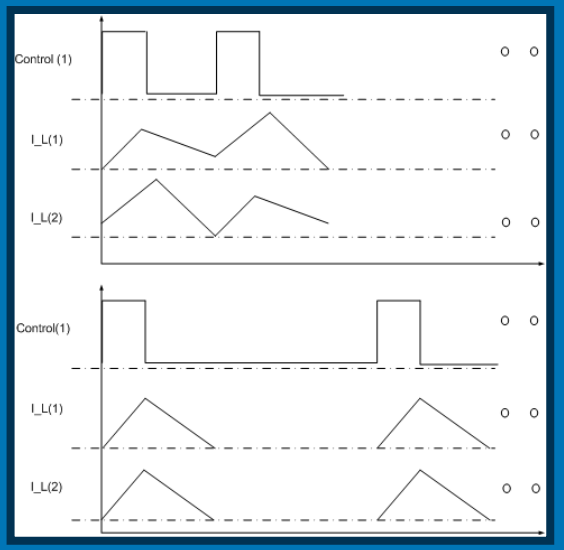


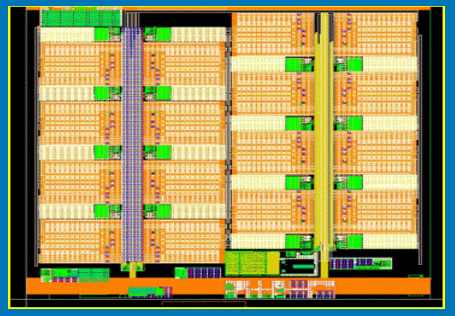


The Topologies

- *VR topologies*
- *Buck type topologies*
- *Coupled systems work best*
  - *Main reasons are saturation mitigation is key*
  - *Which drives size and many other factors*
- *Design topologies to work efficiently at key operating frequencies.*
  - *Controllers need compensation caps and resistors..these do not size well at low frequencies!*
  - *Ultra-low power mode operation is essential – this is a key advantage!*
- *Do not make the same mistake as component suppliers.*







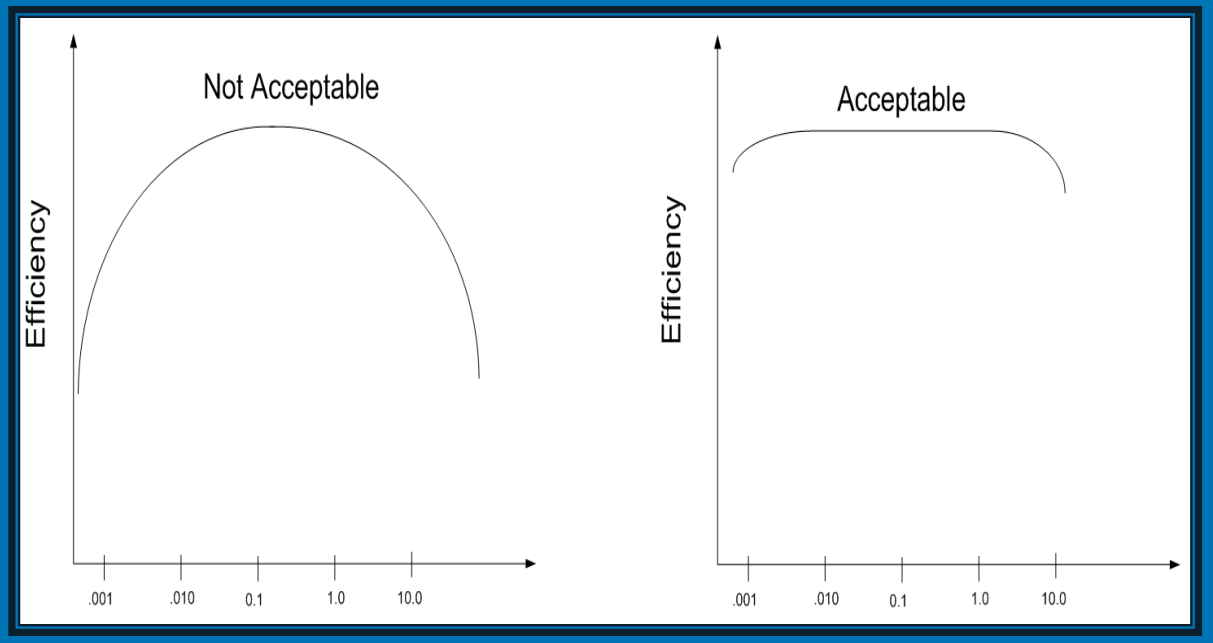
Many small 'VR's and phases is much better than a few large ones

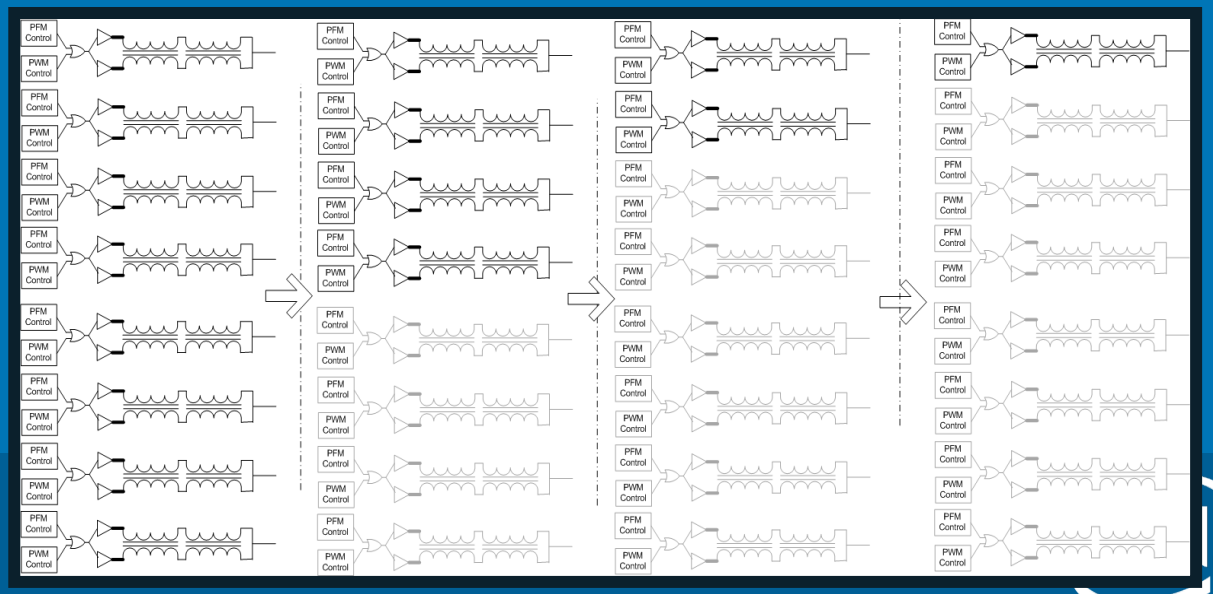
The barriers…finally

- *Power Barrier*
  - *It is **NOT** just the total power that the device needs to deliver, it is the **RANGE** of that power*
  - *It is not just the total number of rails, but the programmability of those rails.*
- *Performance Barrier*
  - *It is NOT just the efficiency that the device needs to meet, it is total system battery savings*
- *Lets give some numbers now…*

Power Barriers..note scales

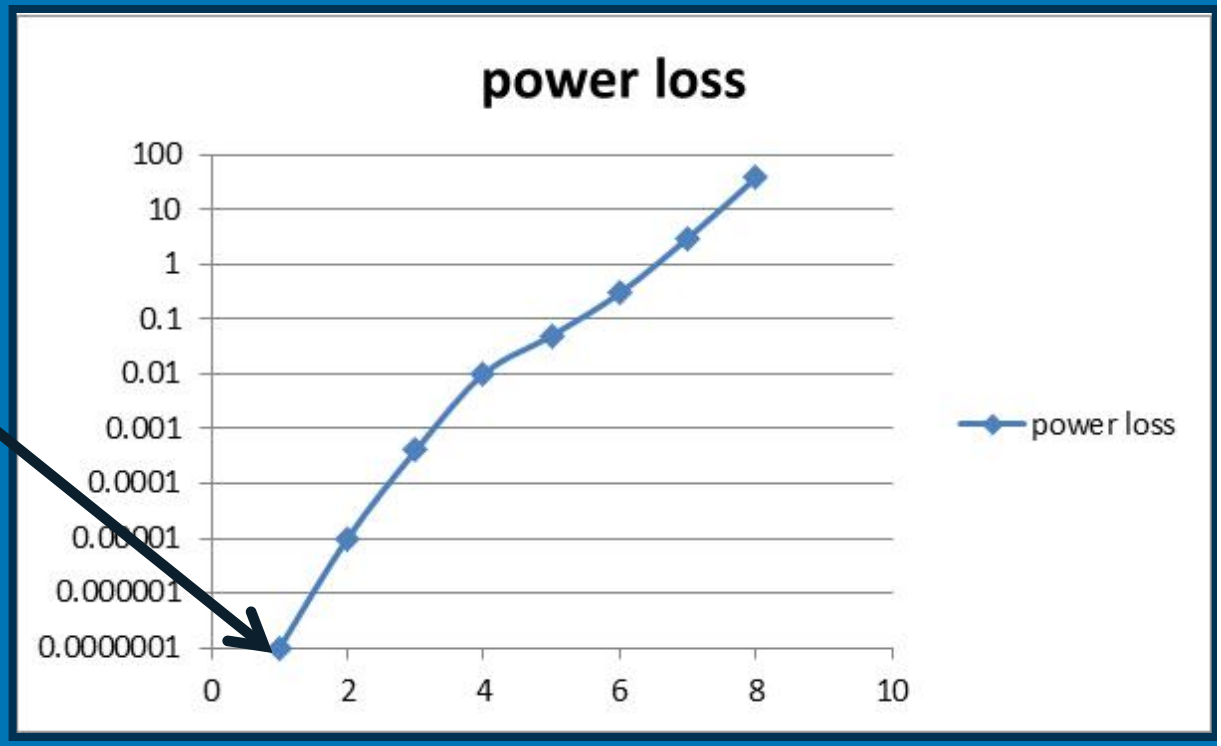
- *Range of operation should be 5 orders of magnitude – not 2 or 3.*
- *Range of control should be at least one order of magnitude..*





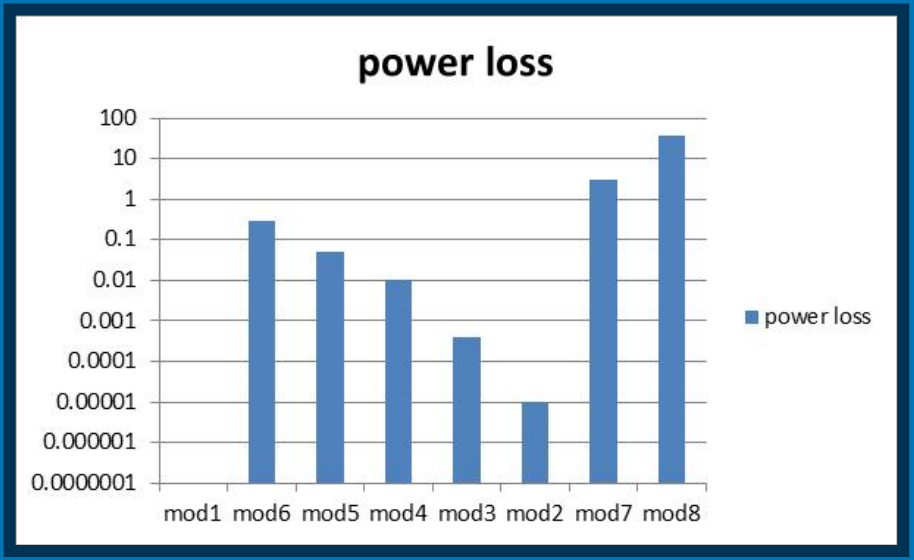
Power Loss and modes

Modes



- *Modal operation should go thru ~10 orders of magnitude…*
- *This is where the industry is heading…why?*

Power Loss and modes

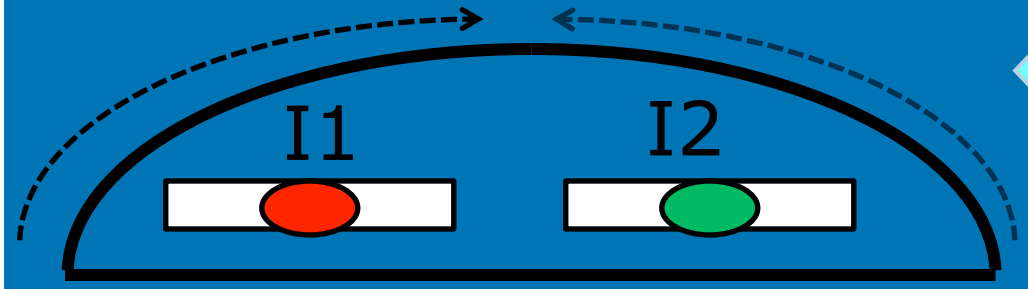


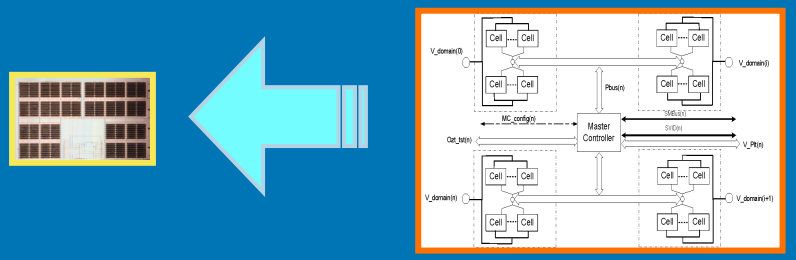
- *The average power is shrinking but the range is growing*
- *This is due to feature and user experience increase.*

On-die magnetics…

$$\psi_1 = M_{12} I_2$$

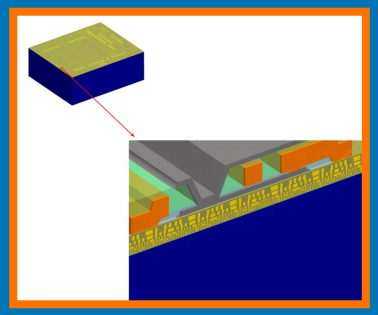
$$\psi_2 = M_{21} I_1$$





The physics and the barriers…

Some physics for on-die magnetics



Start with energy density

$$W_M = \frac{1}{2}\iiint_{\upsilon} \vec{B}\cdot\vec{H}d\upsilon \cong \frac{B^2\upsilon}{2\mu_r\mu_0}$$

Next, look at VR parameters

$$*L_{die} \cong \frac{\Delta V(1/F)D}{\Delta I} \cong \frac{B_{Sat}wt_m}{\Delta I}$$

Then power Loss in magnetics

$$P_{L\_c} \cong \Delta I^2 R_c = \frac{\Delta I^2 l_c}{\sigma w_c t_c}$$

$$P_{L(H)} = f_s \cdot V_m \cdot 2 \cdot H_c \cdot \Delta B$$

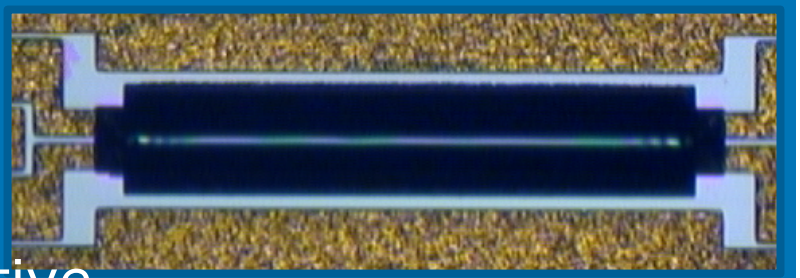
$$P_{L(EC)} = \frac{w \cdot l \cdot t_m^3 \cdot \omega^2 \cdot B^2}{12 \cdot n_{lam}{}^2 \cdot \rho_{MCM}}$$

We will optimize these parameters around the system design

Energy density in the inductor is related to a Number of factors: loss, saturation System operation, coupling, design…

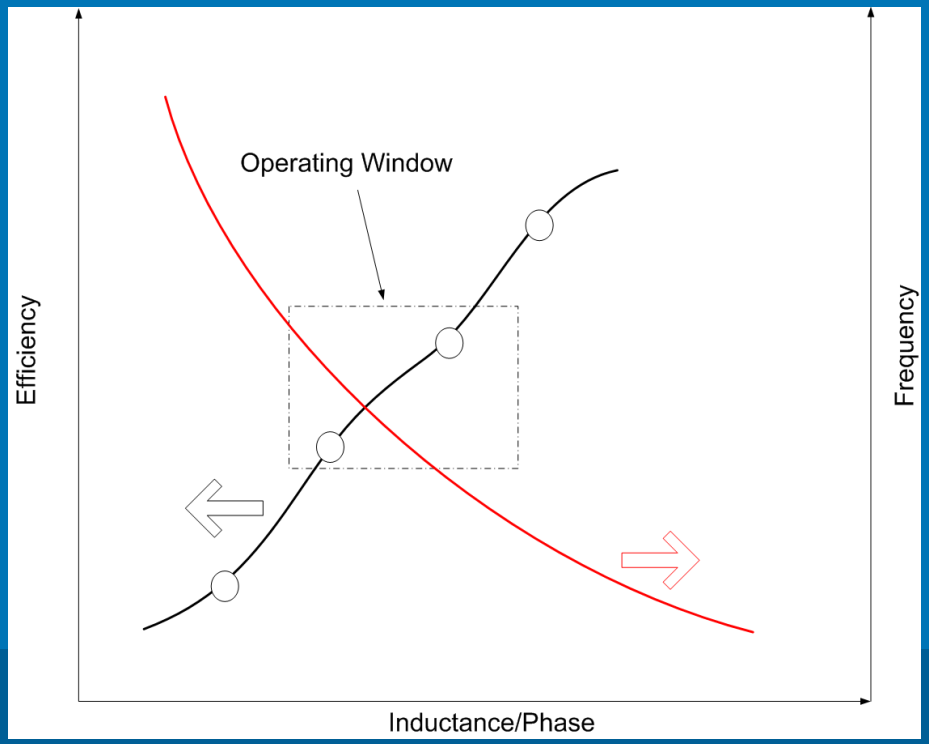
Thin-Film Magnetics in relation to VR Ckts

Single Magnetic Top View



- Want to optimize magnetic power loss relative to other loss factors

$$V(t) = L_1 \frac{di_1}{dt_1} + L_2 \frac{di_2}{dt_2} - M\left(\frac{di_1}{dt_1} + \frac{di_2}{dt_2}\right) \Leftrightarrow P(t) = kf^{\alpha}\hat{B}^{\beta}$$



We will optimize the functions to select the best operating window

Bottom line – we need to optimize for three main things Power loss, inductance, and modal operation – at any one time…

Some basic numbers…before you ask

- *Power loss ranges – in general, the entire device should dissipate less than 15% of the platform power at any one time.*
  - *This is a very loose rule of thumb. There are some platforms which are not as concerned with this.*
- *Must have power on-demand for virtually all rails due to high modal operation at the system level.*
- *Expect your device to have upwards of 40 inductors depending upon application.*

Last Message on the barriers…

- CE devices appear to be first niche, this was true 4 years ago and appears to not have changed.
- Barriers are dependent upon application – But, once a common VR module is built it should be adaptable thru multiple modal operational states.
- VR's and architecture are just as important as technology components – in fact, moving forward, these may be the key differentiators
- *Crack the barriers first – integrate the components - widen the power operation band – meet the power loss in all bands -*

We are done…questions?