Advantages of Paralleling Inductors-on-Silicon in High Frequency Buck Converters

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Abstract

In general power supplies are moving towards higher switching frequencies to reduce the size of passive components with the ultimate goal of integrating the active and passive components on a single power supply on chip (PSoC). This work focuses on paralleling inductors-on-silicon in an 8MHz buck converter to demonstrate the advantages of paralleling inductors-on-silicon in high frequency buck converters.

Introduction

Inductors-on-silicon inherently have low current handling capabilities and high DC resistance due to their size. The purpose of this work is to show that distributing inductors-on-silicon in parallel can:

- Increase the output current while also maintaining the same overall footprint size.
- Retain the same effective inductance as a single inductor with the same footprint size.
- Improve DC-DC circuit efficiency compared with a single inductor.

The performance of distributed inductors is compared in a range of parallel inductor configurations.

Circuit Specification & Topologies

Equivalent single and parallel inductor combinations are compared for the specification in table 1 which is based on a commercially available DC-DC converter from Micrel (MIC2285).

$Freq_{sw}$	8MHz
V_{in}	3.2V
V_{out}	1.8V
$I_{out\ Max}$	500mA

Table 1. Converter specification

Figure 1 shows a typical inductor-on-silicon used in this work.

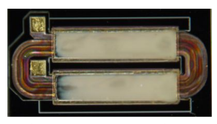

Figure 1. Inductor-on-Silicon

Figure 2 shows the inductors-on-silicon on the adaptor board and Figure 3 shows a Micrel MIC2285YML evaluation board with the inductors-on-silicon adaptor board connected.

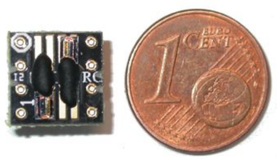

Figure 2. $L2_{p2}$ inductors on an adaptor board

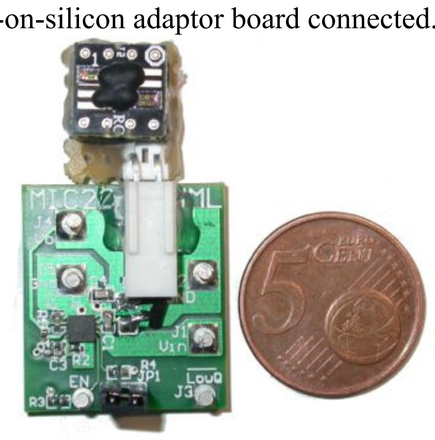

Figure 3. Micrel MIC2285YML board with inductors-on-silicon adaptor board

The single phase buck converter shown in Figure 4 has been investigated with different combinations of inductors outlined in table 2, for example $L1_{s1}$ is equivalent to $L2_{p2}$ and $L3_{p2}$ is equivalent to $L2_{p3}$.

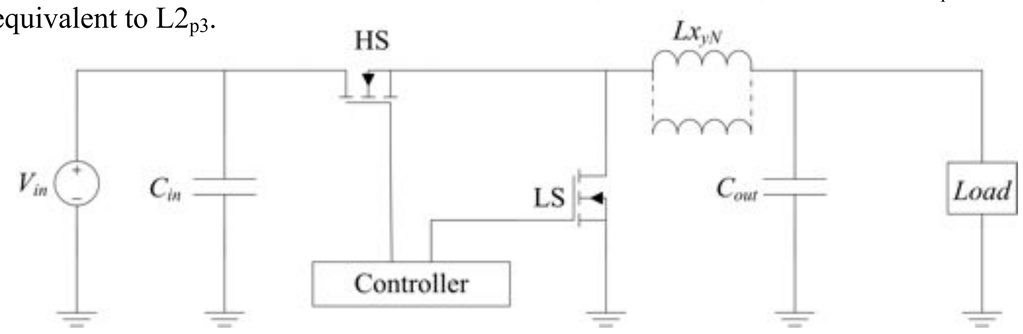

Figure 4. Single phase buck converter with *N* inductors

Device	Equivalent Area	Effective Inductance	Equivalent DCR	Turns	Copper Thickness	Copper Width	Core Thickness
Lx_{yN}	N•mm²	$\frac{L\ (nH)}{N}$	$\frac{Ohms\ \Omega}{N}$	T	µm	µm	µm
$L1_{s1}$	4.06	80	1.041	3	30	116	4.2
$L2_{s1}$	1.95	132	1.388	4	30	38.5	4.2
$L2_{p2}$	2•1.95=3.9	$\frac{132}{2}$ = 66	$\frac{1.388}{2}$ = .694	4	30	38.5	4.2
$L3_{s1}$	3.09	83	1.184	3	30	105	4.2
$L3_{p2}$	2•3.09=6.18	$\frac{83}{2}$=41.5	$\frac{1.184}{2}$ = .592	3	30	105	4.2
$L2_{p3}$	3•1.95=5.85	$\frac{132}{3}$=44	$\frac{1.388}{3}$ = .463	4	30	38.5	4.2

Table 2. Combinations of Inductors-on-Silicon

Analysis of Parallel Inductor Performance

Performance of the inductors in a DC-DC converter was completed for $L1_{s1}$ Vs. $L2_{p2}$ and $L3_{p2}$ Vs. $L2_{p3}$. Figure 5 and 6 show effective Q-factor, Q_{eff} and inductance factor per unit area, A_L/A.

Q_{eff} (1) is defined as the peak energy stored divided by the total energy lost per cycle and A_L/A (2) is the Inductance factor per unit area.

$$Q_{eff} = \frac{f \cdot L \cdot I_{pk}^2/2}{(R_{dc} I_{dc}^2 + R_{ac} I_{rms}^2)} \quad (1) \qquad A_L/A = \frac{L/N^2}{A} \quad (2)$$

The variables are as follows: f is frequency, L is inductance, I_{pk} is the peak inductor current, R_{dc} and R_{ac} are DC and AC resistances, I_{dc} is the DC inductor current, I_{rms} is the RMS of the ripple current, N is the number of inductor turns and A is the footprint area.

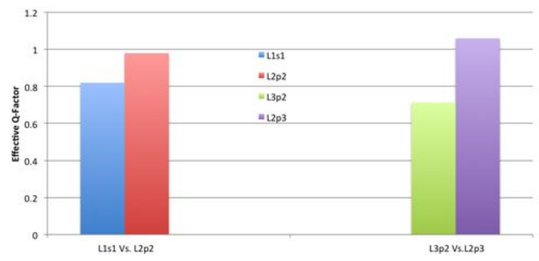

Figure 5. Effective Q-Factor of $L1_{s1}$ Vs. $L2_{p2}$ and $L3_{p2}$ Vs. $L2_{p3}$

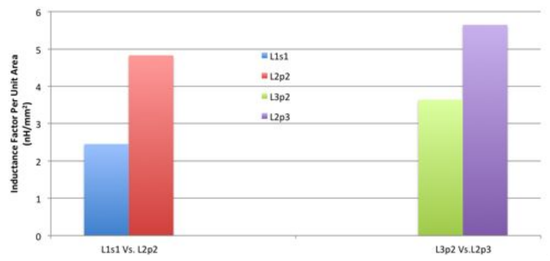

Figure 6. Inductance Factor Per Unit Area of $L1_{s1}$ Vs. $L2_{p2}$ and $L3_{p2}$ Vs. $L2_{p3}$

- Effective Q-Factor is improved for parallel inductors with the same equivalent area.
- Inductance factor per unit area is also improved.

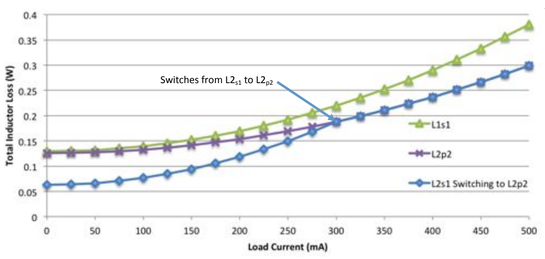

Figure 7. DC and AC conduction loss for $L1_{s1}$, $L2_{p2}$ and $L2_{s1}$ switching to $L2_{p2}$

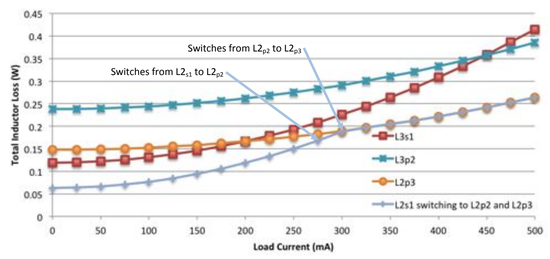

Figure 8. DC and AC conduction loss for $L3_{s1}$, $L3_{p2}$, $L2_{p3}$ and $L2_{s1}$ switching to $L2_{p2}$ and $L2_{p3}$

Parallel Inductors provide the option to switch out parallel inductor paths at low load current resulting in improved light-load efficiency.

Measured DC-DC Converter Performance

Measured converter efficiency results for different inductor combinations are given in figures 10 and 11. Clearly the possibility of switching out parallel inductor paths provides improved efficiency particularly at light-load. The possibility to increase output current with a number of inductors in parallel can also be seen.

Work is ongoing to implement parallel MOSFETs to support parallel inductor paths.

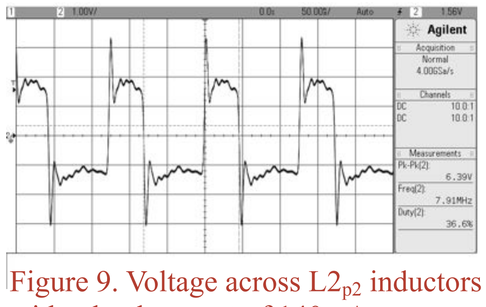

Figure 9. Voltage across $L2_{p2}$ inductors with a load current of 140mA

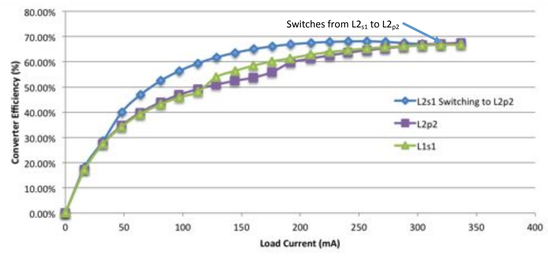

Figure 10. Measured converter efficiency with $L2_{s1}$ switching to $L2_{p2}$, $L2_{p2}$ and $L1_{s1}$

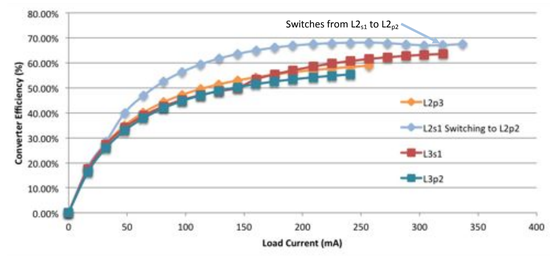

Figure 11. Measured converter efficiency with $L2_{p3}$, $L2_{s1}$ switching to $L2_{p2}$, $L3_{s1}$ and $L3_{p2}$

Conclusions

This work demonstrates that by distributing inductors in parallel efficiency and current handling capabilities of inductors-on-silicon can be improved while maintaining the same overall footprint area and equivalent inductance of a similar single inductor.

Acknowledgments

This project is funded by the NUI Galway fellowship fund and SFI funded National Access Programme (NAP Project 380). It is being completed in association with the Tyndall National Institute, Cork with support from ON Semiconductor. Micrel Inc. provided an evaluation board for testing.

For Further Information

Please contact ciaranfeeney5@gmail.com. More information on this and related projects can be obtained at www.perc.nuigalway.ie