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# Modular ultra low power dc-dc converter with losses reduction using charge recycling.

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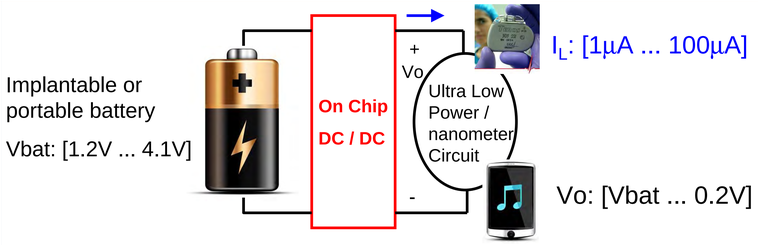
## MOTIVATION




## PROPOSED ARCHITECTURE

- Based on series of capacitors (Fig 1). Phase T1: capacitor charge from VDD, Phase T2: load connection.
- The node connected during T2 determines the conversion ratio.
- The capacitors are rotated in a loop (Fig. 2) so that in steady state the voltage across all of them are approximately equal. Waveforms are shown in Fig. 3.
- Based on a basic cell (Fig 4).

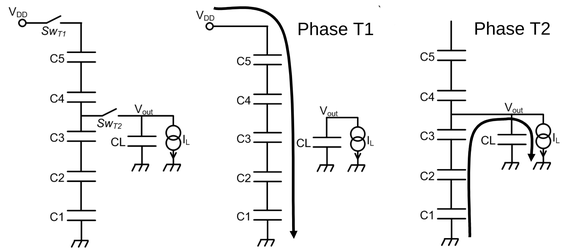



**Fig 1. Basic Idea**

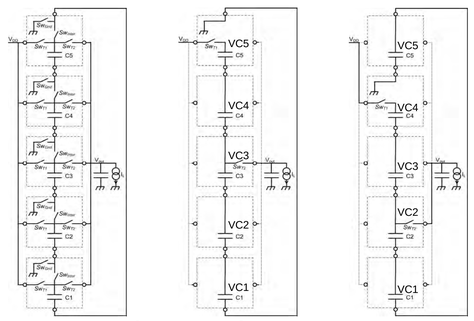


**Fig 2. Rotation process**

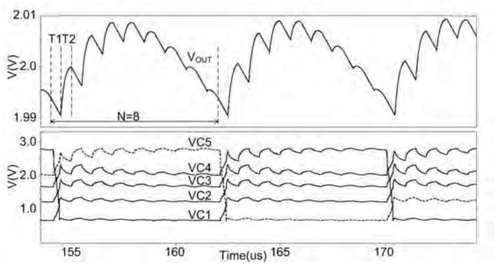
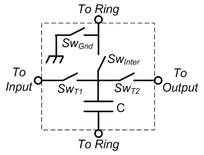



**Fig 3. Voltage waveforms**




Similar to Le et al, IEEE JSSC, 9/2011

**Fig 4. Basic Cell**

## CHARGE RECYCLING TECHNIQUE

- Recycle the charge from parasitic capacitors that need to decrease its charge (related to top plate of C5 (VC5) in Fig. 3) to those that need to increase its charge (top plate of C4…C1 (VC4...VC1) in Fig. 3).
- Fig. 5 summarizes the process and Fig. 6 shows the reduction of the contribution of parasitic capacitances losses (a.k.a bottom plate losses).

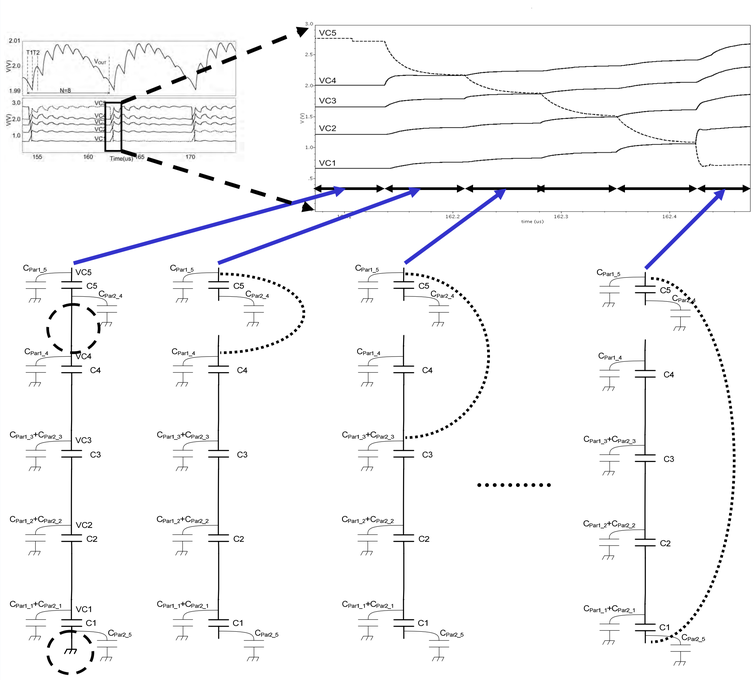



**Fig 5. Charge recycling in one loop rotation step.**

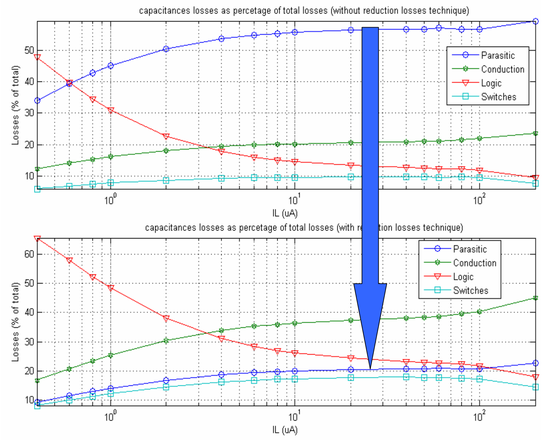



**Fig 6. Reduction in the contribution of parasitic losses.**

## RESULTS

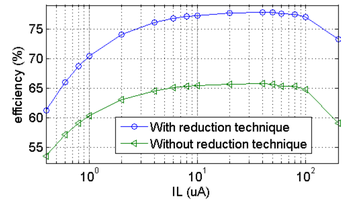



**Fig 7. Efficiency vs. load current (4/5 conv. ratio) with and w.o. parasitic losses reduction technique based on charge recycling**

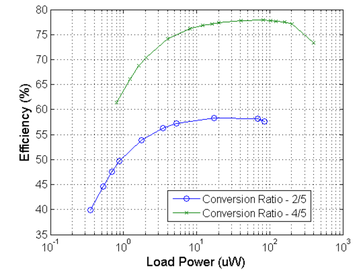



**Fig 8. Efficiency vs. load power .**

| Design | [1] | [2] | This work | |
|---|---|---|---|---|
| Technology (um) | 0.13 | 0.18 | 0.5 | 0.13 * |
| Chip active area (mm2) | 0.52 | 0.57 | 10 | - |
| Total on chip cap (pF) | 350 | 2400 | 29000 | 2000 |
| n (# conversion ratios) | 3 | 5 | 5(10) | 4(6) |
| Vout (V) | 1.1 – 0.3 | 1.1 – 0.3 | 2 – 0.4 | 1.1 – 0.3 |
| VDD (V) | 1.2 | 1.2 & 1.8 | 2.8 | 1.2 |
| Min load current (nA) | 1 uA | 10uA | 1 | - |
| Load Power Range (uW) | 1 - 230 | 5 - 1000 | 0.4 - 200 | - 200 |
| Efficiency range (%) | 80 - 30 | 80 - 50 | 78 - 35 | 80 - |
| Operating frequency (Mhz) | 0.1 – 6.5 | 3.75 - 15 | 0.01 - 1 | 0.2 - 20 |

[1] – O. A.-T. Hasib, M. Sawan, and Y. Savaria, "A low-power asynchronous step-down dc-dc converter for implantable devices", Biomedical Circuits and Systems, Vol. 5, no. 3, June 2011.

[2] – Y.Ramadass and A.Chandrakasan, "Voltage scalabel switched capacitor dc-dc converter for ultra-low-power on-chip applications," in Proc. IEEE Power Electronics Specialists Converence, 2007. PESC, IEEE, pp. 2353-2359.

* - Preliminary results

**Fig 9. Comparison with the state of the art.**

## FUTURE WORK

- Fabrication (2/2013 in 130 nm) and prototype testing.
- Extend the application of the charge recycling principle.

## Acknowledgments

ANII scholarship and CSIC, Universidad de la República