Modeling and Pareto Optimization of Microfabricated Inductors for Power Supply on Chip

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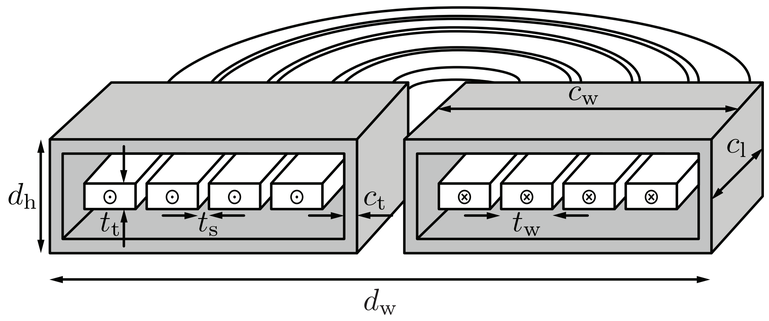
MAIN FEATURES

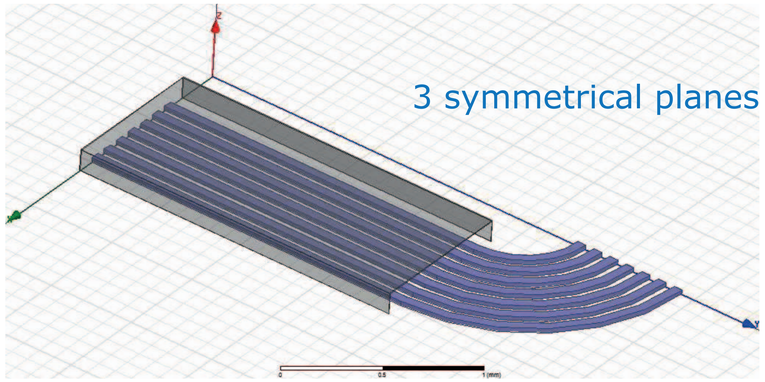
- Accurate cored racetrack inductor model
- Efficiency and power density estimates
- High evaluation speed compared to 3D FEM
- Pareto optimization procedure
- Selection of optimum inductor designs

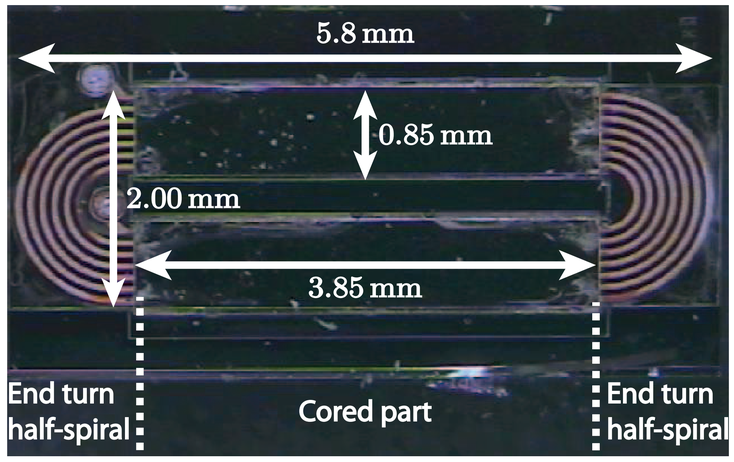


Cored racetrack model includes:

- Influence of losses on the inductor current.
  - Exponential inductor current
- Inductance estimation:
  - Coreless end turn spiral L_{spiral}.
  - Magnetic core L_{core}.
  - Self-inductance of the wires in the cored part $L_{t,core,1}$.
  - Mutual inductance between wires in cored part $L_{t,core,2}$.
- Winding DC losses (R_{dc})
- Winding AC losses (R_{ac})
  - Dowell's analysis
- Core hysteresis losses P_h
- Core eddy current losses P_e
  - Magnetic core considered as a bus bar

Verifying the model with 3D FEM simulations and measured results





Comparison table

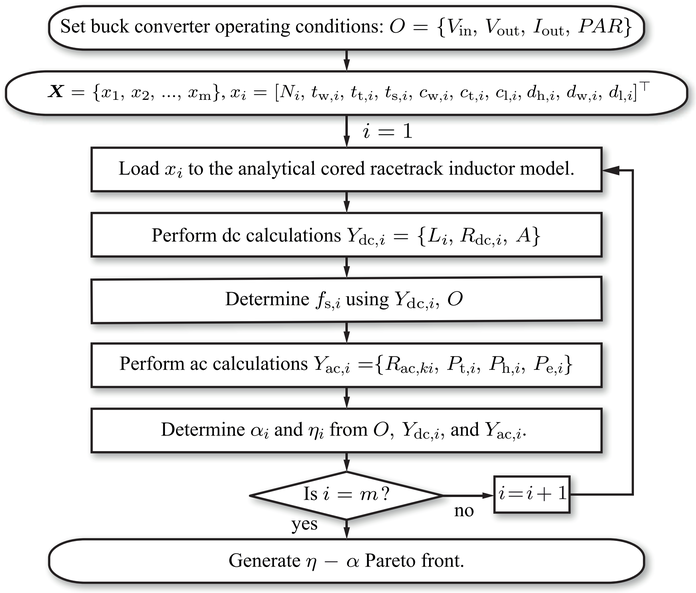
Param.		Calc.	Sim.	[1]	Calc.	Sim.	[2]	Calc.	Sim.	[3]
L_{core}	nH	92	97	–	102	112	–	262	253	–
$L_{t,core}$	nH	28	30	–	19	19	–	63	69	–
L_{spiral}	nH	47	48	–	30	32	–	169	159	–
L	nH	167	175	160	151	163	150	494	481	440
R_{dc}	mΩ	169	180	191	279	297	400	529	576	500
f_s	MHz	20	19	20	30	31	30	17	17	20
R_{ac}	mΩ	249	344	–	315	538	–	765	882	–
P_t	mW	1.1	1.3	1.7	4.8	5.6	9.8	33.8	36.7	31.8
P_h	mW	1.7	1.1	1.7	3.5	2.3	4.3	2.4	1.5	4.0
P_e	mW	2.1	1.8	2.5	8.3	7.2	7.6	2.3	2.3	4.0
P_{loss}	mW	4.9	4.2	5.9	16.6	15.1	22.1	38.5	40.5	39.8
η	%	94.1	94.9	93	91.9	92.6	89.5	88.6	88.1	88.3

[1] R. Meere, T. O'Donnell, H. Bergveld, N. Wang, and S. O'Mathuna, "Analysis of microinductor performance in a 20 – 100 MHz DC/DC converter," *IEEE Trans. on Power Electronics*, vol. 24, no. 9, pp. 2212–2218, Sep. 2009.

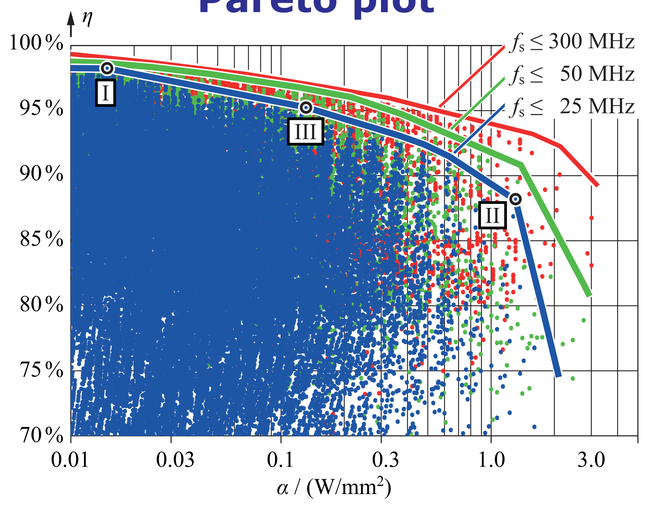
[2] N. Wang, J. Hannon, R. Foley, K. McCarthy, T. O'Donnell, K. Rodgers, F. Waldron, and S. C. O'Mathuna, "Integrated magnetics on silicon for power supply in package (PSiP) and power supply on chip (PwrSoC)," in *Proc. of the Electronic System Integration Technology Conference (ESTC)*, Berlin, Germany, Sep. 2010, pp. 1–6.

[3] N. Wang, T. O'Donnell, R. Meere, F. M. F. Rhen, S. Roy, and S. C. O'Mathuna, "Thin-film-integrated power inductor on Si and its performance in an 8-MHz buck converter," *IEEE Trans. on Magnetics*, vol. 44, no. 11, pp. 4096–4099, Nov. 2008.

Pareto optimization procedure



Pareto plot



[I] - Very high efficiency Pareto design:			
N	4	P_{loss}	4.0 mW
L	41.7 nH	η	98.3%
f_{sw}	21.6 MHz	α	14 mW/mm^2
[II] - Very high power density Pareto design:			
N	2	P_{loss}	30.1 mW
L	40.5 nH	η	88.2%
f_{sw}	22.2 MHz	α	876 mW/mm^2
[III] - High efficiency and high power density Pareto design:			
N	3	P_{loss}	11.3 mW
L	38.6 nH	η	95.2%
f_{sw}	23.3 MHz	α	107 mW/mm^2

Reference:
T. M. Andersen, C. M. Zingerli, F. Krismer, J. W. Kolar, N. Wang, C. Ó. Mathúna, "Modeling and Pareto optimization of microfabricated inductors for power supply on chip," *IEEE Trans. on Power Electronics*, publication pending.