PWR'10 SOC

2nd International Workshop on Power Supply On Chip

www.powersoc.org

October 13-15, 2010

Tyndall National Institute

Cork, Ireland

2nd International Workshop on Power Supply On Chip

Following the overwhelming positive feedback from PwrSOC`08, the second International Workshop on Power Supply on Chip will once again bring together the key players from both the industry and academic communities active in the emerging area of system-in-package (SiP) and system-on-chip (SoC) solutions for power supply miniaturisation.

A major challenge to the further miniaturisation of DC-DC converters is the inability to integrate passive components on silicon due to their relatively large size at today's operating frequencies of 0.5 to 5 MHz. Increasing the switching frequencies into the 10 to 100 MHz region offers the potential for the reduction of passive component values to the point where, with the right technology, their size becomes compatible with silicon device dimensions.

Currently, significant R&D and product development activity is evident in advances in semiconductor, magnetic, capacitor and packaging material technologies that will deliver products operating at multi-MHz frequencies. The ultimate target is to develop new miniaturised product formats that can be referred to as power supply-in-package (PSiP) and power supply-on-chip (PwrSoC). This space has been under increasing focus from semiconductor companies due to their ability to deliver advanced silicon processing technologies and functional integration with increased reliability. This proliferation of functionally-integrated hardware solutions can be seen as an inflection point in the power supply industry which is seeing a dramatic move away from traditional power supply manufacturing (with a focus on the assembly of power supply modules or bricks from discrete components) to an increasing emphasis on power supply products derived from semiconductor and microelectronics platforms and technologies.

At Powersoc '08, the speakers and conference organizers agreed that the interdisciplinary approach of the workshop was essential to the successful development of power supply-on-chip technology. Application needs, technologies, manufacturability and packaging have all converged to the point that a power SoC solution is not only possible but quite likely required in certain applications. Semiconductor manufacturers, materials researchers, system makers and power supply designers all need to come together to address the problems of functional and packaging integration. The 2008 PwrSOC workshop was thus a significant step in that direction and Powersoc '10 is positioned to result in further significant progress in this field.

It is now clear that the concept of integrated power solutions presents a significant disruptive opportunity in power management solutions and warrants an international forum for its discussion and for the elucidation of the key challenges and innovations that lie ahead in the commercialisation of this space.

Tyndall is supported in the organisation of the workshop with technical co-sponsorship by the IEEE Power Electronics Society (PELS) (http://www.ieee-pels.org), the Power Sources Manufacturers Association (PSMA) (http://www.psma.com), and the European Centre for Power Electronics (ECPE) (http://www.ecpe.org).

The workshop is also supported by Enterprise Ireland, Investment Development Agency, Science Foundation Ireland, MIDAS Ireland, IMAPS Europe, National Microelectronics Institute, UK and United Technologies Research Centre.

Dr. Cian Ó Mathúna
General Chair

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General Chair:
Cian Ó Mathúna, Tyndall National Institute

Programme Chairs:
Yan-Fei Liu, Queens University,
Francesco Carobolante, Qualcomm,
Arnold Alderman, Anagenesis,
Saibal Roy, Tyndall National Institute

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Ray Foley, UTRC
Florian Herrault, Georgia Tech
Brice Jamieson, Tyndall National Institute
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Katherine Barry
Saibal Roy
Jeffrey Godsell
Santosh Kulkarni
Shunpu Li
Ningning Wang

Workshop Schedule

Tuesday 12th October

17:30 – 19:00	Registration	

Wendesday 13th October

08:00 – 09:00	Registration	
09:00 – 09:30	Welcome/Workshop Opening	
09:30 – 10:15	Ted DiBene INTEL USA	**Plenary Talk** Power on Silicon with on-die magnetics: The start of a revolution in power delivery and power management for SoC's and high performance applications

Session 1: System Architectures compatible with PwrSoc

Session Co-Chairs: Francesco Carobolante, Ed Standford, Bruno Allard, José Cobos

10:15 – 10:40	Aleksandar Prodic UNIVERSITY OF TORONTO Canada	High-Performance Mixed-Signal Controllers for On-Chip Integrated SMPS
10:40 - 11:05	Alex Vainberg NATIONAL SEMICONDUCTOR USA	Adaptive Voltage Scaling (AVS) Technology
11:05 - 11:35	River Lee Hotel BREAKOUT ROOM Coffee/Tea Break	
11:35 - 12:00	Dominik Schmidt INTEL USA	Challenges and Solutions: Power Delivery and Regulation in NanoCMOS SoCs
12:00 - 12:25	Hans Meyvaert ESAT MICAS K.U. LEUVEN Belgium	The importance of fully-integrated CMOS: Cost Effective Integrated DC-DC Converters
12:25 - 12:50	William O. Keese NATIONAL SEMICONDUCTOR, USA	Power Management Design Challenges and Techniques for Power Amplifiers in 2G/3G/4G Multimode Handsets
12:50 - 14:00	River Lee Hotel Lunch	

Session 2: Technologies and Devices to Enable PwrSoC

Session Co-Chairs: Yan-Fei Liu, John Shen, Shuming Xu

14:00 - 14:25	Anco Heringa NXP, NETHERLANDS	High Voltage transistors for SoCs in baseline CMOS
14:25 - 14:50	Shuming Xu TEXAS INSTRUMENTS, USA	NexFET Technology: New Technology Enables High Power Density
14:50 - 15:15	Paul Chow RENSSELAER POLYTECHNIC INSTITUTE, USA	GaAs p-HEMT-based Power ICs for High Frequency Switching Converter Applications
15:15 - 15:45	River Lee Hotel BREAKOUT ROOM Coffee/Tea Break	
15:45 - 16:05	Sameer Pendharkar TEXAS INSTRUMENTS, USA	Mixed signal technologies enabling PwrSoC and PwrSiP
16:05 - 16:30	Sami Ajram SL3J SYSTEMS France	Power train scaling, high frequency cross talk and its impact on controller design

Session 3: Poster Session

Session Co-Chairs: Brice Jamieson, Ray Foley, Florian Herrault, Magali Brunet, Maeve Duffy, Yan-Fei Liu, José Cobos

19:00 – 20:30	River Lee Hotel BREAKOUT ROOM	Poster Session and Welcome Reception
20:30 – 22:30	River Lee Hotel THE WEIR RESTAURANT Dinner	

Thursday 14th October

Session 4a: Integrated Passives: Magnetics

Session Co-Chairs: Charles R. Sullivan, Maeve Duffy, Matthew Wilkowski, Florian Herrault, Saibal Roy

08:30 - 08:55	Saibal Roy TYNDALL NATIONAL INSTITUTE, IRELAND	Challenges in magnetics for PwrSoC - Development in high-frequency magnetics, materials, and integration
08:55 - 09:20	Donald .S. Gardner INTEL, USA	Integrated On-Chip Inductors Using Magnetic Material
09:20 - 09:45	Sarah Bedair US ARMY RESEARCH LABS, USA	Thin Film Piezotransformers for High Frequency Switched Mode Power Supplies
09:45 - 10:10	Florian Herrault GEORGIA TECH, USA	Lamination-Based Technology for High Performance Metallic Magnetic Cores
10:10 - 10:40	River Lee Hotel BREAKOUT ROOM Poster Session and Coffee/Tea Break	
10:40 - 11:05	Nian Sun NORTHEASTERN UNIVERSITY, USA	Low-Temperature Deposited Metallic Magnetic Films and Ferrite Films and Their Applications in Integrated RF Magnetic Devices
11:05 – 11:30	Matthew Wilkowski ENPIRION, USA	Magnetics on Wafer: Transitioning From Prototype to Manufacturing
11:30 – 12:30	Open Forum Discussion	"PwrSoC or Not"
12:30 - 13:30	River Lee Hotel Lunch	

Session 4b: Integrated Passives: Capacitators

Session Co-Chairs: Seth Sanders, Magali Brunet

13:30 - 13:55	Catherine Bunel IPDiA CAEN, FRANCE	3D capacitors: Manufacturing and applications
13:55 - 14:20	Magali Brunet LAAS CNRS, TOULOUSE, FRANCE	Ultra-high power carbon-based microsupercapacitors
14:20 - 14:45	Mihaela Popovici IMEC, BELGIUM	ALD Strontium Titanates and their characterization
14:45 - 15:10	Stephen O'Brien CITY COLLEGE OF NEW YORK, USA	Printed components and large-area capacitators
15:10 - 15:40	River Lee Hotel BREAKOUT ROOM Poster Session and Coffee/Tea Break	

Session 5: Converter Topologies and Control Systems for PwrSoC

Session Co-Chairs: Ray Foley, Yan-Fei Liu, Eduard Alarcon

15:40 – 16:05	Rais Miftakhutdinov TEXAS INSTRUMENTS, USA	PSiP and PwrSoC Based Opportunities and Solutions for High Power Systems
16:05 - 16:30	Eby Friedman UNIVERSITY OF ROCHESTER, USA	Small Area Power Converter for Application to Distributed On-Chip Power Delivery
16:30 - 16:55	Olivier Trescases UNIVERSITY OF TORONTO, CANADA	Gate-Charge Recovery for Light-Load Efficiency Improvement in High-Frequency DC-DC Converters
18:30 - 23:00	Trident Hotel, Kinsale Workshop Banquet	

Friday 15th October

Session 5: Converter Topologies and Control Systems for PwrSoC

Session Co-Chairs: Ray Foley, Yan-Fei Liu, Eduard Alarcon

08:30 - 08:55	David Anderson NATIONAL SEMICONDUCTOR, USA	Compact, Cost-effective, Efficient Power: Is there a sweet-spot for integration?
08:55 - 09:20	Seth Sanders UC BERKELEY, USA	Integrated Power Conversion - The Switched Capacitor Approach
09:20 - 09:45	Gabriel A. Rincón-Mora GEORGIA TECH, USA	Energy-Harvesting Switching Converter ICs

Session 6: Monolithic Integration vs System in Package

Session Co-Chairs: Arnold Alderman, Baoxing Chen, Cian Ó Mathúna

09:45 - 10:10	Arnold Alderman ANAGENESIS, USA	Overview of product integration
10:10 - 10:35	Bill Liu ANALOG DEVICES, USA	Advanced Power Management Techniques for Portable Applications
10:35 - 11:05	River Lee Hotel BREAKOUT ROOM Coffee/Tea Break	
11:05 - 11:40	Dion Manessis FRAUNHOFER INSTITUTE, GERMANY	Embedded Power Dies for System in Package
11:40 - 12:05	Brian Molloy INFINEON TECHNOLOGIES, USA	Power SoC Vs SiP – Competitive Challenges in High-Volume Applications
12:05 - 12:30	Ashraf Lofti ENPIRION, USA	PowerSoC Commercialisation – Market Drivers and Key Technology Enablers
12:30 - 12:55	Satoshi Matsumoto KYUSHU INSTITUTE OF TECHNOLOGY, JAPAN	Future Power Electronics for Realizing Sustaining Society
12:55 - 13:10	Close of Workshop	
13:10 - 14:15	River Lee Hotel Lunch	

Poster Session

A 100MHz 8x step-up dc-dc converter in 130nm 1.2V CMOS process with micro-fabricated air-core inductor
Lin Xue, Christopher Meyer, Christopher Dougherty, *Sarah Bedair,*Brian Morgan, David P. Arnold and Rizwan Bashirullah
Department of Electrical and Computer Eng., University of Florida, Gainesville, FL 32611
*U.S. Army Research Laboratory, 2800 Powder Mill Road, Adelphi, MD 20783.

Fully Integrated Switched-Capacitor DC-DC Converters in Standard CMOS: The Key- Enabler for on-chip Power Management
Tom Van Breussegem, Hans Meyvaert and Michiel Steyaert ESAT – MICAS K.U. Leuven – Kasteelpark Arenberg 10 Belgium

Multilayer Micromachined Air-Core Power Inductors and Transformers
Christopher D. Meyer[1], Sarah S. Bedair[2], Brian C. Morgan[2], and David P. Arnold[1]
[1]Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL 32611
[2]U.S. Army Research Laboratory, Adelphi, MD 20783

Performance and Fabrication of On-Chip Power Inductors Using Multi-Layer Co-Zr-O Films
Di Yao, Jizheng Qiu, and Charles R. Sullivan
Thayer School of Engineering at Dartmouth, Hanover, NH, USA

Effect of anisotropic permeability on a closed-core inductor
Joyce Mullenix[1] and Shan X. Wang[1, 2]
[1.] Dept. of Electrical Engineering, Stanford University, Stanford, CA 94305, USA
[2.] Dept. of Materials Science and Engineering, Stanford University, Stanford, CA 94305, USA

Improvement of the efficiency of HF DC/DC converters by resonant gate drivers
Malal Bathily, Frederic Hasbani and Bruno Allard
STMicroelectronics (Crolles) 850 rue Jean Monnet 38926 Crolles, France

Output cap reduction thanks to a fast and novel control technique: V^2I_C control
M. del Viejo; P. Alou; J. A. Oliver; O. García; J. A. Cobos.
Centro de Electrónica Industrial. Universidad Politécnica de Madrid**,** Madrid, Spain

Potential for improved efficiency of PwrSoC with parallel micro-inductors
M. Duffy[1], N. Wang[2]
[1] Power Electronics Research Centre, NUI Galway, Ireland
[2] Tyndall National Institute, Cork, Ireland

Fully-Integrated Inductive DC-DC converters in Standard CMOS
Mike Wens, Hans Meyvaert and Michiel Steyaert
ESAT-MICAS K.U.Leuven – Kasteelpark Arenberg 10 Belgium

Portable PV Fed Maximum Power Point Tracking Switched Capacitor Battery Charger
Pradeep K. Peter, Indian Space Research Organization, India
Vivek Agarwal, Indian Institute of Technology Bombay, India

A novel simple-inductance, double-output Step-down converter for embedded audio applications
Xavier Branca, ST ERICSSON, Grenoble, France

Integrated LC filter on silicon for DC-DC converter applications

Magali Brunet, Philippe Artillan, David Bourrier, Jean-Pierre Laur, Nicolas Mauran, Laurent Bary, Monique Dilhan, Bruno Estibals, Corinne Alonso and Jean-Louis Sanchez
Laboratoire d'Analyse et d'Architecture des Systèmes (LAAS-CNRS), 7 avenue du Colonel Roche, 31077 Toulouse cedex 4, France

Design of a DC-DC Converter with Co-Packaged Inductor

Jason Hannon, Santosh Kulkarni, Ray Foley, Ningning Wang, Saibal Roy, Cian O'Mathuna and Kevin McCarthy, Tyndall National Institute, Cork, Ireland

A 150V Power SOI LDMOS Transistor for MHz Frequency Switching Applications

Patrick Shea
University of Central Florida, USA

GaN Schottky diodes for high operating temperature electronics

Donagh O'Mahony[(1)], Pleun Maaskant[(1)], Peter J. Parbrook[(1,2)] and Brian Corbett[(1)]

[(1)]Tyndall National Institute University College Cork, Lee Maltings, Cork, Ireland.
[(2)]Department of Electrical and Electronic Engineering, University College Cork, Western Road, Cork, Ireland.

Digital Control of Multi-Rail DC-DC Converter Systems with Non-Integer Switching Frequency Ratios

James Mooney
University of Limerick, Ireland

HIGH-FREQUENCY COMPLEX PERMEABILITY ANALYSIS OF CONIFE FERROMAGNETIC THIN FILMS FOR INTEGRATED PASSIVES.

Jeffrey F. Godsell, Santosh Kulkarni and Saibal Roy
Tyndall National Institute, Cork, Ireland.

Engineered Anisotropy in Modulated Magnetic Films for Miniaturized Devices

Shunpu Li, Jeffrey Godsell, Saibal Roy
Tyndall National Institute, Cork, Ireland

20MHz DC-DC Converter with Integrated Inductor on Si

Ningning Wang[1], Jason Hannon[2], Ray Foley[2], Kevin McCarthy[2], Kenneth Rodgers[1], Finbarr Waldron[1], Santosh Kulkarni[1], Saibal Roy[1], Cian Ó Mathúna[1]
[1]Tyndall National Institute, University College Cork, Ireland, [2] Dept. of Electrical Engineering , University College Cork, Ireland, [3] Enterprise Ireland, Industry House, Rossa Avenue, Bishopstown, Cork, Ireland

AN IMPROVED CALCULATION METHOD FOR AC COPPER LOSSES IN POWER INDUCTORS INTEGRATED ON SILICON

Ningning Wang, Sean Cian Ó'Mathúna

Tyndall National Institute, University College Cork, Ireland,

Structural and Electrical Analysis of Interface Control Layers of MgO or Al2O3 Deposited by Atomic Layer Deposition, at the high- κ/III-V Interface

A. O'Mahonya, S. Monaghana, R. Chiodoa,b, I. M. Poveya, A. Blakea, K. Cherkaouia, R. E. Naglea, É. O'Connora, R. D. Longa, V. Djaraa, D. O'Connella, F. Crupib, P. K. Hurleya and M. E. Pemblea
[a] Tyndall National Institute, University College Cork, Lee Maltings, Prospect Row, Cork, Ireland.
[b] Università della Calabria, Via P. Bucci, 41C I-87036 Arcavacata di Rende (CS), Italy.

KEYNOTE SPEECH

Power on Silicon with on-die Magnetics: The Start of a Revolution in Power Delivery and Power Management for SoC's and High Performance Applications

Ted DiBene

Intel

USA

Abstract:

"Power delivery for advanced platforms, from consumer electronics to large servers is becoming very challenging. Sophisticated power management on these platforms, particularly in the high power devices, has been ongoing for some time but much, much more is needed. Until very recently, the problems with on-die power delivery have resulted in low current and low efficiency indicating that it might be a while before this technology was mature enough to be introduced into products. However, this has now changed. This presentation will illustrate some of the platform level challenges and will then discuss in detail a technology that has broken the mold in on-die power delivery with magnetics and will show a device that has the capability of powering an entire server platform with a device the size of a fingernail."

Bio:

J. Ted DiBene II is currently a lead silicon power architect at Intel advancing both silicon and system power management. His recent focus has been in power management for microprocessors and other silicon devices including SoC's. Prior to that, Dr. DiBene was the lead architect and senior technologist for a highly advanced integrated silicon power chip inside of Intel. Along with his background in power he has spent a large portion of this time on system architecture. Prior to working at Intel, Dr. DiBene was the chief technology officer at INCEP Technologies, a startup in San Diego. He has been involved in advanced signal integrity, power system management, and platform research and development since the late 80's and has brought many products thru the development process over his career. Dr. DiBene holds a BSEE from UC Santa Barbara as well as an MSEE and PhD in Applied Physics and Electrical Engineering from UC San Diego. He holds 26 patents and has authored over 50 papers in the area of power, signal integrity, and thermal. He is an affiliate professor at the University of Washington and spends his spare time volunteering his time to education of bio-diesel and other energy conservation efforts at high schools.

Session 1: System Architectures compatible with PwrSoC

Session Co-Chairs: Francesco Carobolante, Ed Stanford, Bruno Allard, José Cobos

Potential application areas for on-chip or highly integrated power supplies include mobile/battery powered devices, microprocessor power supplies, power management for RF transmitters, energy harvesting, etc. This session addresses the key system-level issues brought out by power supply on chip and other power integration techniques. The session will also discuss the requirements, constraints and trade-offs (i.e. performance, cost, complexity) in such systems with a view to defining the potential benefits of power supply integration. Other issues to be discussed will include: suitable input voltages, single or 2-stage conversion, point of load, integration with load.

10:15 – 10:40	Aleksandar Prodic UNIVERSITY OF TORONTO Canada	High-Performance Mixed-Signal Controllers for On-Chip Integrated SMPS
10:40 - 11:05	Alex Vainberg NATIONAL SEMICONDUCTOR USA	Adaptive Voltage Scaling (AVS) Technology
11:05 - 11:35	River Lee Hotel BREAKOUT ROOM Coffee/Tea Break	
11:35 - 12:00	Dominik Schmidt INTEL USA	Challenges and Solutions: Power Delivery and Regulation in NanoCMOS SoCs
12:00 - 12:25	Hans Meyvaert ESAT MICAS K.U. LEUVEN Belgium	The importance of fully-integrated CMOS: Cost Effective Integrated DC-DC Converters
12:25 - 12:50	William O. Keese NATIONAL SEMICONDUCTOR, USA	Power Management Design Challenges and Techniques for Power Amplifiers in 2G/3G/4G Multimode Handsets
12:50 - 14:00	River Lee Hotel Lunch	

High Performance Mixed Signal Controllers for On-Chip Integrated SMPS

Aleksandar Prodic

University of Toronto, Canada

Abstract:
This paper gives a review of emerging digital and mixed-signal control methods and architectures for on-chip integrated dc-dc switch-mode power supplies (SMPS). The paper is divided into three main parts.

First, it discusses practical implementation problems of digital controllers and shows architectures enabling operation of at ultra high switching frequencies (beyond 100 MHz) allowing significant minimization of the power stage components.

The second part addresses dynamic response of controllers and associated problems of the output filter overdesign creating challenges in on-chip integration of the filtering components. In this part mixed-signal control solutions for obtaining minimum output filter size, defined by the physical limitations of a given power stage, is shown. The presented mixed-signal controller does not require any prior knowledge about the components values and, as such, eliminates the need for custom design.

In the final part, load-interactive controllers and advanced SMPS topologies further minimizing the size of the reactive components and improving power processing efficiency are shown. Theoretically, the presented load-interactive solutions allow drastic reduction of the filtering components, such that their size is limited by the output ripple value only.

Bio:

Aleksandar Prodic is an associate professor at the ECE department of the University of Toronto, where, in 2004, he formed Laboratory for Power Management and Integrated SMPS. He received his Ph.D. and M.Sc. degrees from the University of Colorado in Boulder, and Dipl. Ing. degree from the University of Novi Sad in Serbia.
His research interests include digital and mixed-signal control of low to medium power high-frequency SMPS, mixed-signal IC design for power electronics, and converter topologies.
In this area he has more than 70 journal and conference publications.
Prof Prodic a recipient of IEEE Power Electronics Transactions Paper Award, and multiple IEEE conference paper prizes. He is especially proud of two Excellence in Teaching Awards, elected and given by the University of Toronto undergraduate students.

Adaptive Voltage Scaling (AVS) Technology

Alex Vainberg

National Semiconductor, USA

Abstract:

With the emphasis on lowering power consumption a concern for system designers, National Semiconductor has pioneered a technology for reducing the energy consumed by large-scale CMOS ASICs and other digital systems on a chip (SoCs).

This technology is called Adaptive Voltage Scaling (AVS) which can reduce the overall energy consumption by 40% or more. AVS is a closed-loop control system that not only handles process variation between devices, but it also handles shifts in temperature, digital load, and process aging.

Bio:

B.Sc. of Engineering from Technology Institute in Haifa, Israel
M.Sc. Electrical Engineering from Tel-Aviv University, Israel
Worked on different engineering and management positions at Tower, Jazz Semiconductor, Novelics and National Semiconductor.
Has an expertise in intellectual property development, foundry and mixed-signal design

Challenges and Solutions: Power Delivery and Regulation in NanoCMOS SoCs

Dominik Schmidt

Intel, USA

Abstract:

As geometries scale to 32nm and below, the voltage-handling capability of CMOS systems is coming under increasing strain. The core transistors and SRAM cells are constrained to mV levels, and even the periphery devices no longer offer a dependable interface to system voltages. At the same time, voltage regulation and conversion systems can inject unacceptable noise into the substrate, with ever more complex power routing schemes and ground-plane management. As with other aspects of CMOS scaling, these problems come with opportunities, such as potentially lower power conversion losses due to improved switching, SoC-level quasi-adiabatic power management techniques and increasing integration of regulation sub-systems on the nanoCMOS die. To balance these tradeoffs requires a careful re-assessment of the overall SoC design process, including new EDA tools and circuit techniques.

Bio:

Dominik Schmidt, M.S.M., Ph.D., PE has been working in the semiconductor industry for 20 years. He earned his EE doctorate from Stanford in 2003. He was at Altera working in reconfigurable logic and has worked with Sharp, TI, Cypress and TSMC. He co-founded Pixel Devices International (PDI) in 1997, one of the first companies to offer CMOS imaging chips. After PDI was acquired by Aglient he founed Airify Communications, specializing in multi-protocol wireless chip design. Following the acquisition of Airify, Dr. Schmidt is now Director of Engineering at Intel Corporation, where he is leading the introduction of next generation mixed-signal processes. He has also worked for the Stanford Linear Accelerator and Lawrence Berkeley National Laboratory on several advanced projects, and consulted for several large companies and startups in the mixed-signal and RF design areas. He has taught at UC Extension since 2000 and also taught at Tsinghua University in Beijing and the Swedish Royal Institute. He is wiring a graduate textbook on RF Design for Elsevier Press. He is also a Lieutenant with the US Coast Guard.

The Importance of Fully-Integrated CMOS: Cost Effective Integrated DC-DC Converters

Hans Meyvaert

ESAT MICAS K.U. Leuven, Belgium

Abstract:

Scaling of CMOS is enabling ever more complex systems to be fully-integrated on a single die, this results in various System on Chip (SoC) designs with advanced functionality available at ever lower processing cost. Transistor supply voltages are low in these advanced CMOS technologies in order to reduce power consumption. At the same time battery supply voltages remain constant or even increase to enable a higher energy density. This creates a gap that cannot be solved by the well known linear regulator technology due to their poor associated efficiency.

Integrated switched-mode DC-DC converters are a much better choice to close this gap in terms of conversion efficiency. As a result, switching converters are able to increase the autonomy in mobile devices, thereby reducing battery constraints. Moreover, they are also crucial in high-end designs such as CPU' s and SoC' s by avoiding excess power losses and alleviating thermal issues.
Research at the MICAS (K.U.Leuven) laboratory has explored the field of both fully-integrated inductive and fully-integrated capacitive converters. Since 2006 this has resulted in more than 13 prototypes of fully-integrated DC-DC converters in standard CMOS.

In these prototypes various specifications important for DC-DC conversion are targeted. These include high efficiency (up to 88%), low ripple (down to 0.5%), reconfigurability, high power density (213mW/mm2), large conversion ratio (10X) and tight control (PID, hysteretic,...).
This presentation will give an overview of the results produced by the research conducted at MICAS. It will go deeper into the fundamental restrictions of fully-integrated DC-DC converters in standard CMOS. But also the opportunities of on die power management.

Bio:

Hans Meyvaert was born in Sint-Truiden, Belgium, in 1985. He received the M.Sc. degree in electrical engineering from the Katholieke Universiteit Leuven (K.U.Leuven), Belgium, in 2009.
Currently he is a research assistant at the ESAT-MICAS Laboratory of the same university where he is working towards the Ph.D. degree. His research interest includes on die power management in general and currently capacitive DC-DC converters in specific.

Power Management Design Challenges and Techniques for Power Amplifiers in 2G/3G/4G Multimode Handsets

William O. Keese

National Semiconductor, USA

Abstract:

The linearity requirements and complexity of the handset RF Front End to support multimode multi-band architectures place a premium on power amplifier performance. With the explosion of high-speed data services on the radio channel and resultant increase in average output power, the importance of the transmitter efficiency is emphasized even more. A variable PA power supply offers superior and unique performance benefits for improving talk time of mobile phones by maximizing utilization of battery power consumed.

This presentation reviews the technical advantages of implementing DCDC converters in mobile transmitters and discusses the relative efficiency and current consumption improvements. Recent advancements in power management design technology and system techniques to address the specific challenges in meeting multimode performance requirements will be discussed.

Bio:

Senior member of Technical Staff at National Semiconductor, leads the system definition and architecture of RF power supplies for handset power amplifiers. Previously he has been in the forefront of innovation and development of Frequency Synthesizer, Femtocell, and RFIC wireless communications devices and architecture.

Session 2: Technologies and Devices to Enable PwrSoC

Session Co-Chairs: Yan-Fei Liu, John Shen, Shuming Xu

This session discusses active switching power devices suitable to facilitate various PwrSoC concepts, ranging from traditional BCDMOS to vertical/lateral hybrid devices and SOI RESURF devices. The focus will be on switching frequency from multi-MHz up to radio frequency (RF), process compatibility, and special power electronics requirements such as SOA and energy capability of different CMOS-based device technologies.

14:00 - 14:25	Anco Heringa NXP, NETHERLANDS	High Voltage transistors for SoCs in baseline CMOS
14:25 - 14:50	Shuming Xu TEXAS INSTRUMENTS, USA	NexFET Technology: New Technology Enables High Power Density
14:50 - 15:15	Paul Chow RENSSELAER POLYTECHNIC INSTITUTE, USA	GaAs p-HEMT-based Power ICs for High Frequency Switching Converter Applications
15:15 - 15:45	River Lee Hotel BREAKOUT ROOM Coffee/Tea Break	
15:45 - 16:05	Sameer Pendharkar TEXAS INSTRUMENTS, USA	Mixed signal technologies enabling PwrSoC and PwrSiP
16:05 - 16:30	Sami Ajram SL3J SYSTEMS France	Power train scaling, high frequency cross talk and its impact on controller design

High Voltage Transistors for SoCs in Baseline CMOS

Anco Heringa

NXP, Netherlands

Abstract:

In many modern IC applications the supply voltage has to be converted to the lower voltage as needed by advanced CMOS technology. Preferably the power management enabled by HV-transistors, should be integrated with the advanced CMOS circuits in baseline CMOS technology offering a one-chip solution which guarantees cost competiveness and short time to market.
Both advanced CMOS at one hand and the high voltage transistors as needed in SoCs on the other hand have their own figures of merit with feature size and clock speed for CMOS and breakdown voltage, power handling, on-resistance and high frequency as key features for HV-transistors. We will show that the extreme feature size and process control from advanced CMOS can be exploited for the implementation of HV-transistors. By smart-layout of shallow trench, implants and poly/field plates HV-transistors can be realized in a base line state of the art sub-100 nm bulk foundry CMOS or PD-SOI CMOS process with figures of merit on par with transistors in special purpose HV-processes. Also the Hot-Carrier/reliability characteristics of these transistors, often being a major limiting factor, meet the requirements for a 10 year operational life time.

Biographies

Anco Heringa
Anco Heringa graduated in technical physics at the University of Groningen in 1977.
From 1977-1987 he did research on medical physics and cardiophysics at the Catholic University Nijmegen.
From 1987-2002 he was consultant in process, device and interconnect modelling in Philips Research and Philips Semiconductors. Since 2002 he is with Philips Research, now NXP Semiconductors, Leuven, Belgium, working on advanced CMOS and on integrated high voltage devices.

Jan Šonský
Jan Šonský has received MSc. in solid state physics at Czech Technical University in Prague, Czech Republic, in 1997 and his PhD degree at Delft University of Technology, The Netherlands, in 2002 on ultra-low noise silicon X-ray detectors. He joined Philips Research, now NXP Semiconductors, Leuven, Belgium, in 2002, where he has been working on integrated power management, RF power and SOI processes, and power conversion discrete technologies, including GaN. He serves on technical committees of ISPSD and IEDM, holds over 25 patents/patent applications in semiconductors and published on radiation detectors and high voltage and smart power technologies.

NexFET Technology: New Technology Enables High Power Density

Shuming Xu

Texas Instruments, USA

Abstract:

In this presentation, a new device technology NexFET will be discussed. It improved the Figure of Merit (FOM) drastically, allowing high frequency operation, reducing the filter size. Scaling down to low voltage, NexFET shows great reduction of cost and better performance, promising two stage operation for MHz operation. The second generation NexFET is configured as source on the bottom of the substrate, allowing stacking the high side switch device on the low side synchronies device directly: this reduces the footprint by 50%, eliminates three parasitic inductors out of four. Furthermore, it removed the PCB parasitic resistance between the two devices in the traditional way. With the stack die power block, high frequency and small active block can be achieved simultaneously.

Bio:

Shuming Xu, graduated from Jiaotong University, Xian China in 1982. Received his Master's degree from Shaanixi Microelectronics Institute in 1987 and got the Ph. D from University of Bremen, Germany in 1997. Shuming worked in Daimler-Benz AG in Germany, IME in Singapore, Vishay Siliconix in CA, where he worked for power MOSFET development based on Trench technology; From 2001 to 2004, Shuming worked at Agere Systems and worked for RF LDMOS development. In the beginning of 2005, he co-founded a company called Ciclon Semiconductor and served as VP of technology. Where lead the development of NexFET. He is currently the Chief Technologist in Power Stage of Power Business Unit, Texas Instruments.

GaAs p-HEMT-based Power ICs for High Frequency Switching Converter Applications

Paul Chow

Renesselaer Polytechnic Institute, USA

Abstract:

Switching regulators operating at 100s of Megahertz would enable high bandwidth power supplies capable of catering to the fast load transients especially in point of load converters in portable battery powered appliances. Such switching frequencies also allow for the use of air-core inductors, which can be integrated on chip or on package to minimize the form factor and achieve high power densities. However, the efficiency of hard-switched converters decreases drastically at these frequencies because of the gate driver and output switching loss in the power transistor, which are proportional to the gate charge of the FET used. Due to their improved material properties and device structure, GaAs pHEMTs, which are Schottky gate, field-effect transistors with a high mobility 2DEG channel, are shown to have a 2 to 4x advantage in figure of merit over silicon N-MOSFETs with the same voltage rating.

Enhancement mode low leakage pHEMTs are available through commercial foundries and are suitable for monolithic high frequency power supplies. We demonstrate a 4.5V input, 0.5-3.3V output, 1-2A multiphase buck converter in a 0.5um E/D pHEMT process with the power transistors, gate drivers and charge pumps integrated ON chip. A thick metal air-core coupled spiral inductor fabricated on a GaAs substrate is used in the output filter. The converter is capable of operating at a switching frequency of up to 200MHz and achieves a peak efficiency of 86%.

Bio:

Professor, RPI
Dept. of Electrical, Computer and Systems Engineering
Education: B.A., Mathematics and Physics, Augustana College (S. Dak.); M.S., Materials Science, Columbia University; Ph.D., Electrical Engineering, Rensselaer Polytechnic Institute (RPI).
Experience: Dr. Chow was a member of the technical staff at GE-CRD from 1977 to 1989. Since 1989, he has been with RPI, where he is now professor of the Electrical, Computer and Systems Engineering Department. He has been working in the power semiconductor device area since 1982. His present research activities include novel device concepts, processing and circuit models for high-voltage silicon, GaAs and wide bandgap (particularly SiC and GaN) semiconductor power devices. He has published over 100 papers in scientific journals, has contributed seven chapters in technical textbooks, and has filed over fifteen patents. He is a fellow of the IEEE and a member of the Electrochemical Society.

Mixed Signal Technologies Enabling PwrSoC and PwrSiP

Sameer Pendharkar

Texas Instruments, USA

Abstracts:

This presentation will focus on recent advances and innovations in mixed signal bicmos-dmos technologies that enable complex power SoCs as well as multi-chip power SiPs. Key performance metrics and robustness (short term and long term) criteria and characterization techniques will be presented. While the advances in lithography and processing help with SoC design, it also introduces challenges in monolithic integration of digital, analog, power and passives which drive new integration techniques and power device and esd design. The presentation will also touch on a few packaging techniques that enable SiP and help integrate disparate technologies to improve overall system performance.

Bio:

Sameer Pendharkar graduated in Electrical Engineering at the University of Wisconsin-Madison in 1996 Since 1996, he has been at Texas Instruments Inc., Dallas, USA where he is presently a TI-Fellow and manager of high voltage and power component development team. His group's main focus is defining integrated power roadmap and designing and developing high voltage and high power devices and ESD components for numerous BiCMOS and High Voltage CMOS technologies. He has published more than 50 papers and has more than 50 issued patents in the general area of semiconductor devices and processing.

Power Train Scaling, High Frequency Cross Talk and its Impact On Controller Design

Sami Ajram

SL3J Systems

Abstract:

The emergence low cost Chip Scale and Flip Chip packaging techniques for standard power ICs enabled a significant push of the switching frequency of DCDC converters and allowed several suppliers to introduce 4, 6, and 9MHz DCDCs that fit in a 6 mm^2 PCB area. Designers start realizing that scaling the power switches becomes a complex equation that not only includes conduction and switching losses of the power switch but also wasted reactive power that stores in the extrinsic parasitics.

Complex PMICs based on 0.18um and 0.13um extended drain processes offer higher capabilities toward 50MHz to 200MHz switching frequency but the challenge is quite similar regarding the criteria for better scaling the power switches, reducing the die area, reducing the electrical overstress and managing the extrinsic power losses. The presentation provides simple rules and a simple theory that help the designer realize an optimum device scaling.

The most concerning challenge from design point of view comes from the controller that has to be radically changed because of the short on time duration and the difficulty on using blanking techniques due to the non-damped HF ringing after each power switching event. The presentation highlights the crosstalk mechanisms and suggests ideas and techniques for solving such issues.

Bio:

Dr. Sami Ajram has 16 years experience in Electronics industry. He received his Ph.D. in 1998 from the University of Sciences and Technologies of Lille and pursued his research activities at the IEMN (http://www.iemn.univ-lille1.fr) pioneering 100MHz DCDC converter design based on IIIV power switches and PCB printed power inductors. He joined the ASIC department at ATMEL Rousset in 2000 where he led the design activity of HF clock synthesizers and low power front end sensors. In 2006, he joined Fairchild Semiconductor as Marketing Manager in charge of the development of High Frequency DCDC converters dedicated Dynamic Voltage Biasing of GSM / WCDMA RFPAs. He recently started SL3J SYSTEMS, a small design center focusing on Power Management and electronic solutions for handheld devices. He has 5 granted patents, published several papers and he received a Best Paper award from the IEEE PEL society in 2001.

Session 4a: Integrated Passives: Magnetics

Charles R. Sullivan, Maeve Duffy, Matthew Wilkowski, Florian Herrault, Saibal Roy

Inductors are key elements for dc-to-dc converters. For power supply on chip, inductors require novel and improved materials and integration techniques. In particular, multi-MHz, soft magnetic materials, deposited in a CMOS-compatible technique, are needed. The issues to be addressed in this session include:

- Magnetic integration – opportunities and challenges.
- Multi-MHz magnetics – thin film magnetic materials and deposition techniques.
- Material compatibility issues for integration on top of active silicon.
- Achievable power density and efficiency.

08:30 - 08:55	Saibal Roy TYNDALL NATIONAL INSTITUTE, IRELAND	Challenges in magnetics for PwrSoC - Development in high-frequency magnetics, materials, and integration
08:55 - 09:20	Donald .S. Gardner INTEL, USA	Integrated On-Chip Inductors Using Magnetic Material
09:20 - 09:45	Sarah Bedair US ARMY RESEARCH LABS, USA	Thin Film Piezotransformers for High Frequency Switched Mode Power Supplies
09:45 - 10:10	Florian Herrault GEORGIA TECH, USA	Lamination-Based Technology for High Performance Metallic Magnetic Cores
10:10 - 10:40	River Lee Hotel BREAKOUT ROOM Poster Session and Coffee/Tea Break	
10:40 – 11:05	Nian Sun NORTHEASTERN UNIVERSITY, USA	Low-Temperature Deposited Metallic Magnetic Films and Ferrite Films and Their Applications in Integrated RF Magnetic Devices
11:05 - 11:30	Matthew Wilkowski ENPIRION, USA	Magnetics on Wafer: Transitioning From Prototype to Manufacturing
11:30 - 12:30	Open Forum Discussion	"PwrSoC or Not"
12:30 - 13:30	River Lee Hotel Lunch	

Challenges in magnetics for PwrSoC - Development in high-frequency magnetics, materials and integration

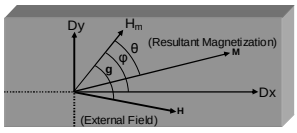
Saibal Roy

Tyndall National Institute, Ireland

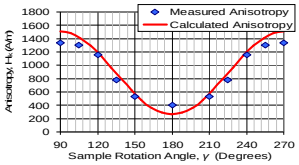
Abstract:

To enable the next-generation of highly-integratable, Power-RF magnetic components for on-chip converters, challenges must be overcome in various facets, such as device design, modelling, next generation magnetic materials and integration. Accurate modelling is the basis of any thorough understanding of the properties of a ferromagnetic thin-film, necessary to correctly predict the effects of thin-film deposition in a miniaturized device. Starting from characterisations of as-deposited materials, analytic models are applied to predict the effects of shape and thickness on the permeability of a structure. As well, the effects on inductance and loss at high-frequency of a conductive seed layer have been analytically modelled, which is of particular necessity for electrodeposited conformal thin-films.

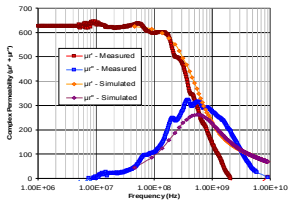
To miniaturise the inductive components, magnetic materials are required which exhibit low loss at high frequencies. The features of these materials must include a high anisotropy field, low hysteresis, high saturation flux densities and low eddy current losses. To meet these requirements novel nanostructured magnetic materials are being synthesised. We have considered a number of different electroplated, high-frequency nanostructured magnetic materials such as NiFe, CoNiFe, and CoP. Electroplating is compatible with the deposition of conformal and relatively thick layers i.e. several □m to 10's of □m to achieve required power density. However eddy current losses due to the lower resistivity of the electroplated films mean that thick layers will have an inferior frequency response. Typically, films are developed with pulse reverse plating to generate Co rich and Co deficient 'multi-nano-layers' having improved saturation magnetisation and better frequency response. The plating parameters have been optimised in order to produce a material with low loss and a high permeability of around 700 retained up to 103 MHz for a sample with a thickness of 1.7 □m, Bs of 1.2T and a resistivity of 136□Ohm cm. Some of the developed nano-materials have been integrated in the next generation of micro-inductors fabricated at Tyndall.



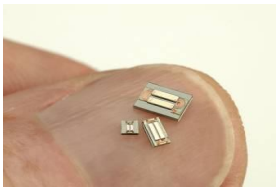
1a)



1b)



2a)



2b)

1a) Schematic representation of a magnetic thin-film core illustrating components of anisotropy
1b) Measured and simulated anisotropy of a thin-film CoP layer as a function of sample rotation
2a) Wide-band complex permeability of a 1.7μm thick layer of $Co_{91.5}P_{8.5}$ Measured and simulated including Cu seed layer
2b) Image of fabricated micro-inductors at Tyndall National Institute

Bio:

Dr. Saibal Roy is working as *Senior Scientist* in the Microsystems Centre of Tyndall National Institute, Cork, Ireland. He is Science Foundation Ireland Principal Investigator (SFI PI) and R&D leader in the Micropower - Nanomagnetics research area. He did his M.Sc. in Physics from the Indian Institute of Technology and received his Ph.D. working on advanced nanostructured materials from IACS in 1994. Since receiving his Ph.D, his professional experiences include 13 years academic and 3 years industrial research experiences; particularly he has served both in academia and industry as a senior scientist while leading research groups. Dr Roy's present research interests at Tyndall include how engineered nanostructures could be employed for potential benefits for micron scale devices from beyond Moore (BM) to More than Moore (MtM) scenario. Since joining the Tyndall National Institute, Dr. Roy was able to bring substantial (€ 3.28 Million) government and corporate research funding. Recently Dr. Roy has been honoured by the president of University College Cork (UCC) for licensing the patented technology to INTEL. Some of his published work featured in BBC technology news; Daily Mail; Sunday Telegraph and in American radio. His recent microfabricated high frequency inductor work has been described as a global benchmark for integrated magnetics by NXP (PHILIPS). Dr. Roy has supervised several PhD and Post doctoral fellows at Microelectronics Dept., University College Cork, and at Tyndall National Institute. He has served as a member of several programme committees, chaired sessions and delivered invited talks in many International Conferences / Research Institutes. So far, he has filed 5 international patents, written 1 book chapter and published 90 papers with h index 14.

Integrated On-Chip Inductors Using Magnetic Materials

Donald S. Gardner

Intel, USA

Abstract:

Rapidly increasing input current of microprocessors has resulted in rising costs and motherboard real estate occupied by the power delivery system. The current DC-DC converters on microprocessor motherboards are switching at or near KHz frequencies because of the strict efficiency requirements. Significantly higher frequency switching DC-DC converters in a CMOS process has been demonstrated for microprocessor power delivery [1-2]. The ultimate goal is to have a fully integrated converter with on-chip inductors to provide fine-grain power distribution and fast response time. On-chip inductors with magnetic material were integrated into both advanced 130 and 90 nm CMOS processes [3]. Increases in inductance of over 30 times corresponding to an inductance density of up to 1,700 nH/mm^2 were demonstrated [4], significantly greater than air-core and other on-chip inductors with magnetic material. With such improvements, the effects of eddy currents, skin effect, and proximity effect become clearly visible at higher frequencies. The CoZrTa was chosen for its good combination of high permeability, good high-temperature stability (>250 °C), high saturation magnetization, low magnetostriction, high resistivity, minimal hysteretic loss, and compatibility with silicon technology. The CoZrTa alloy can operate at frequencies up to 9.8 GHz, but trade-offs exist between frequency, inductance, and quality factor. Techniques are presented to extract a *sheet inductance* and examine the effects of magnetic vias (vias that allow complete closure in the magnetic flux) on the inductors. The DC resistance is also important for converters and was 0.04 ohms with quality factors of 8 when using thick copper metallization and thick CoZrTa (see Fig. 1).

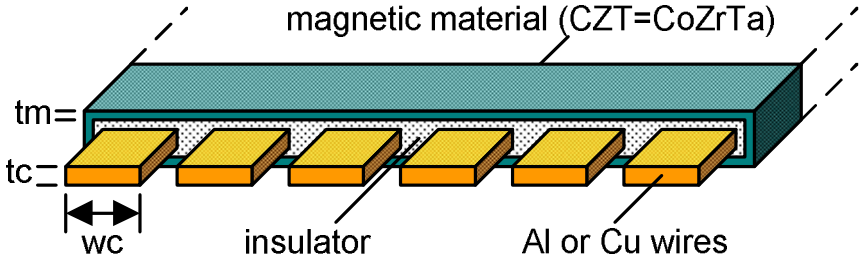


Fig. 1. Inductor structure with magnetic material

[1] **G. Schrom, *et al.*, "A 480-MHz, multi-phase interleaved buck DC-DC converter with hysteretic control," in *IEEE PESC*, 2004, pp. 4702-4707 Vol.6.**

[2] **G. Schrom, *et al.*, "A 100 MHz Eight-Phase Buck Converter Delivering 12A in 25mm2 Using Air-Core Inductors," in *Appl. Power Electronics Conf.*, 2007, pp. 727-730.**

[3] **D. S. Gardner, *et al.*, "Integrated on-chip inductors using magnetic material (invited)," *Journal of Applied Physics,* vol. 103, p. 07E927, Apr 2008.**

[4] **D. S. Gardner, *et al.*, "Review of On-Chip Inductor Structures With Magnetic Films," *IEEE Transactions on Magnetics,* vol. 45, pp. 4760-4766, Oct 2009.**

Bio:

Donald Gardner has been with Intel Corporation since 1991 and is currently a Principal Engineer in Intel Research. He received his PhD in Electrical Engineering from Stanford University and is currently a visiting scholar at Stanford. Donald is the inventor or co-inventor of 64 issued patents including for inductors using magnetic materials, reflowed copper for interconnections, layered aluminum interconnections, and embedded decoupling capacitors. He has received Intel's highest technical award "For Fundamentally Changing Platform Power Delivery with Integrated Voltage Regulators and Magnetic Inductors on CMOS". Donald has published over 135 electrical engineering, materials science and computer science papers in journals and conferences. He has received three Best Paper and Poster awards at international conferences and over 1,700 authors have cited his publications. Donald invented a copper technology and used it to fabricate the first working chip with copper-based interconnections at Intel, then published on copper size effects that has been referred to as the first study that showed surface scattering and grain size to be a potential interconnect scaling issue. He pioneered techniques for the study of metallic films using *in-situ* mechanical stress measurements that are widely cited in the literature. He also invented an Al alloy/Ti metallization for interconnections as part of his PhD thesis studies that was later widely used by industry in microchips. Donald has had appointments as a visiting research scientist at Hitachi Research Labs in Japan and also at Stanford University. He enjoys bringing new life to old technologies by blending them with new scientific technologies or integrating them with new materials. His current interests include future microprocessor technology, magnetic materials for inductors, silicon-based optoelectronic devices, new materials integration and nanostructure design and devices.

Thin Film Piezotransformers for High Frequency Switched Mode Power Supplies

Sarah Bedair

US Army Research Labs, USA

Abstract:

There is interest in power units with a single battery input and multiple output voltages for mobile micro-systems which are palm-sized and below [1]. Implementation of these units using larger COTS switched mode converters would cripple the entire system or limit functionality. Power converter size reduction motivates increasing the switching frequency (>20MHz), further reducing passive components' size. An array of thin film, high frequency piezoelectric resonant transformers (PTs), each of which is impedance matched to various loads, is envisioned (Fig.1-top). The predicted performance (AC/AC, AC/DC) of PTs in a power converter is evaluated where electrodes may be lithographically defined for load impedance-matching. Although there are challenges with thin film PTs including depoling and power handling, they present a promising, alternate technology to thin film magnetic transformers where the magnetic material losses limit high frequency implementation.

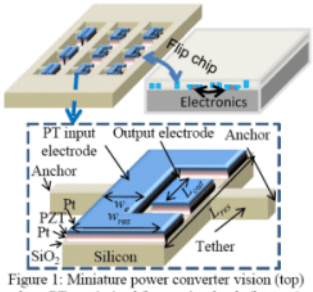


Figure 1: Miniature power converter vision (top) where PTs optimized for varying loads (bottom).

A performance model of a 21.4MHz (190µm x 40µm x 11µm) length extensional thin film PT using lead-zirconium-titanate is presented [2]. The extracted series motional resistance, Rx, inductance, Lr, and capacitance, Cr, (Q=2023) are 50Ω, 0.75mH and 74fF, respectively [3]. The input/output electrode coverage is used to tailor to various loads and specifications including efficiency and voltage boosts. The performance may be tailored through decreasing the output electrode area which is traded for input electrode coverage (Fig-1). Although this comes at a cost of reduced electromechanical coupling, the tradeoffs in efficiency and boosts over higher Rx are superior under higher resistive load, lower power regimes where voltage boosts are desired. Expected performances are shown for various output electrode coverage, 100%*Lout/Lres. For example, if 50% efficiency can be tolerated, voltage boosts (normalized power delivered) of 3.53(156µW/V2), 3.47(750µW/V2) and 2.80(2.6mW/V2) may be achieved by designing the output electrode coverage at 100%*Lout/Lres=1%, 5% and 20% for loads of 80, 16 and 3kΩ, respectively. Simulations of the PT in an AC/DC configuration (Table-1) at the optimal frequency show that boosts up to 8.2 at 29% efficiency and 0.4% ripple may be achieved.

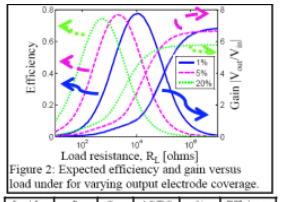


Figure 2: Expected efficiency and gain versus load under for varying output electrode coverage.

L_{out}/L_{res} x 100%	R_L [kΩ]	C_{filter} [nF]	AC/DC gain	% ripple	Efficiency
5 %	16	0.625	2.12	0.4	61%
1 %	80	0.125	2.17	0.4	61%
1 %	100	0.01	8.2	0.4	29%

Table 1: Expected performance (Pspice) with varying loads in a voltage doubler configuration.

[1] B. Morgan, S. S. Bedair, W. Nothwang, D. Arnold, C. Meyer, B. Bowers, A. Sopeju, C. Dougherty, X. Lin, and R. Bashirulla, "Micro-power requirements & conversion for autonomous Microsystems" NATO Specialist Meeting on Energy Technologies and Energy Management for Portable Power Systems for Military Applications, Slovenia, May 2009.

[2] S. S. Bedair, J. S. Pulskamp, B. Morgan, and R. G. Polcawich, "Performance model of electrode tailored thin film piezoelectric transformers for high frequency switched mode power supplies", PowerMEMS 2009, p. 435, Dec. 2009.

[3] H. Chandrahalim, S. A. Bhave, R. Polcawich, J. Pulskamp, D. Judy, R. Kaul, and M. Dubey, "Performance comparison of Pb(Zr0.52Ti0.48O3-only and Pb(Zr0.52Ti0.48O3-on-silicon resonators", Applied Physics Letters, 93, p. 233504-1 (2008).

Bio:

Sarah S. Bedair is an Electronics Engineer at the US Army Research Laboratory (ARL) in Adelphi, Maryland. Prior to joining ARL as an employee, she was an Oak Ridge Associated Universities (ORAU) Postdoctoral Fellow. She received her B.S. (2002) degree in Applied Sciences from the University of North Carolina at Chapel Hill. She also received her M.S. (2004) and Ph.D. (2008) degrees from Carnegie Mellon University from the Electrical and Computer Engineering Department where she conducted research on CMOS-MEMS gas chemical sensors and MEMS resonator / oscillators. During her studies she was awarded the UNC-Chapel Hill James D. Crawford Award (2002) and the Phillip and Marsha Dowd-ICES Fellowship (2005) and was a member of the Phi Beta Kappa and Eta Kappa Nu honor societies. She also received the 2010 Excellence in Federal Career - Rookie of the Year Award (Technical & Scientific) in addition to the 2009 Army Research Laboratory Research and Development Award. Her research interests include high frequency switched mode power supplies, high frequency piezoelectric resonators / transformers and the fabrication of integrated MEMS passives.

Lamination-Based Technology for High Performance Metallic Magnetic Cores

Florian Herrault

Georgia Tech, USA

Abstract:

Traditional passive elements in power conversion technologies, inductors and capacitors, are comprised of combinations of electrical conductors and materials of high magnetic permeability or high electric permittivity. Microelectromechanical (MEMS) researchers have been working on integrating these structures with integrated circuitry for many years. More recently, MEMS technology is being utilized to improve the performance of the materials themselves. This presentation will give an example of the use of MEMS to improve the properties of passive elements. Specifically, we have developed highly-laminated metallic magnetic alloys with suppressed eddy current losses for high-frequency power converters.

Iron alloys are used as magnetic core materials for inductors at low frequency, due in part to their extremely high value of saturation flux density. However, at higher frequencies (such as the continually increasing frequencies of switching converters), induced eddy current losses make the use of iron alloys challenging. Ferrites are therefore used due to their high electrical resistivity, even though they have low saturation flux density, resulting in relatively bulky inductor cores. Although laminations can be used to suppress eddy currents in iron cores (and are, at power delivery frequencies such as 60 Hz), the thickness of laminations necessary to suppress these currents at switcher frequencies extends into the submicron range. Using MEMS technology, we have developed approaches to realize iron alloy cores with macroscopic total thickness built from many submicron laminations. These cores allow the use of high saturation flux density iron materials in switching converters, potentially greatly shrinking the size of converter modules.

Bio:

Florian Herrault received the B.S. and M.S. degrees in physics and materials science and the Ph.D. degree in electrical and electronics engineering from the National Institute of Applied Sciences (INSA), Toulouse, France, in 2003, 2005, and 2009, respectively. However, his Ph.D. research was performed at Georgia Institute of Technology (Georgia Tech), Atlanta. He is currently a Research Engineer with the MicroSensors and MicroActuators Group, Georgia Tech. His current research interests include piezoelectric and electromagnetic actuators, small-scale power generation systems, high-performance magnetics for on-chip power converters, 3-D microelectromechanical systems (MEMS) fabrication, and MEMS-enabled thermal management devices.

Coupled Analysis of Magnetic Hysteresis and Electromagnetic Filed to Design On-Chip Planar Power Inductor

Masahiro Yamaguchi

Tohoku University, Japan

Abstract:
It is important for a planar power inductor for one-chip DC-DC converter to keep required AC inductance under superimposed DC field defined by DC output current. This paper proposes a new design methodology to endure coupled analysis of magnetic hysteresis model and numerical electromagnetic (EM) field simulation to realize more smaller inductor [1]. The Jiles-Atherton static hysteresis model [2] is employed.

A 5.0 x 5.0 x 0.5 mm^3 size planar rectangular spiral inductor is modeled in a commercial EM simulator (Maxwell 3D, Ansoft Co.), where 2-turn coil is sandwiched by 0.2mm thick MnZn ferrite layers, as shown in Fig. 1. The extracted J-A parameters are; Ms=1.46x10^-6, a=88, c=0.35, k=72 and alpha=0.00017. The conductor carries DC 1.1A and AC ripple 0.1Ap-p. Initially, permeability is assumed as non-linear and non-hysteretic with magnetic field intensity but uniform within the core space. After the first turn of the EM simulation, the permeability is replaced by position-dependent constants based on the J-A model depending on the simulated local flux density. This process was repeated for 9 times to be converged, as shown in Fig. 2. Flux density B on the coil (Cuboids 2 & 4) is B=0.43T and closely to saturation with relatively low permeability of ur=1600 whereas B=0.10T with ur=2300 at the edge of the inductor (Cuboids 1 & 5). Smaller inductor with improved DC-superimposed performance can be developed based on this method.

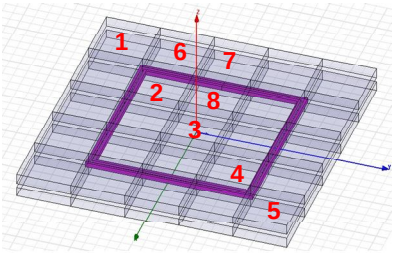


Fig. 1 Simulation model

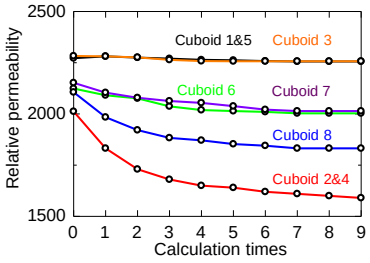


Fig. 2 Local permeability extraction as a result of the proposed coupled analysis

References

[1] M. Yamaguchi, T. Inagaki, M. Furuta, Y. Lu and S. Muroga, Joint European Magnetic Symposia(JEMS) 2010, Soft-A-oral 370, August 2010, Krakow, Poland.
[2] D. C. Jiles, et al., J. Mag. Mater., 61 (1986) 48.

Bio:

1984 Ph.D, Dept of Electrical Engineering, Tohoku University
1984 Assistant Professor, Dept of Electrical Engineering, Tohoku University
1991 Associate Professor, Research Institute of Electrical Communication, Tohoku University
2003 Professor, Dept of Electrical Engineering, Tohoku University

Academic Society Activities

- 2010 Editor of the IEEE Transactions on Magnetics – Conference (Intermag 2010)
- 2003-2009 Program Committee member of the IEEE International Magnetics Conference (Intermag 2003 -2009)
- 2005-2009 Member of the Board of Directors, Co-Editor-in-Chief, the Magnetics Society of Japan.
- 2002 – 2008, General Chairman of the IEEE Magnetics Society 1st to 7th International Workshop on the high frequency micromagnetic devices and materials
- 2007 IEEE Magnetics Society Japan-Sendai Chapter Chair

Awards

- 2010, 2004, 1986: Outstanding paper award, The Magnetics Society of Japan
- 2002 Award of the Society of promotion of Scientific measurements “High frequency magnetic field measurements using multilayer shielded-loop coil.”

Low-Temperature Deposited Metallic Magnetic Films and Ferrite Films and Their Applications in Integrated RF Magnetic Devices

Nian Sun

Northeastern University, USA

Abstract:

Integrated magnetic inductors, magnetic transformers and RF magnetic filters, etc. require soft magnetic material that can be deposited at low temperatures and have a high permeability, large saturation magnetization, high resistivity, high ferromagnetic resonance frequency, low loss tangent, etc. In this presentation, we will cover our research on different metallic magnetic films and ferrite films deposited at near room temperature and their applications in integrated RF magnetic devices. These metallic magnetic films include FeCoN, FeCoHf, and CoZrTa/Al_2O_3 multilayers, etc. High saturation magnetization FeCoN films with a saturation magnetization of 2.4 T were developed with a high relative permeability of 1000, high ferromagnetic resonance frequency of ~2 GHz and a low coercivity of ~1 Oe. In addition, we investigated the composition gradient sputtering method for depositing a series of $(Fe_xCo_{1-x})_{1-y}Hf_y$ alloy films with different Fe/Co atomic ratios and a small amount of Hf doping, which had a high saturation magnetization of 1.8 ~ 2.2 T. The compositional gradient of the Hf content in Fe-Co-Hf films led to a large in-plane anisotropy field of 200 ~ 500 Oe and a high ferromagnetic resonance frequency of > 7 GHz. We also investigated the magnetic properties of laminated CoZrTa/Al_2O_3 multilayer films with different periods and a total thickness of ~1.7μm, which show significantly enhanced performance at GHz frequency compared to single layer CoZrTa films with similar thickness. Besides metallic magnetic films, we also fabricated different NiZnCo-ferrite films with high μ_r in the GHz range through spin spray deposition at a low temperature of 90°C. The NiZn-ferrite films showed a low magnetic loss tangent $\tan\delta_m = \mu''/\mu'$ of ~0.025 between 1~1.5GHz, and a high ferromagnetic resonance frequency of 2.7 GHz. At the same time we have designed, fabricated and tested different RF magnetic devices such as inductors, transformers and filters which showed excellent performance.

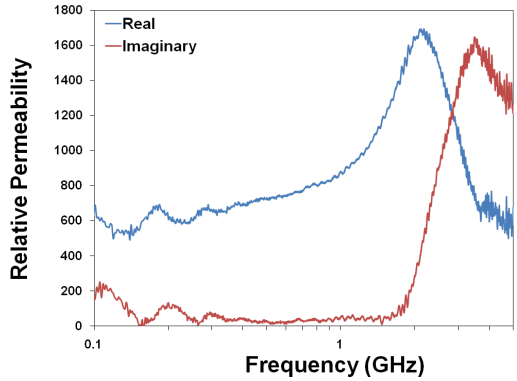


Fig. 1 Real and imaginary permeability spectrum of the CoZrTa/Al_2O_3 multilayers with a total thickness of 1.7 μm.

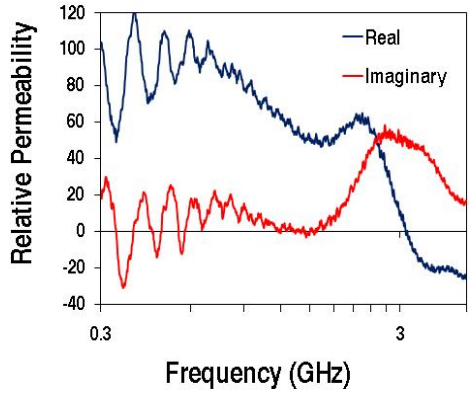


Fig. 2 Permeability spectrum of $Ni_{0.27}Zn_xFe_{2.73-x}O_4$ thin film with x=0.03.

Bio:

Nian Sun is an associate professor at the Electrical and Computer Engineering Department, Northeastern University. He received his Ph.D. degree from Stanford University. Prior to joining Northeastern University, he was a research scientist at IBM and Hitachi Global Storage Technologies between 2001~2004. Dr. Sun was the recipient of the NSF CAREER Award, ONR Young Investigator Award, USAF Summer Faculty Fellowship, and the first prize IDEMA Fellowship. His research interests include novel magnetic, ferroelectric and multiferroic microwave materials and devices such as antennas, filters, phase shifters, circulators, inductors, transformers, energy harvesting technologies, magnetic sensors, solar cell materials and devices, etc. He has over 80 publications and has >20 patents and patent disclosures.

Magnetics on Wafer: Transitioning From Prototype to Manufacturing

Matthew Wilkowski

Enpirion, USA

Abstract:

Integration of the magnetic function with the power switches and control function for dc-dc converters has progressed significantly over the past twenty years. There have been numerous publications citing reduction of physical size with acceptable power efficiencies for dc-dc converters with the magnetic function implemented on silicon. With the existence proofs in place for the various fabrication and design methodologies, it is time to drive further improvements in cost, technology acceptance by proliferation of device designs into various applications and availability of certification and field reliability data etc., through commercialization of products.

The cost effective and successful commercialization of magnetics on silicon requires trade-offs between the obvious technical physical and electrical improvements and the constraints of the currently available manufacturing processes with an eye towards future process capabilities as market acceptance warrants the required investments.

Critical performance criteria such as small signal inductance, series resistance, saturation current and large signal ac power loss can be defined for inductor performance for specific levels of device performance as well as for specific combinations of materials, geometries and fabrication technologies. However these levels of performance must be sustainable through the temperature and physical stresses of wafer manufacturing process and the device packaging process. This requires verification of the critical inductor parameters through all stages of the manufacturing process as well as through industry recognized JEDEC device level reliability characterization programs in an effort to identify potential variations and shifts and their appropriate countermeasures.

The insights obtained from manufacturing and reliability characterization of the first generation of commercial devices can be applied to more complex second generation devices which involve greater levels of integration of materials and geometries.

Bio:

Matt Wilkowski is Director of Magnetics and Components Engineering for Enpirion. In this role, Matt is responsible for the design and analysis, characterization and verification as well as reliability characterization of new and existing inductor designs and manufacturing technologies in PSIP and PwrSoC packages. Prior to Enpirion, Matt was Director of Component Engineering for Tyco Power Systems. During his tenure at Power Systems, Matt was responsible for the design and development of new magnetic structures for standardization throughout a broad product portfolio from first concepts based on electrical and physical requirements through manufacturing realization.
Matt has been involved with the design, characterization and qualification of discrete and integrated magnetic components for more than thirty (30) years. Throughout this involvement, Matt has been an active member of various professional organizations relative to magnetic and packaging. These include the Electronic Transformer Technical Thrust of the PELs Power Systems and Components Technical Committee, IEC TC 51 Magnetic Components and Ferrite Materials, PELs Standards Committee and PSMA's Magnetics and Packaging committees.

Session 4b: Integrated Passives: Capacitators

Session Co-Chairs: Seth Sanders, Magali Brunet

Capacitors are fundamentally essential passive devices for any DC-DC converter. For power supply on chip, key measures are energy density, power density, parasitic losses, reliability, and compatibility with standard or emerging fabrication and packaging technologies. In particular, 3-D structures, nano-materials, and otherwise high quality films withhigh dielectric constant (K) and high breakdown field are needed to be deposited in CMOS-compatible techniques. In the case of integration-in-package, more flexibility with materials, processes, and substrates is possible, and solutions that take advantage of such flexibility are of interest.

The issues to be addressed in this session include:

- Silicon compatible capacitor materials and technologies.
- High energy density and high power density capacitor technologies suitable for low-cost co-integration or co-packaging with silicon.
- Magnetic and capacitor integration - opportunities and challenges.

13:30 - 13:55	Catherine Bunel IPDIA, FRANCE	3D capacitors: Manufacturing and applications
13:55 - 14:20	Magali Brunet LAAS CNRS, TOULOUSE, FRANCE	Ultra-high power carbon-based microsupercapacitors
14:20 - 14:45	Mihaela Popovici IMEC, BELGIUM	ALD Strontium Titanates and their characterization
14:45 - 15:10	Stephen O'Brien CITY COLLEGE OF NEW YORK, USA	Printed components and large-area capacitators
15:10 - 15:40	River Lee Hotel BREAKOUT ROOM Poster Session and Coffee/Tea Break	

3D Capacitators: Manufacturing and Applications

Catherine Bunel

IPDIA, France

Abstract:

As the market for miniaturized devices continues to grow and expand , it has become evident that IPDIA has made the right choice to consider the 3D passive integration as a top priority. This IPD (Integrated Passive Device) provider is focusing its activities on 3D passive integration in Silicon with an advanced and unique technology called "PICS" (Passive Integrated Connective Substrate). High-density trench capacitors, MIM capacitors, resistors, high-Q inductors, Zener diodes are implemented in Silicon enabling their integration in various packaging technologies with active devices suitable for high power applications. In this paper, the PICS capacitors performance will be discussed and compared to the standard MLCC capacitors . The outstanding characteristics of IPDIA Silicon Capacitors , in terms of integration , electrical performance and reliability will be illustrated by several examples of applications. The technology roadmap towards higher densities will conclude the paper.

Bio:

Catherine started her career in Philips in 1985 .She worked in several departments in Process and Product Development and Manufacturing taking a new position every 4 years .

She was assigned as the Process Development Manager in Philips and then in NXP Semiconductors since 2004. . She drove innovation and developed the new technologies to create future "System-in-Package", providing the support to the manufacturing and external manufacturing in Asia as soon as needed.

She is now. The R&D director of IPDIA leading the innovation of Integrated Passive Devices for several market segments such as Medical, Industrial, Communications and Lighting . She manages a team of 20 Engineers and she drives the development of new technologies in partnership with European labs and Research institutes.

Catherine holds a degree from *Ecole Supérieure d'Ingénieurs en Electronique et Electrotechnique* (ESIEE) in Paris

Ultra-High Power Carbon-Based Microsupercapacitators

Magali Brunet

LAAS CNRS, Toulouse, France

Abstract:

Supercapacitors also called Electrochemical Double Layer Capacitors (EDLCs), with a charge storage mechanism purely electrostatic are intermediate components between batteries and capacitors. In storage applications, despite lower energy density, they have the advantages over batteries of long life time (millions of cycles) and provide fast charge/discharge rates in a wide potential window and temperature range. In power applications, supercapacitors, despite their lower power than standard capacitors, have a high capacitance density that can make them interesting as energy reservoirs in various power integrated circuits.

We present here the integration of supercapacitors onto silicon substrate elaborated using electrophoretic deposition (EPD) of activated and onion-like carbon. We show that thanks to the design of the micro-electrodes, the carbon nanomaterial and the absence of organic binder and polymer separator in the process, the micro-devices can reach very high power densities (close to 1kW/cm^3), of the same order of electrolytic capacitors while keeping a high enough energy density (10 mWh/cm^3). These performance will be compared to actually available 3D integrated capacitors.

Bio:

Magali Brunet obtained her PhD in Microelectronics Engineering in 2003, at the National Microelectronic Research Centre (NMRC, now Tyndall Institute), Cork, Ireland. After a post-doc in Leti-CEA in Grenoble in 2004, she joined the Laboratory of Analysis and Architecture of Systems (LAAS – CNRS), Toulouse, as a research scientist in the group Integration of Power Management Systems. Her research is focused on integrated passive components for power electronics (micro-inductors, micro-transformers, micro-capacitors) and for energy storage (micro-supercapacitors). She is looking in particular at the micro-fabrication technologies and the integration of new materials for these applications.

ALD Strontium Titanates and Their Characterization

Mihaela Popovici

IMEC, Belgium

Abstract:

Strontium titanate ($Sr_xTi_{1-x}O_y$) perovskite films are highly attractive as high-k dielectric materials for dynamic random access memory (DRAM) applications in Metal-Insulator-Metal (MIM) capacitors due to their high dielectric constant allowing a high storage capacity. In view of 3-D structures envisaged for these applications to achieve ultra-high storage density, the most suitable technique is atomic layer deposition (ALD), which through its self-limiting growth mechanism ensures a conformal coverage. Strontium titanates (STO) can be obtained over a composition range between 45 and 67 % Sr using for example $Sr(^tBu_3Cp)_2$ and $Ti(OMe)_4$, as precursors. The cubic lattice cell can be modified by incorporation of an excess of Ti or Sr atoms varying Sr:Ti pulse ratio during film growth [1]. After crystallization anneals at temperatures above 550^{o}C typically a perovskite structure is formed. Growth of the STO thin films was done on metals such as TiN, Ru or Pt that form the MIM bottom electrode. The films were investigated via X-ray diffraction (XRD), transmission electron microscopy (TEM), Rutherford backscattering spectrometry (RBS), X-ray photoelectron spectroscopy (XPS) and time-of-flight secondary ion-mass-spectrometry (TOFSIMS). The electrical performance of crystalline strontium titanates with different compositions was investigated via C-V and I-V measurements of MIM capacitor stacks using Pt or TiN as top electrodes. The dielectric constant (extracted from film thickness series) and leakage current strongly depend on the Sr/(Sr+Ti) content [2]. The leakage current density can be significantly lowered (without compromising the high capacitance densities) by stacking multiple dielectric layers, e.g. the use of a seed layer (thin STO layer crystallized before the ''bulk'' STO deposition) or a multilayer such as $SrTiO_3/GdAlO_3/SrTiO_3$ [3].

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2. N. Menou, M. Popovici, S. Clima, K. Opsomer, W. Polspoel, B. Kaczer, G. Rampelberg, K. Tomida, M.A. Pawlak, C. Detavernier, D. Pierreux, J. Swerts, J. W. Maes, D. Manger, M. Badylevich, V.V. Afanas'ev, T. Conard, P. Favia, H. Bender, B. Brijs, S. Van Elshocht, G. Pourtois, D.J. Wouters, S. Biesemans, J.A. Kittl, *Composition influence on the physical and electrical properties of $Sr_xTi_{1-x}O_y$-based metal-insulator-metal capacitors prepared by atomic layer deposition using TiN bottom electrodes*, ***Journal of Applied Physics***,106(9) (**2009**) 094101
3. N. Menou, M. Popovici, K. Opsomer, B. Kaczer, M.A. Pawlak, C. Adelmann, A. Franquet, P. Favia, H. Bender, C. Detavernier, S. Van Elshocht, D.J. Wouters, S. Biesemans, J.A. Kittl, *Seed Layer and Multistack Approaches to Reduce Leakage in $SrTiO_3$-Based Metal-Insulator-Metal Capacitors Using TiN Bottom Electrode*, ***Japanese Journal of Applied Physics***, 49 (4) (**2010**), 04DD01

Bio:

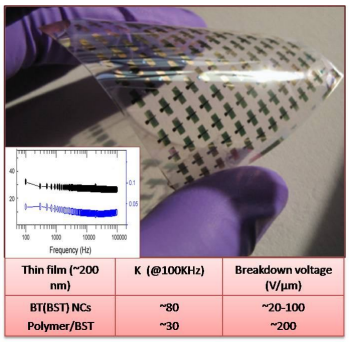
Dr. Mihaela Popovici is currently researcher of the Thin Films Scientific Group at imec, Belgium. Her area of research includes atomic layer deposition of high-k oxides and metal gates. She is involved in designing metal-insulator-metal capacitors stacks, responsible for the dielectric materials development and physical characterization. She has a BS and MS in chemical engineering and received her PhD in Materials Science and Engineering in 2004, at the "Politehnica" University of Timisoara, Romania. After a two years post-doctoral stage in Philips Research Netherlands (Photonic Materials and Devices) she joined imec in 2007. Past research interests comprise magnetic nanocomposites and optical thin films development via sol-gel chemistry. She has authored or co-authored over 30 papers published in international journals and conference proceedings and holds 6 patents.

Printed Components and Large-Area Capacitators

Stephen O'Brien

City College of New York, USA

Abstract:



Thin film (~200 nm)	K (@100KHz)	Breakdown voltage (V/μm)
BT(BST) NCs	~80	~20-100
Polymer/BST	~30	~200

Production of complex metal oxides for high k dielectric applications, either as gate dielectrics or in capacitor technology is commonplace. Requirements for integrated electronics are generally towards miniaturization, higher permittivity and dielectric strength, and lower loss/leakage. New sources of energy production (e.g. renewables, intermittant) will also require advances in energy storage and power conversion. Assembly of dielectric nanoparticles into thin films is a highly attractive means to produce composites with improved performance and tunability as a function of size, composition and structure. One of the major processing challenges is conversion of the nanoparticle building block into a reliable thin film device. Essential to this approach is an understanding of the chemical components and interface chemistry, combined with an ability to integrate them into thin films that have uniform and characteristic electrical properties. An attractive feature of this pursuit is the possibility to adapt large area deposition approaches, for example preparing printed capacitors. Our current process allows us to prepare capacitor thin films or gate dielectrics (particle/polymer composites) with dielectric constants k in the range of 10-60, over 100 kHz-1 MHz. Such methods aim to circumnavigate the need to develop complex fabrication tools normally associated with semiconductor manufacturing, and to make the process cheap and scalable.

Bio:

Steve O'Brien is an established academic researcher in nanotechnology, with expertise in inorganic materials chemistry and materials science and engineering. He works on Nanoparticle synthesis and self-assembly. He is associate professor of chemistry at City University of New York, City College, and a faculty member of the CUNY Energy Institute. He is published in over 75 articles, and invented new methods for the preparation of electronic materials for the semiconductor industry and other areas of nanotechnology, with several pending patents. He was a Lindemann Post-Doctoral Fellow and an NSF CAREER recipient. Steve has a D.Phil from Oxford University.

Session 5: Converter Topologies and Control Systems for PwrSoC

Session Co-Chairs: Ray Foley, Yan-Fei Liu, Eduard Alarcon

This session addresses power train circuits and controller design for on-chip and other power supplies targeting miniaturization or integration with loads. The session will present the latest advances in converter circuit topologies, including high-frequency, multi-phase or multi-level configurations, resonant power converters operating at RF frequencies, switched-capacitor circuits, topologies that enable ultra-high density miniaturization etc., as well as control systems enabling efficient operation at high frequencies. Light load efficiency issues will also be considered in the context of battery performance in mobile applications.

15:40 – 16:05	Rais Miftakhutdinov TEXAS INSTRUMENTS, USA	PSiP and PwrSoC Based Opportunities and Solutions for High Power Systems
16:05 - 16:30	Eby Friedman UNIVERSITY OF ROCHESTER, USA	Small Area Power Converter for Application to Distributed On-Chip Power Delivery
16:30 - 16:55	Olivier Trescases UNIVERSITY OF TORONTO, CANADA	Gate-Charge Recovery for Light-Load Efficiency Improvement in High-Frequency DC-DC Converters
18:30 - 23:00	Trident Hotel, Kinsale Workshop Banquet	

PSiP and PwrSoC Based Opportunities and Solutions for High Power Systems

Rais Miftakhutdunov

Texas Instruments, USA

Abstract:

While the integration trend in low-power hand-held devices is very well pronounced and established, the benefits of PSiP and PwrSoC technologies are not so obvious for relatively high power non-isolated and isolated power systems. This topic considers PSiP and PwrSoC based functional blocks, optimal topologies and control strategies as part of power system with the output power up to few kW.

One example is high end micro-processors and DSPs where power supply integration into the package allows significant cost and number of decoupling capacitors saving by better handling extremely high di/dt transients of such digital processors. In case of isolated converters and inverters, the PSiP and PwrSoC technologies can find place as bias supplies for MOSFET/IGBT drivers and isolated active current and voltage sensors. Additionally, integrated magnetics can be part of conceptually loss-less resonant drivers for power switches.

Major challenges for PSiP and PwrSoC in the outlined applications are relatively high operating voltage up to 20V, currents up to tens amps in case of power supplies for microprocessors, and, in many cases, the need for the electrical isolation. The topic describes few possible solutions to address these challenges.

Bio:

Dr. Rais Miftakhutdinov is a technologist and Senior Member of Technical Staff at Texas Instruments Inc., currently focusing into the area of power supply controller and driver ICs for high efficiency and power density power systems. He has graduated from Moscow State Aviation Institute, where in 1997 was awarded PhD Degree in Electrical Engineering without interrupting his work in the industry. Rais Miftakhutdinov shares with the audience his more than 30 years experience in Power Electronics field where he has been awarded 12 patents and published more than 40 papers, including presentations at Power Systems World, APEC, PESC and others.

Small Area Power Converter for Application to Distributed On-Chip Power Delivery

Eby Friedman

University of Rochester, USA

Abstract:

The presentation is composed of three parts. First, a recently manufactured test circuit of a small on-chip point-of-load voltage converter will be described. This active filter-based circuit is a hybrid combination of a switching DC-DC voltage converter and a linear voltage regulator, exploiting active circuitry rather than the bulky passive devices typically used in a buck converter. The voltage regulator can supply over 140 mA current while exhibiting high current efficiency greater than 99% and achieves fast load regulation (72 ns) while requiring only 0.026 mm2 on-chip area. This circuit provides a means for distributing multiple local power supplies across an integrated circuit while providing high current efficiency. In the second part, simultaneous co-placement of these point-of-load power supplies with on-chip decoupling capacitors to improve overall signal integrity of the power grid will be discussed and the many highly complex interactions among the power supplies, decoupling capacitors, and load circuitry will be reviewed.
In the third part, a distributed voltage regulator designed and manufactured in a 3-D IC technology will be briefly reviewed.

Bio:

Eby G. Friedman is a Distinguished Professor at the University of Rochester and a Visiting Professor at the Technion - Israel Institute of Technology. His research is in high performance synchronous digital and mixed-signal microelectronic circuit design. He is the author of almost 400 papers and book chapters and thirteen books in the fields of high speed and low power CMOS design techniques, high speed interconnect, and synchronous clock and power distribution networks. He previously was the Editor-in-Chief of the IEEE Transactions on Very Large Scale Integration (VLSI) Systems, a recipient of the University of Rochester Graduate Teaching Award, and a College of Engineering Teaching Excellence Award. Dr. Friedman is a Senior Fulbright Fellow and an IEEE Fellow.

Gate-Charge Recovery for Light-Load Efficiency Improvement in High-Frequency DC-DC Converters

Olivier Trescases

University of Toronto, Canada

Abstract:

Dynamic power consumption in the gate-drive circuitry limits the light-load efficiency of high-frequency, low-power integrated dc-dc converters. In this talk a power MOSFET gate-charge recycling technique is introduced, where the output capacitor is used to store a portion of the gate charge between switching events. The charge is transferred between the gate of power MOSFET and the output capacitor using transmission gates with precise closed-loop timing control. The timing of the charge transfer is regulated using a simple digital delay-locked loop in order to compensate for temperature and process variations. The converter is designed in 0.13 µm CMOS technology, and simulation results show a total saving of 25% in gate driver power and an overall efficiency improvement of 5%. The converter operates at 20 MHz and converts 2.5 V to 0.8 - 1.6 V at up to 300 mA.

Bio:

Olivier Trescases is an Assistant Professor in the Department of Electrical and Computer Engineering at the University of Toronto, where he received his Ph.D. degree in 2007. Dr. Trescases' past research topics include high-efficiency switch-mode power supplies, quasi-resonant dc-dc converters, dynamic voltage/frequency scaling in VLSI circuits, all-digital class-D audio amplifiers and motor drives for hybrid electric vehicles. From 2007 to 2008, Dr. Trescases worked as a concept engineer at the high-integration group at Infineon Technologies AG. He has received two IEEE best-paper awards in 2003 and 2006. Dr. Trescases' current research group focuses on high-efficiency power converters for industrial, automotive, aerospace and renewable energy applications.

Session 5: Converter Topologies and Control Systems for PwrSoC

Session Co-Chairs: Ray Foley, Yan-Fei Liu, Eduard Alarcon

08:30 - 08:55	David Anderson NATIONAL SEMICONDUCTOR, USA	Compact, Cost-effective, Efficient Power: Is there a sweet-spot for integration?
08:55 - 09:20	Seth Sanders UC BERKELEY, USA	Integrated Power Conversion - The Switched Capacitor Approach
09:20 - 09:45	Gabriel A. Rincón-Mora GEORGIA TECH, USA	Energy-Harvesting Switching Converter ICs

Compact, Cost-effective, Efficient Power: Is there a sweet-spot for integration?

David Anderson

National Semiconductor, USA

Abstract:

The move to higher switching frequencies facilitates the use of physically smaller filter components that are a requirement for full integration of switching converters, but introduces numerous challenges for controlling frequency-dependent loss mechanisms. This paper will review the capabilities and limitations of integrated power inductors and will examine the application of various circuit control topologies to explore the possibility of a sweet-spot for a cost-effective yet efficient PSOC.

Bio:

David Anderson is a senior technologist, working in National's research laboratory on advanced power management development. He received his BSc (Hons) degree from Edinburgh University in 1968. He has spent a long and distinguished career in the electronics business and often provides unique insights on the various panels and forums he participates in as technology guru.
David's first role was Design Engineer at Nuclear Enterprises in Edinburgh, working with a team developing a portable X-ray spectrometer for mineralogy application. After Nuclear, he joined Ferranti Electronics to work on telemetry systems and later joined Siemens in Munich, Germany where he developed analog integrated circuits for audio, video and camera applications.
Returning to Scotland in 1978, David joined National Semiconductor in Greenock, where he developed audio ICs, including analog Telecom and Dolby Noise Reduction ICs. In 1991 he moved to National's headquarters in Silicon Valley as Design Manager for Automotive IC Development and was responsible for the development of over 40 automotive IC's.
In 1996, he joined Semtech Corporation as Vice President of Engineering where he established and grew Semtech's Power Management Development Group before moving to a start-up company, Volterra, in 2001 as Vice President of Engineering. Volterra has pioneered integrated switchers utilizing mixed-signal control topologies and achieved industry-leading power density for fully integrated power switchers utilized in computers and POL [point-of-load] regulators.
In 2004, David returned to his roots at National Semiconductor in Santa Clara, California as Chief Technologist for Power Management. Working in NS Labs , National's research and design laboratory, David's current focus is on advanced semiconductor and power control topologies that show potential to transform existing IC systems. In this role he is involved in a wide gamut of power circuits that range from milliwatts to kilowatts, with a strong emphasis on alternative energy systems.

Integrated Power Conversion - The Switched Capacitor Approach

Seth Sanders

UC Berkeley, USA

Abstract:

Technical merits and challenges of the switched capacitor approach to dc-dc power conversion are discussed. A detailed analysis enabling a strategic comparison among switched-capacitor converter topologies and also enabling comparison of switched-capacitor topologies with conventional magnetic topologies is outlined. The analysis framework allows a quantitative comparison of the various popular power conversion circuits in terms of their utilization of switch technology and also their utilization of energy storage devices (eg. capacitors, inductors). Significantly, the analysis shows that for a wide range of conversion applications, switched capacitor converters should be expected to outperform the conventional buck, boost, and transformer-based converters with respect to component utilization. Since switched capacitor converters contain no magnetic devices, they are well suited to integration in a range of CMOS processes. Further, since devices can be effectively stacked, extended voltage operation can be realized with low voltage processes.

However, switched capacitor converters also present a number of challenges in voltage regulation and in ripple performance. Design strategies to meet these challenges, and to exploit the excellent potential of switched capacitor dc-dc converters are outlined. Examples of on-die multi-core VR conversion, board-level point-of-load conversion, and ultra-low-power on-die conversion for wireless sensor applications will be discussed.

Bio:

Seth R. Sanders is a Professor of Electrical Engineering in the Department of Electrical Engineering and Computer Sciences at the University of California, Berkeley. He received S.B. degrees (1981) in Electrical Engineering and Physics, and the S.M. (1985) and Ph.D. (1989) degrees in Electrical Engineering from the Massachusetts Institute of Technology, Cambridge. Following an early experience as a Design Engineer at the Honeywell Test Instruments Division in 1981-83, he joined the UC Berkeley faculty in 1989. His research interests are in high-frequency power conversion circuits and components, in design and control of electric machine systems, and in nonlinear circuit and system theory as related to the power electronics field. Dr. Sanders is presently or has recently been active in supervising research projects in the areas of flywheel energy storage, novel electric machine design, renewable energy, and digital pulse-width modulation strategies and associated IC designs for power conversion applications. During the 1992-1993 academic year, he was on industrial leave with National Semiconductor, Santa Clara, CA. Dr. Sanders received the NSF Young Investigator Award in 1993 and multiple Best Paper Awards from the IEEE Power Electronics and the IEEE Industry Applications Societies. He has served as Chair of the IEEE Technical Committee on Computers in Power Electronics, and as a Member-At-Large of the IEEE PELS Adcom. He is an IEEE Fellow.

More information available at www.power.eecs.berkeley.edu

Energy-Harvesting Switching Converter ICs

Gabriel A. Rincón-Mora

Georgia Tech, USA

Abstract:

Wireless microsensors and other miniaturized electronics cannot only monitor and better manage power consumption in emerging large-scale applications for space, military, medical, agricultural, and consumer markets but also add energy-saving and performance-enhancing intelligence to old, expensive, and difficult-to-replace infrastructures. The energy these small smart devices store, however, is often insufficient to power the functions they incorporate (such as telemetry, interface, processing, and others) for extended periods, and replacing or recharging the batteries of hundreds of networked nodes is prohibitively expensive. Harvesting energy from the surrounding environment to continually replenish a battery is therefore an appealing alternative, even if the development of relevant technologies today is at its infancy. This seminar illustrates the means by which microelectronic semiconductor switching converters can harness energy and condition power from miniaturized piezoelectric and electrostatic transducers that transform kinetic energy in vibrations into the electrical domain. The presentation introduces and describes how power-conditioning stages and control circuits draw and direct derived energy into a battery and shows the experimental results obtained from integrated-circuit (IC) prototypes.

Bio:

Prof. Rincón-Mora worked for TI in '94-'03, was Adjunct Professor for Georgia Tech (GT) in '99-'01, and is a tenured professor at GT since '01. His scholarly products include 8 books, 1 book chapter, over 125 scientific publications, 27 patents, over 26 commercial chips, and over 55 speaking engagements. He received the "National Hispanic in Technology Award," "Charles E. Perry Visionary Award," a "Commendation Certificate" from the Lieutenant Governor of California, IEEE Service Award, and Robins Air Force Base's "Orgullo Hispano" and "Hispanic Heritage" awards and was inducted into GT's "Council of Outstanding Young Engineering Alumni." He is an IET Fellow, IEEE Distinguished Lecturer; TCAS II Associate Editor; JOLPE Editorial Board Member, and SSCS-CASS Chapter Chair.

Session 6: Monolithic Integration Vs System in Package

Session Co-Chair: Arnold Arnold, Baoxing Chen, Cian Ó'Mathúna

In conclusion, this session will try to place the power supply on a chip (PwrSoC) in perspective by exploring the entire landscape of power supply integration. Designs and market overview will be presented ranging from "discretes in a package" (PSiP) to "system on a chip" (SoC) in which power supply function is an integral portion of the system. The benefits and the limitations of each level of integration will be explored. Figures of merit will be considered to allow objective integration route characterisation for specific applications. The session will also address issues of performance, efficiency, thermal management, EMC, reliability, cost, flexibility, afforded by the implementations

09:45 - 10:10	Arnold Alderman ANAGENESIS, USA	Overview of product integration
10:10 - 10:35	Bill Liu ANALOG DEVICES, USA	Advanced Power Management Techniques for Portable Applications
10:35 - 11:05	River Lee Hotel BREAKOUT ROOM Coffee/Tea Break	
11:05 - 11:40	Dion Manessis FRAUNHOFER INSTITUTE, GERMANY	Embedded Power Dies for System in Package
11:40 - 12:05	Brian Molloy INFINEON TECHNOLOGIES, USA	Power SoC Vs SiP – Competitive Challenges in High-Volume Applications
12:05 - 12:30	Ashraf Lofti ENPIRION, USA	PowerSoC Commercialisation – Market Drivers and Key Technology Enablers
12:30 - 12:55	Satoshi Matsumoto KYUSHU INSTITUTE OF TECHNOLOGY, JAPAN	Future Power Electronics for Realizing Sustaining Society
12:55 - 13:10	Close of Workshop	
13:10 - 14:15	River Lee Hotel Lunch	

Overview of Product Integration

Arnold Alderman

Anagenesis, USA

Abstract:

Meant to be the introductory paper for session 6, this presentation provides a summarized overview of the product development the market drivers enabling these devices to become mainstream integrated power converter products. PSiP device performance trends and events will be discussed covering the past 2 years since the PowerSoC 2008 Workshop. These trends include improvements in current density, efficiency, switching frequency, cost reduction, higher functionality multiple conversion, and other key parameters. This presentation provides a wide perspective of the spectrum of variously integrated power management devices. The complementary role of devices such as power ICs, power management units (PMUs) and power PMUs (PMUs with power transistors) and system on chip (SoC) are put in perspective. This dissertation gives the attendee insight regarding future product trends including the expected advent of high voltage (off-line) ac-dc conversion integrated devices and introduction of fully integrated PwrSoC devices. Present PSiP and PwrSoC market size and expected market growth will be discussed highlighting possible key market enhancement and barriers. Material for this presentation is based on extensive market research conducted over the past 5 years. Former work in this area of study was published by PSMA in 2007 and 2009 with highlights and updates presented at PowerSoC 2008 and APEC 2009 and APEC 2010. The author is presently conducting research to update previous work. This most recent information will be included in the presentation.

Bio:

Not available at the time of going to print

Advanced Power Management Techniques for Portable Applications

Bill Liu

Analog Devices, USA

Abstract:

Power management has been the largest market of analog integrated circuits. With the conflict of the exponentially increased data processing and limited improved battery capacity, efficient energy management and further power reduction is rising to be the most important consideration for portable applications. The mass, public portable devices lead to the requirement of light weight, small volume, low cost as well as long battery lifetime, which challenges the system power management. This paper will try to cover several advanced power management IC techniques for portable applications. (a) The single-inductor multiple-output (SIMO) solution provides multiple regulated outputs by a single inductor. It has the merit of reducing external inductors. (b) Higher switching frequency results in smaller filter inductor and capacitor, furthermore the bulky passive components can shrink to be integrated on chip. (c) Nowadays electronic systems are so complex that a smart partitioning of battery energy management and power conversion is required. This drives the development of power management units (PMU), which are well defined integrated mixed signal circuits for specific customers. (d) The pursuit of high efficient power usage in each block level circuitry leads to more power management functions being embedded inside chip, e.g. audio amplifiers. (e) The solution of system in package (SiP) could optimize the trade-off among process, performance, board space and cost for many power management systems. This talk will also address and explore its future development and opportunities.

Bio:

Works in Analog Devices as director of Shanghai Design Center and Communication Infrastructure Asia Technical Groups with over 15 years experience in Semiconductor industry, mainly focus on analog and mixed signal product developments including linear amplifier, data converter, power management and high efficient switching amplifier and MEMS ASIC… published several patents, international conference papers and served as sub chairman, panelist and technical committee member in international conferences like A-SSCC, ISSCC and APCCAS…Profound international working experience in Japan, US and China, worked in TI, Burr-Brown and Fujitsu before.

Embedded Power Dies for System in Package

Dion Manessis

Fraunhofer IZM, Germany

Abstract:

Embedding of semiconductor chips into organic substrates allows a very high degree of miniaturisation by stacking multiple layers of embedded components. Among its merits, it provides superior electrical performance by short and geometrically well controlled interconnects as well as a homogeneous mechanical environment for the chips and thus resulting in superior reliability. By exploiting conventional PCB manufacturing practises, this paper will show how component embedding can be implemented in industrial 18"x24" organic substrate formats for large scale system-in-package manufacturing. Embedding allows to have conductors not only under but also over a component leading to a 3-dimensional packaging also on top of the embedded components. The component can be electrically connected to the top or to the bottom conductive layer or to both of them, e.g. in case of power ICs with contacts on both sides. Such embedding approach is very beneficial in the case of power Dies for enhanced heat dissipation from the backside of the power die. The Embedding process flow will be thoroughly discussed and results on embedded power MOS dies having a thickness in the range of 150-300µm will be shown. The resultant system-in-packages with embedded power die can be ultimately assembled as conventional SMD packages.

Bio:

Dion Manessis possesses M.Sc and Ph.D degrees in Materials Science from Stevens Institute of Technology, USA and has also acquired technology and project management certificate degrees from Cornell University. Since 2001, he is working as Principal Technology Scientist in Fraunhofer IZM Berlin in close collaboration with the Microperipheric Research Center of Technical University Berlin. He is project manager for EU and industrial projects. His main R&D interests lie on Flip chip and Wafer Level CSP bumping, solder balling, printing of polymeric materials for wafer level packaging. The last 4 years, he has focused on component embedding technology implementation for manufacturing of miniature system-in-packages for advanced technological applications.

Power SoC Vs SiP – Competitive Challenges in High-Volume Applications

Brian Molloy

Infineon Technologies, USA

Abstract:

The focus at Infineon is energy efficiency, system miniaturization in high volume applications such as computing. Ongoing research into PowerSiP and PowerSoC is focused on a right-fit approach. Further miniaturization is compelling in certain applications but may be overkill for others. High volume manufacturability with acceptable yield must be a consideration from the concept stage to satisfy any high-volume market. Many key markets have multi source requirements where unique single source solutions will find resistance. This presentation will discuss how these factors are taken into consideration at Infineon.

Bio:

Brian Molloy is Director of Business Development for Infineon's low-voltage DCDC controller and integrated power stage business. He received his BE (Hons) degree from the National University of Ireland (Galway) in 1987. Brian's background is in mixed-signal power ASIC and ASSP development covering over 20 years in Design, Applications and now Business Development roles with Digital Equipment Corporation, Quantum, Seagate, MicroLinear, ST and now Infineon. Brian's current focus is on DCDC for the PC and Server market.

PowerSoC Commercialisation – Market Drivers and Key Technology Enablers

Ashraf Lofti

Enpirion, USA

Abstract:

Enpirion continues to be a pioneer in commercializing PowerSoC technology, for this presentation, Enpirion will highlight corporate advancements towards a full power system on a chip (PwrSoC) from Enpirion's historical and future perspectives. With a strong focus on market applications driving its adoption as well as manufacturing enablement, the design, development and production of a PwrSoC is a continuously evolving effort towards the ultimate fully-monolithic single chip power system. Enpirion will present significant milestones in this development path and how it intends to implement commercialization efforts for many years to come.

Bio:

Ashraf Lofti is the President, Chief Technology Officer and Founder of Enpirion. Ashraf has been continuously involved in research, design and commercial development in the power field for over 20 years
Prior to founding Enpirion, he led the power management R&D effort at Bell Laboratories as Director of Power Management Research (Lucent/Agere). During this period he laid the vision for a research effort with the ambitious goal of creating the technology pieces needed to create, for the first time, true power management on a single chip.
These efforts combined multiple disciplines from power semiconductors, RF circuits, high-speed power topologies, magnetic design to package technology in a highly coordinated development to achieve a commercially viable yet breakthrough technology enabling high performance in a single chip in an economical manner. Prior to that as Department Head, Power Systems Research, his development efforts in power systems applications ranged from high-density dc/dc power modules to planar high density magnetics to custom dc/dc converters to high power rectifiers and battery plants for telecommunications energy supplies. These technologies and others formed the cornerstone for many product lines delivered by Lucent's (previously AT&T's) Power Systems Division driving highly differentiated products in the market place commanding leadership market share and revenues. He also held various engineering and instructor positions at Virginia Tech and Cairo University.

Future Power Electronics for Realising Sustaining Society

Satoshi Matsumoto

Kyushu Institute of Technology, Japan

Abstract:

The climate changes bring the human race a lot of disadvantages. Japan is positively grappling with this problem. For example, in 2006, the Japanese Ministry of Economy, Trade, and Industrial issued its "Ultra-long-term Energy Vision in Japan" which stresses the importance from fossil fuel based energy sources to electrical energy. The effective use of electric energy is one of the most promising candidates to confront climate change. In such situation, the power electronics becomes a key technique. In future power electronics, we will utilize a lot of numbers of miniaturized DC-DC converters to use the electrical energy effectively. In this paper, I describe the example of the effective use of a electrical energy using a lot of number of the DC-DC converters. In addition, I also talk about how we can implement the semiconductor devices with passive devices on the same chip based on my past researches.

Bio:

Satoshi Matsumoto received the B.S., M.S., and Ph.D. degrees in applied chemistry from Waseda University, Tokyo, Japan, in 1982, 1984, and 1996, respectively.
In 1984, he joined Nippon Telegraph and Telephone Corporation (NTT) LSI Laboratories. In 1993, he transferred to NTT Energy and Environments Systems Laboratories, where he has been engaged in research and development of analog high frequency devices and circuits, and environment friendly power electronics. In 2010, he moved to Kyushu Institute of Technology, Fukuoka, Japan. His current interests are power devices and IC's and environment friendly power electronics.

Poster Session

Session Co-Chairs: Brice Jamieson, Ray Foley, Florian Herrault, Magali Brunet, Maeve Duffy, Yan-Fei Liu, José Cobos

As a part of the workshop discussions, an open call for posters was announced for PwrSoC 2010 to allow researchers from both industry and academic institutions to take part and highlight their research and contributions to this dynamic and growing field.

Rizwan Bashirullah UNIVERSITY OF FLORIDA USA	A 100MHz 8x step-up dc-dc converter in 130nm 1.2V CMOS process with micro-fabricated air-core inductor
Tom Van Breussegem K.U. LEUVEN Belgium	Fully Integrated Switched-Capacitor DC-DC Converters in Standard CMOS: The Key- Enabler for on-chip Power Management
Christopher D. Meyer UNIVERSITY OF FLORIDA USA	Multilayer Micromachined Air-Core Power Inductors and Transformers
Di Yao DARTMOUTH COLLEGE USA	Performance and Fabrication of On-Chip Power Inductors Using Multi-Layer Co-Zr-O Films
Joyce Mullenix STANFORD UNIVERSITY USA	Effect of anisotropic permeability on a closed-core inductor
Malal Bathily ST MICROELECTRONICS France	Improvement of the efficiency of HF DC/DC converters by resonant gate drivers
Miriam del Viejo UNIVERSIDAD POLITÉCNICA DE MADRID Spain	Output cap reduction thanks to a fast and novel control technique: V2IC control
Maeve Duffy NUI GALWAY Ireland	Potential for improved efficiency of PSoC with parallel micro-inductors
Mike Wens K.U. LEUVEN Belgium	Fully-Integrated Inductive DC-DC converters in Standard CMOS
Pradeep K. Peter INDIAN SPACE RESEARCH ORGANIZATION India	Portable PV Fed Maximum Power Point Tracking Switched Capacitor Battery Charger
Xavier Branca ST ERICSSON / INSA-LYON France	A novel simple-inductance, double-output step-down converter for embedded audio applications

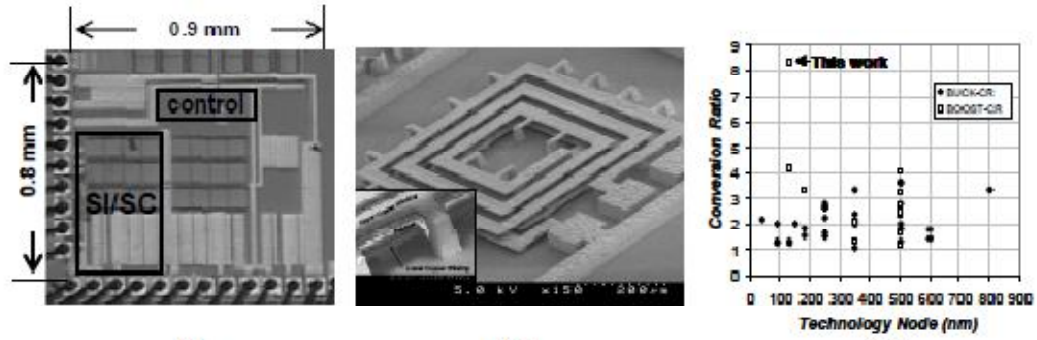
Magali Brunet LAAS-CNRS France	Integrated LC filter on silicon for DC-DC converter applications
Jason Hannon UNIVERSITY COLLEGE CORK Ireland	Design of a DC-DC Converter with Co-Packaged Inductor
Patrick Shea UNIVERSITY OF CENTRAL FLORIDA USA	A 150V Power SOI LDMOS Transistor for MHz Frequency Switching Applications
Donagh O'Mahony TYNDALL NATIONAL INSTITUTE Ireland	GaN Schottky diodes for high operating temperature electronics
James Mooney UNIVERSITY OF LIMERICK Ireland	Digital Control of Multi-Rail DC-DC Converter Systems with Non-Integer Switching Frequency Ratios
Jeffrey Godsell TYNDALL NATIONAL INSTITUTE Ireland	High-Frequency Complex Permeability Analysis of CoNiFe ferromagnetic thin films for integrated passives
Shunpu Li TYNDALL NATIONAL INSTITUTE Ireland	Engineered anisotropy in modulated magnetic films for miniaturized devices
Ningning Wang Tyndall National Institute Ireland	20MHz DC-DC Converter with Integrated Inductor on Si
Ningning Wang Tyndall National Institute Ireland	AN IMPROVED CALCULATION METHOD FOR AC COPPER LOSSES IN POWER INDUCTORS INTEGRATED ON SILICON
Aileen O'Mahony Tyndall National Institute Ireland	Structural and Electrical Analysis of Interface Control Layers of MgO or Al2O3 Deposited by Atomic Layer Deposition, at the high-K/III-V Interface

A 100MHz 8x step-up dc-dc converter in 130nm 1.2V CMOS process with micro-fabricated air-core inductor

*Lin Xue, Christopher Meyer, Christopher Dougherty, *Sarah Bedair, *Brian Morgan, David P. Arnold and Rizwan Bashirullah*

Department of Electrical and Computer Eng., University of Florida, Gainesville, FL 32611
**U.S. Army Research Laboratory, 2800 Powder Mill Road, Adelphi, MD 20783.*
E-mail: {brian.morgan6@arl.army.mil darnold@ufl.edu rizwan@ufl.edu}

The development of sensors and autonomous platforms for mobile microsystems is driving the need for cubic-millimeter, milligram-scale power conversion and management systems capable of boosting 10-100 mW of power from a battery source (<4 V) to >20 V. No power conversion systems exist today that can accomplish such a feat in the required mm3/mg-scale without crippling the mobility of the scaled platform. Herein we report on progress towards the development of hybrid boost converter that is intended to provide high voltage gain from a battery source in an ultra-miniature form factor. By utilizing the fine feature sizes of modern processes readily available in CMOS technologies, and combining micromachined, thick-copper, high-frequency inductors, designers can leverage high switching frequency and thus the desired minimization of passives. However, since conventional step-up converters are not suitable for integration in low voltage processes because of breakdown problems, one of the primary challenges then becomes that of enabling the creation and processing of large voltages within an inherently voltage limited process. Moreover, the step up ratio of traditional switch-mode boost converters is generally limited by realizable duty cycle and parasitic losses of the inductor and power train stages. The boost converter presented herein utilizes a hybrid switched-inductor and switched capacitor topology with integrated schottky barrier diodes and composite stacked nMOS synchronous switch capable of sustaining nearly 8x the rated voltage using high-voltage devices developed in standard low voltage CMOS processes without additional masking steps.
The converter here is fabricated in a 130 nm 1.2V CMOS process and operates at ~100 MHz using a microfabricated air-core inductor. From a 1.2V source, the converter achieves a maximum conversion ratio of ~8 and peak efficiency of 37% for 7 V output and 1.6 mA load.



(a) (b) (c)

A 100MHz step-up dc-dc converter in 130nm CMOS: (a) die photo (b) microfabricated air-core inductor and (c) comparison with recently published integrated dc-dc converters.

Fully Integrated Switched-Capacitor DC-DC Converters in Standard CMOS: The Key- Enabler for on-chip Power Management

Tom Van Breussegem, Hans Meyvaert and Michiel Steyaert
ESAT – MICAS K.U.Leuven – Kasteelpark Arenberg 10 Belgium

Discrete type DC-DC converters are expensive and bulky due to the external components they require. Therefore it is a reasonable approach to integrate DC-DC converters on-chip in order to achieve a cost-effective solution and to integrate power management features on-chip. Integration of inductive converters turned out to be quite cumbersome. The efficiency of these converters is penalized by high parasitic series resistance of the CMOS integrated air coil inductors and the parasitic coupling between inductor windings and the silicon substrate. As a consequence they achieve only limited peak efficiencies. Integrated capacitors instead are available with higher quality factors and make converters based only on these passives a promising research topic.

Research at the MICAS group has been conducted to demonstrate the potential of switched-capacitor DC-DC converters. Several fully integrated prototypes have been developed as proof of concept and research is conducted on modeling and control of these converters. Integration of DC-DC converters in standard CMOS technology requires thorough knowledge of the process and additional improvements on circuit and layout level. A short overview of 3 most recent realizations:
A prototype of a voltage doubler has shown good ripple characteristics by using a multiphase switching approach. This approach achieved a ripple smaller than 0.5% of the output voltage, a peak efficiency of 82% and maximum output power of 4.7mW. (Chip picture in Fig. 1)
Mobile applications face a battery voltage drop as it gets empty. To maintain a constant output voltage, the conversion ratio will therefore have to follow the decline of input voltage. Switched-capacitor converter topologies however have fixed conversion ratios. A prototype has been designed to incorporate reconfiguration between topologies to achieve good efficiency over a wider input range. A peak efficiency of 88% was achieved. (Chip picture in Fig. 1)
Another prototype has been designed to facilitate a large conversion ratio from 12V to 70V. This design is implemented as a 10 stage Dickson ladder delivering 320mW at 85.5% efficiency per stage.
We will demonstrate our recent findings and present our recent developments in the field of fully integrated DC-DC converters.

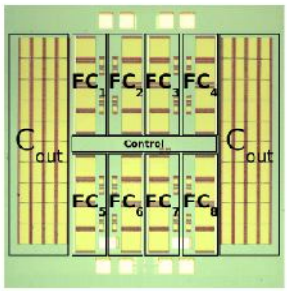


Fig. 1. A 82% Efficiency 0.5% Ripple 16-Phase Fully Integrated Capacitive Voltage Doubler in 130nm CMOS

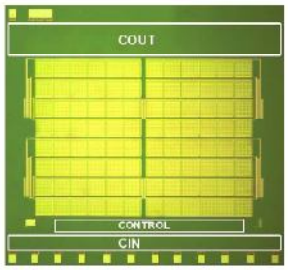


Fig 2. A Fully Integrated Cockcroft Capacitive DC DC converter in 90nm CMOS

Multilayer Micromachined Air-Core Power Inductors and Transformers

Christopher D. Meyer1, Sarah S. Bedair2, Brian C. Morgan2, and David P. Arnold1
1Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL 32611
2U.S. Army Research Laboratory, Adelphi, MD 20783

This work presents high-inductance-density air-core power inductors and transformers to enable miniature integrated switching power converters operating in the 100–500 MHz frequency range. Air-core magnetic passives are attractive at these very high frequencies for avoiding the core losses that are often prohibitively large in ferromagnetic materials above several MHz [1].
However, typical air-core integrated passives have inductances and quality factors that are too low for efficient conversion in the MHz range [2]. Increasing the inductance density of these devices requires a large number of tightly spaced turns, which leads detrimentally to greater series resistance and shunt capacitance [3].

In this work, surface micromachining of the structures, such as the inductor depicted in Fig. 1, has addressed these challenges through the plating of 10-µm-thick copper windings for low resistance, vertical stacking of metal windings for increased mutual inductance coupling, and removal of dielectric material between windings for low parasitic capacitance. Inductors of various geometries were fabricated with sizes ranging from 1–4 mm2, ac inductance densities over 100 nH/mm2, and peak quality factors up to 21.

The microtransformers employed nested and interleaved winding schemes for strong magnetic flux coupling of the primary and secondary coils. The layout of these transformers provided not only high coupling but also the opportunity to create transformers with turns ratios greater than unity for voltage or current gain. Three transformer designs were fabricated and tested, all with areas 2.25 mm2 and primary inductances of 47 nH but with variable secondary inductances to yield voltage gains from 1:1 up to 1:3.5. Load-dependent transformer performance characteristics were predicted from the 50-Ω-load measurements using network analysis techniques. The 1:3.5 step-up transformer projected a maximum efficiency of 78% around 150 MHz, while the isolation transformer had a projected 91% efficiency with a voltage gain of 0.95.

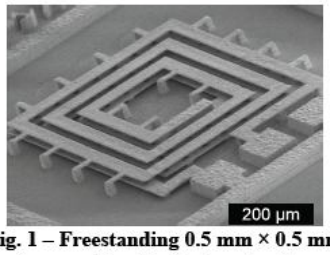


Fig. 1 – Freestanding 0.5 mm × 0.5 mm micromachined inductor structure.

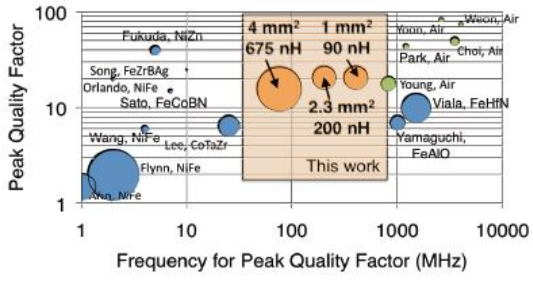


Fig. 2 – Comparison of microfabricated inductors. Bubble size is proportional to inductance density.

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Performance and Fabrication of On-Chip Power Inductors Using Multi-Layer Co-Zr-O Films

Di Yao, Jizheng Qiu, and Charles R. Sullivan
Thayer School of Engineering at Dartmouth, Hanover, NH, USA
charles.r.sullivan@dartmouth.edu

Efficient and compact on-chip power converters could enable higher performance and new capabilities in many electronic systems. We report progress on high-power-density, low-loss very-high-frequency microfabricated power inductors, as required by integrated power converter designs.
For high-current applications such as powering digital systems, V-groove inductors (Fig. 1) provide low dc resistance and high current capability [1]-[5]. Nano-granular Co-Zr-O magnetic materials provide the moderate permeability and needed for power inductors along with low losses at frequencies up to 100 MHz or more, while exhibiting saturation flux density much higher than that of ferrites [6],[7].

Performance of previous V-groove inductors was limited by the 5 MHz converter switching frequency used [4],[5] and by degradation of the magnetic material properties for the films deposited on the sloping sides of V-grooves [8]. We report newly fabricated inductors that overcome these limitations. Techniqes in [8] are used to achieve good magnetic properties on sloping substrates. Loss prediction methods from [9] are used to design multi-layer magnetic material with well controlled eddy-current loss, including displacement current effects, for the high switching frequencies (10 to 100 MHz) enabled by implementation of power switches in modern CMOS. Fabrication of set of inductors embedded in a silicon wafer has recently been completed; testing will begin shortly. Calculated performance predictions for an example application of the fabricated inductors are shown in Table I.

application of the fabricated inductors are shown in Table I.

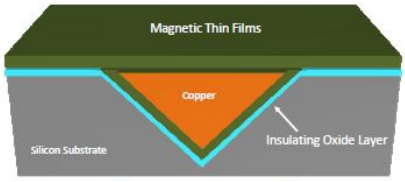

Fig. 1. Schematic of a V-groove inductor

TABLE I
CALCULATED PERFORMANCE OF FABRICATED INDUCTORS IN POWER CONVERTER APPLICATION

Converter dc voltage	7 V in; 3.3 V out
Output current	3.9 A
Switching Frequency	50 MHz
Inductance	8 nH
V-groove depth	200 μm
DC resistance	6 mΩ
ESR (50 MHz)	24 mΩ
Q (50 MHz)	107
Inductor efficiency	> 99%
Inductor power density	8 W/mm^2

For applications with a larger conversion ratio, such a a 12-V input, 1-V output converter, alternative circuit designs such as tapped-inductor buck converters and related topologies offer advantages for semiconductor devices stresses. We are also developing inductor designs for these circuits using similar magnetics technology. Fabrication approaches and optimized designs for these devices will also be presented.

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in *12th IEEE Workshop on Control and Modeling for Power Electronics*, 2010.

Effect of anisotropic permeability on a closed-core inductor

Joyce Mullenix[1] and Shan X. Wang[1,2]
[1.] Dept. of Electrical Engineering, Stanford University, Stanford, CA 94305, USA
[2.] Dept. of Materials Science and Engineering, Stanford University, Stanford, CA 94305, USA

This study demonstrated the effect of uniaxially anisotropic permeability on an integrated solenoid inductor with a closed magnetic path. While a closed magnetic path should enhance the inductance of a magnetic device, the closure is dependent on the magnetic permeability being isotropic. If the magnetic material is anisotropic, it will prevent the flux from being contained within the magnetic core, effectively forming an air-gap and breaking the magnetic path.

Devices were fabricated on silicon substrate with 5µm thick copper conductor. The magnetic core was 2µm thick Co90Ta5Zr5 (at. %), with a relative permeability of approximately 600 at 10MHz. The inductors were modeled using the Ansoft MaxwellTM software.

The measured inductance of the two series connected inductors with the closed core was 62nH at 10MHz, while inductors without the closed magnetic path was 49nH. Although the closed-core device in Fig. 1(a) out-performed the device in Fig. 1(b), the increased magnetic length could account for this difference. The length of the magnetic film for the closed-core device is longer, increasing the effective permeability and thus inductance.

Further simulations were conducted on the closed-core device using Maxwell, comparing uniaxially anisotropic and isotropic permeabilities, and both devices with an air-gap at each end. Fig. 2 depicts the inductance of the four scenarios as a function of film thickness. At very small film thickness, the benefit of adding a closed magnetic path was small regardless of the anisotropy. As the film thickness increased, the inductance of the device with anisotropic permeability began to roll off, while the inductance of the other film continued to increase linearly. The performance of the device with anisotropic permeability was identical to the devices with air-gaps. This indicated that uniaxial anisotropic magnetic material could not be used to create a closed magnetic path.

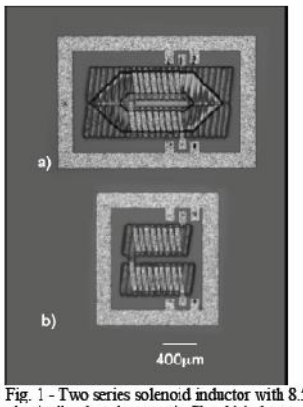


Fig. 1 - Two series solenoid inductor with 8.5 turns on each inductor, a) inductor with a physically closed magnetic film, b) inductor with two magnetically separated cores.

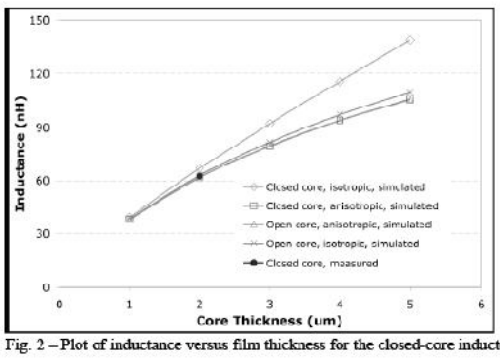
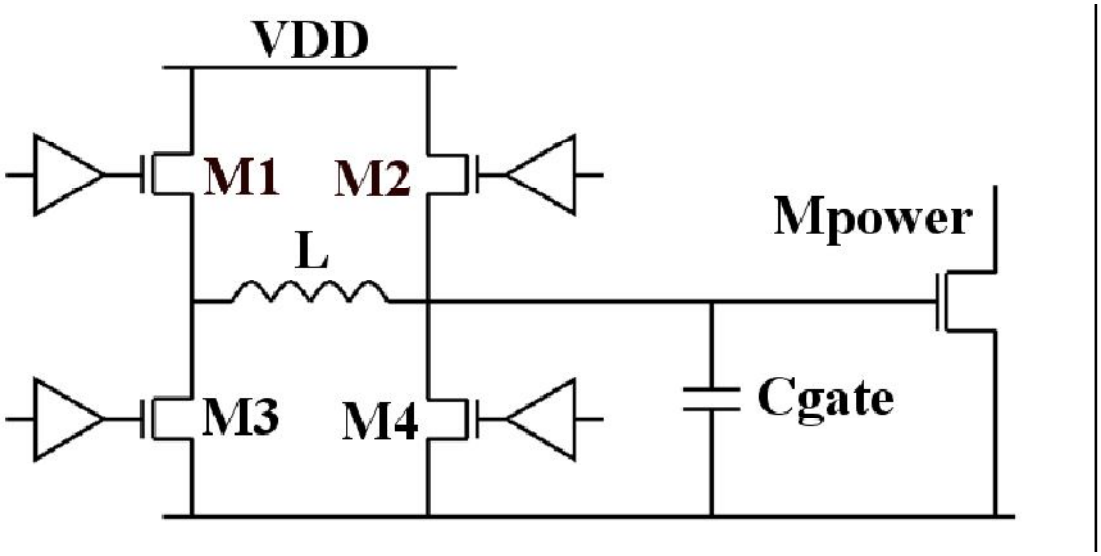


Fig. 2 – Plot of inductance versus film thickness for the closed-core inductor.

Improvement of the efficiency of HF DC/DC convertersby resonant gate drivers

Malal Bathily, Frederic Hasbani and Bruno Allard
STMicroelectronics (Crolles) 850 rue Jean Monnet 38926 Crolles, France

This work introduces a resonant gate driver for the improvement of the efficiency of high frequency DC/DC converters. The proposed resonant gate driver performs a local recycling of the switching energy of the gate of the power transistors (see figure). Thanks to this energy recovery the total switching losses of the DC/DC converter are reduced and the efficiency is improved, especially in light load condition. The driver's elements are designed to minimize the switching losses compared to what is obtained with a conventional driver, i.e. a chain of inverters. An analytical model is built to compare both types of driver. Based on this model two buck converters switching at 200 MHz have been designed: one with the conventional driver and the other one with the proposed resonant gate driver. Experimental results indicate a reduction by 30% of the switching losses thanks to the resonant gate drivers. An improvement of the efficiency by as much as 5% in low power range is obtained. The inductors of the drivers are integrated on-chip with the converters.



Output cap reduction thanks to a fast and novel control technique:

V^2I_C control

M. del Viejo; P. Alou; J. A. Oliver; O. García; J. A. Cobos.
Centro de Electrónica Industrial. Universidad Politécnica de Madrid
Madrid, Spain

The reduction of the output capacitance, $C_{out,}$ is critical to facilitate converter integration. High switching frequency is mandatory to integrate low power DC/DC converters. However, although high switching frequency would theoretically allow a voltage mode control with very high bandwidth, parasitic effects and robustness make very complex to achieve bandwidths higher than 1MHz, and the actual bandwidth is normally in the order of hundreds of kHz. Since the output cap is related to the bandwidth, bulky caps are necessarily used in spite of the high frequency used.

This work presents a fast control to dramatically improve the dynamic response of high frequency DC/DC converters, even with low bandwidth (tens of kHz). The proposed V2IC control is very appropriate for very high switching frequency (5MHz) integrated converters that need to achieve fast dynamic response under both load and reference voltage steps. **It enables the reduction of the required output capacitors (10µF instead of 50µF** for the considered application) with a robust and low bandwidth (50kHz) solution. The results are comparable to a standard voltage mode control with a bandwidth of about 1MHz for the same specifications, which is really complex to achieve since the resonance frequency of the output capacitors is very close.

The V2IC control presented in this work is based on two loops, a fast internal loop that provides fast dynamic response under load and reference voltage steps and a slow external loop provides accurate steady state regulation. The control signal (Ctrl) obtained in the fast loop is the weighted addition of the estimation of the output capacitor current, the error between the reference voltage and the output voltage and a compensating slope to avoid sub-harmonic oscillations. The control proposed is based on a peak mode control of this control signal (Ctrl).
The advantages of this control are: 1) constant switching frequency, 2) fast dynamic response under load and reference voltage steps allowing the reduction of the output capacitance, 3) low sensitivity to parasitic effects and sensor mismatches thanks to the slope compensation and 4) it is easy to be integrated on silicon with the rest of the power converter.

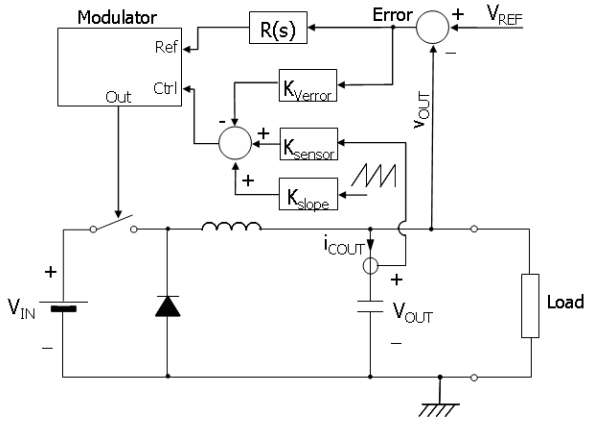


Figure 1: Proposed control: V^2I_C control.

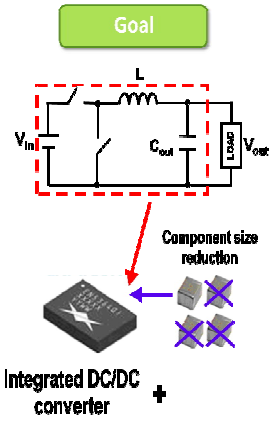


Figure 2: Goal: Reduction of required output capacitors.

Potential for improved efficiency of PSoC with parallel micro-inductors

M. Duffy[1], N. Wang[2]
Power Electronics Research Centre, NUI Galway, Ireland
Tyndall National Institute, Cork, Ireland

The main motivation for integrating magnetics on silicon is to reduce the inductance of interconnects so that tighter voltage regulation can be achieved to support the low voltages targeted in future microprocessors. However, due to the limitations of manufacturing technologies for producing large conductors and effective magnetic cores, the performance of inductors is limited, particularly in terms of the levels of efficiency achievable. This is exacerbated by high frequency operation as required for component miniaturization and for addressing the trade-off between efficiency and transient response rate.

A method for improving the light-load efficiency of high-current, high-frequency DC/DC converters has been proposed, which involves switching out of parallel inductor paths. To date, the method has been demonstrated using planar magnetics. It is shown that while there is little or no improvement in inductor loss, the increase in effective inductance per phase combined with a separation of MOSFET connections produces significant savings in MOSFET losses.

The aim of this work is to illustrate how the method described translates to power converters based on magnetics on silicon. The method involves replacing each inductor in a buck circuit with several smaller inductors connected in parallel. The parallel inductors are designed to provide the same functionality as a single inductor under full load and the rated current is shared equally between them; i.e. for n_L parallel inductors, the inductance of each parallel inductor is n_L times higher than the single inductor and it is rated to handle $1/n_L$ of the total current. Therefore when the load current reduces, it is possible to successively switch out the parallel inductors in turn.

In doing so, the effective inductance acting in the circuit is increased, so that the total AC ripple current is reduced and components of core and AC winding losses are also reduced. Note that each parallel inductor needs to have a separate connection to its own high and low side MOSFETs, but the current rating of the individual MOSFETs is $1/n_L$ that of the equivalent single MOSFET. Therefore, in addition to potential improvements in inductor losses, more significant MOSFET losses are also reduced by switching out of parallel paths.

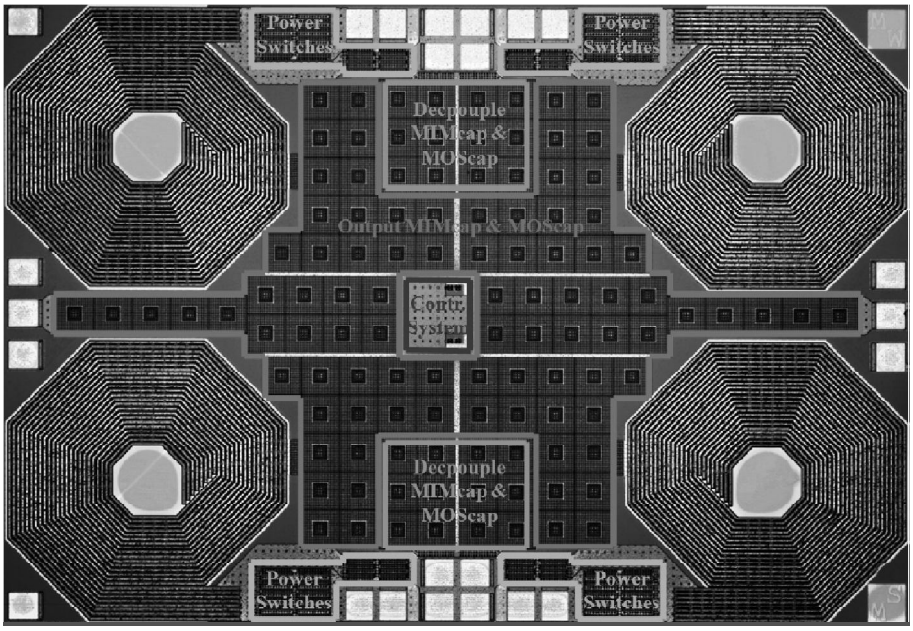
Results of a design study will be presented where detailed models of losses in the inductors and MOSFETs will be applied to predict how much the efficiency vs. load is improved in a typical PSoC application. Different combinations of connections between the inductors and MOSFETs will be considered, along with different numbers of parallel paths.

Fully-Integrated Inductive DC-DC converters in Standard CMOS

Mike Wens, Hans Meyvaert and Michiel Steyaert
ESAT-MICAS K.U.Leuven – Kasteelpark Arenberg 10 Belgium

CMOS technology scaling due to Moore's law enables ever more complex systems to be integrated on a single chip die, reducing the processing cost. Advanced, miniaturized, wireless and battery operated user applications are the direct result of this fact. A System on Chip (SoC) requires analog and digital circuitry to be combined, usually in a native digital CMOS technology. These technologies are optimized for the integration of large digital circuits, using very small transistors and low supply voltages to reduce the power consumption. Integrating the (switched-mode) power supply on the same SoC will thus reduce both the number of external components and the PCB footprint area.

The power consumption of battery operated applications needs to be minimized, since this maximizes the autonomy. Therefore on-chip linear voltage regulators, will not be an option, due to the excess power losses at high output power. Therefore, switched-mode voltage converters are a better choice in terms of power conversion efficiency. However, the poor Q-factors of on-chip passives (L, C) and their low values (nH, nF) pose many difficulties, potentially compromising the power conversion efficiency.
Combing both the concepts of full-integration and achieving a maximal (overall) power conversion efficiency, is the key to success. Moreover, to minimize the costs, the power density of the fully-integrated DC-DC converter is to be maximized. Research at the MICAS (KULeuven) laboratories has pointed out that these goals are best achieved by means of inductive DC-DC converters.
Above statements are proven through various practical realizations and measurements. These designs include, boost and buck converters, both single and multi-phase, without needing any external components. Power densities of over 200mW/mm² are achieved and an efficiency enhancement over linear regulators up to 23% is observed. These results prove the fully-integrated feasibility and practical use of inductive DC-DC converters.



A Fully-Integrated 800mW 4-Phase Step-Down Converter in 130nm CMOS

Portable PV Fed Maximum Power Point Tracking Switched Capacitor Battery Charger

Pradeep K. Peter, Indian Space Research Organization, India (pkp@isac.gov.in)
Vivek Agarwal, Indian Institute of Technology Bombay, India (agarwal@ee.iitb.ac.in)

Almost all hand held electronic devices like cameras, handy cams, simputers etc are battery powered. It is very desirable to maximize the time between the need for recharging the battery. Using batteries of larger capacity is an option, but one has to pay the prize of increased weight, size and cost. A single chip, PV fed, Switched Capacitor (SC) dc-dc converter based battery charger with built in Maximum Power Point (MPP) tracking facility, that may be integrated into the hand held device, for topping up the battery and thus prolonging battery life, is proposed here. Since SC dc-dc converters do not use magnetics, they are very well suited for miniaturization and realization in a single monolithic IC. Fig. 1 shows the block diagram of this system which is capable of charging a battery with a full charge voltage $V_B \leq 8V$. The PV array is made of five 2cm×4cm series connected high efficiency (≈28%) multi junction solar cells which are pasted to the exposed surface of the hand held device. At normal incidence and 28°C, each cell has a V_{oc} and V_{mp} of 2.57V and 2.25V respectively and I_{sc} and I_{mp} of 110mA and 105mA respectively. Thus the PV array's V_{mp} = 11.3V and I_{mp} = 105mA. The V_{mp} and I_{mp} of the PV array change with PV panel temperature and solar radiation intensity. MPP tracking techniques are employed in photovoltaic (PV) systems for optimum power extraction from the PV array with variation in load, solar radiation intensity and panel temperature. A buck type SC dc-dc converter based MPP tracker is used to track the arrays MPP by Pulse Width Modulating (PWM) the drive signal to the MOSFET switches in the SC converter. A 1cm^2 multi junction test solar cell provides a variable reference proportional to the array's V_{mp}. The comparator C generates a PWM signal whose pulse width is proportional to the error amplifier's (E) output. The PWM circuit is powered by the PV array itself and is activated when $V_{PV} > 6V$.

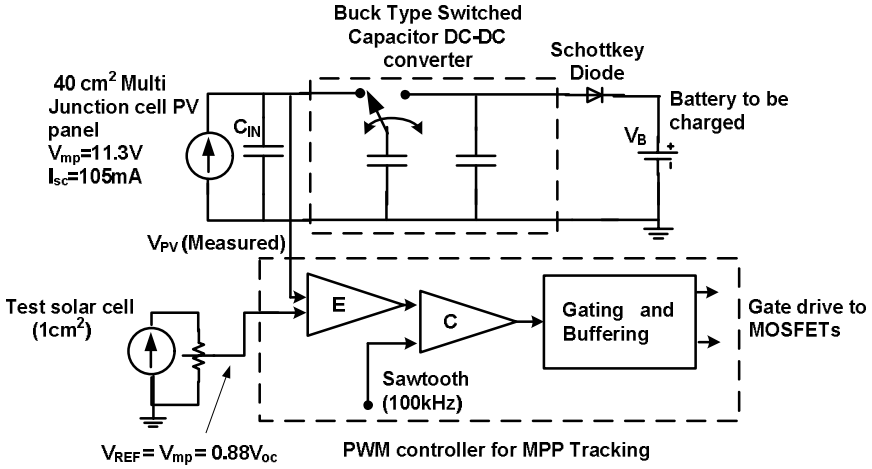


Fig. 1. Block diagram of PV fed SC dc-dc converter based portable battery charger with MPP tracking

Table 1

Test results showing charger parameters for different scenarios. In Case 1 an 8V Li ion battery needs to be charged and in Case 2 a series pack of four Ni-metal-hydride cells have to be charged.

Set V_{mp} (V)		V_{in} (V)	I_{in} (mA)	P_{in} (W)	V_o (V)	I_o (mA)	P_o (W)	η%
Case 1	**11.3**	**11.3**	**95**	**1.07**	**8.3**	**109**	**0.91**	**85.1**
Case 2	**9.0**	**9.0**	**80**	**0.72**	**5.6**	**100**	**0.55**	**77.2**

A novel simple-inductance, double-output Step-down converter for embedded audio applications

Xavier Branca
Email: xavier.branca@stericsson.com
Affiliation: STERICSSON, GRenoble, France
Position: PhD student, INSA-Lyon, France

An IC has been fabricated in CMOS 0.18um (namely HCMOS9A) as an embedded audio application for mobile platform. One power converter is a 8W, 5-switch step-down based on a single inductance, double-capacitor for dual voltage output. Specific power switches have been embedded to stand the electrical constraints issued by the converter specifications and operation. Specific level-shifters are necessary. An original analogue control has been proposed to avoid the complexity of a digital implementation and save energy. Primary experimental results confirm the operation, the dynamic performances and the efficiency (peak 89%, full load).

Integrated LC filter on silicon for DC-DC converter applications

Magali Brunet, Philippe Artillan, David Bourrier, Jean-Pierre Laur, Nicolas Mauran, Laurent Bary, Monique Dilhan, Bruno Estibals, Corinne Alonso and Jean-Louis Sanchez.

Laboratoire d'Analyse et d'Architecture des Systèmes (LAAS-CNRS), 7 avenue du Colonel Roche, 31077 Toulouse cedex 4, France (phone: +33-561-33-7964)

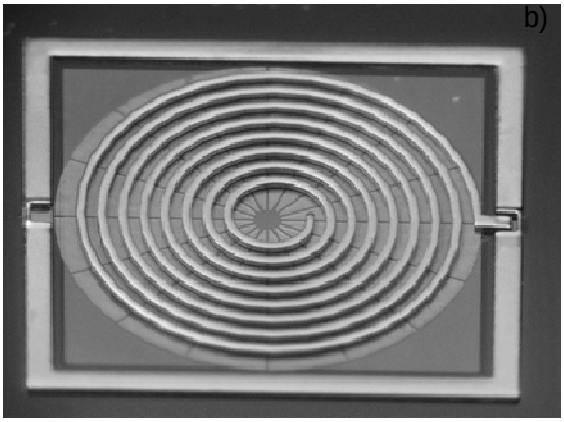
The integration of passive components on silicon for future DC-DC converters applications is still a challenging area of research. We present here the realization of an integrated output LC filter with the following characteristics: 560 nF 3D capacitor on top of which is realized a 110 nH spiral micro-inductor .The integration of a magnetic shield layer is investigated to reduce eddy current losses induced in the capacitor by the micro-inductor.

The impedances of the capacitor and inductor of the fabricated filter were measured separately first on a wide range of frequencies (10 kHz to 4GHz). The equivalent series resistances of both the inductor and the capacitor are minimized thanks to thick copper conductors (50 µm) and highly conductive substrate respectively.

Beyond the challenge of technological steps successions, we demonstrate here the double interest of realizing a thin magnetic shield layer (CoNiFe) between the inductor and the capacitor: the inductor value is modestly increased and the magnetic layer provides an excellent shielding against eddy current losses induced in the conductive substrate /capacitor. As a result, the inductance is stable up to the resonance frequency (110 MHz).

Finally, the full LC filter is tested under real conditions in a DC-DC converter architecture. The component presents sufficient values of inductance and capacitance to be implemented in a DC-DC buck converter working at 5 MHz supplying 400-500 mA output current.

a) b)



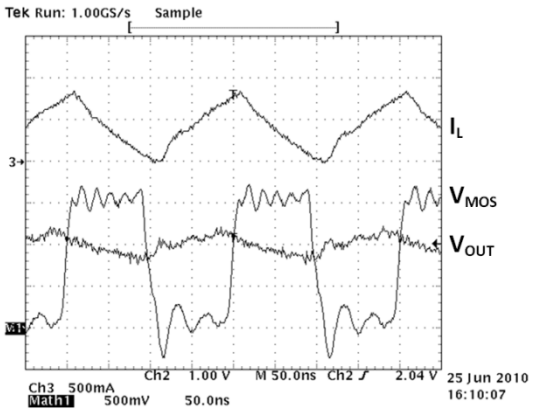


Fig. 1. a) Optical picture of the LC filter (3 mm x 3 mm) with a micro-inductor on top of a 3D capacitor: a magnetic shield (laminated) is integrated. b) Inductor current I_L, MOS V_{MOS} and output voltage V_{OUT} in the buck converter at 5MHz containing the integrated output LC filter.

Design of a DC-DC Converter with Co-Packaged Inductor

Jason Hannon, Santosh Kulkarni, Ray Foley, NingNing Wang, Saibal Roy, Cian O'Mathuna and Kevin McCarthy
Tyndall National Institute, Cork, Ireland

The design of a miniaturized, dc-dc power converter rated up to 1 W that has been specifically designed to meet particular area, efficiency and assembly constraints is presented. The power train has been optimized for low voltage CMOS processes while the filter inductor has been carefully designed using a specially developed optimization tool to meet the converter specification and to achieve the maximum possible efficiency. Simulations predict up to 77% efficiencies can be achieved at frequencies of 30 to 40MHz with a converter area of smaller than 4 mm^2.

A high switching frequency is chosen for the converter to allow a small inductor to be used which in turn reduces the overall size. The trade-off with increasing switching frequency is an increase in switching losses [1], which results in a lower overall converter efficiency. One option to decrease switching losses while still increasing switching frequency is to migrate to a more advanced CMOS node with smaller gate lengths. The downside with the use of smaller processes is the reduction in maximum supply voltage. For this design the nominal input voltage is 3.6 V but the maximum input voltage can be as high as 5 V, necessitating a cascade power device arrangement as shown in Fig (1).

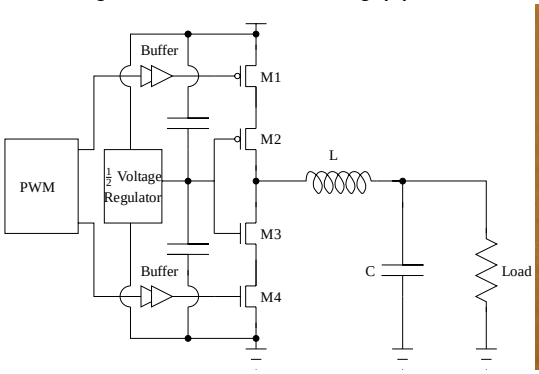


Fig. 1

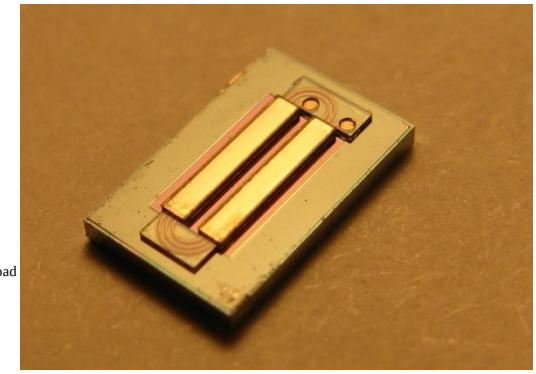


Fig. 2

The inductor uses a racetrack design with a closed magnetic core as shown in Fig. 2. The inductor consists of a racetrack-shaped copper winding, sandwiched between layers of magnetic material, the details of the fabrication process having been previously outlined [2]. The objective of the inductor design optimization process is to maximize the efficiency for the smallest area while minimizing the inductor losses for varying designs. The winding and core losses are evaluated using the expected current waveforms for the convertor. Estimates of the inductor performance are then fed back to the circuit simulations to refine the driver device dimensions.

[1] J. Hannon, D. O'Sullivan, R. Foley, J. Griffiths, K. G. McCarthy,and M. G. Egan, "Design and optimisation of a high current, high frequency monolithic buck converter," in *Applied PowerElectronics Conference and Exposition, 2008. APEC 2008.Twenty-Third Annual IEEE*, Austin, TX, Feb. 24–28, 2008, pp. 1472–1476.

[2] T. O'Donnell, N. Wang, R. Meere, et al., "*Microfabricated Inductors for 20 MHz Dc-Dc converters*", ," in *Applied PowerElectronics Conference and Exposition, 2008. APEC 2008.Twenty-Third Annual IEEE*, Austin, TX, Feb. 24–28, 2008, pp. 689-693.

A 150V Power SOI LDMOS Transistor for MHz Frequency Switching Applications

Patrick Shea and John Shen

University of Central Florida, Orlando, USA

To enable MHz frequency switching of PwrSoC or PwrSiP converters, power MOSFETs with very low gate charge and low on resistance are needed. In this poster paper, we report on the design and fabrication of a 150V, 102 mΩ, chip-scale SOI lateral power MOSFET. The power LDMOS transistor is based on SOR RESURF principle and fabricated in a 0.35um CMOS foundry using a custom process. Device parametrics varied across a wide array of designs and processes. Trends will be presented which correlate layout features and process conditions to electrical parametrics. For a typical design, avalanche current capability was greater than 73 Amps at 230 V during unclamped inductive switching tests (current limited by power supply and circuit inductance). BVdss of this design was typically 155 V with Vth of 5.0 V. Rdson values measured at Vgs = 8V, 10V, and 12V were 115 mΩ, 109 mΩ, and 102 mΩ respectively. The device is designed with very low gate-to-drain charge in order to improve power efficiency at MHz switching frequencies. Qgd for the aforementioned design is 1.7 nC measured at 1MHz and Vgs = 8 V. Qgd for most designs ranged from 1.3 to 2.0 nC depending on design and process. Waveforms including forward conduction, reverse recovery, and gate charge will be presented to illustrate performance of this new SOI power MOSFET design.

GaN Schottky diodes for high operating temperature electronics

Donagh O'Mahony[(1)], Pleun Maaskant[(1)], Peter J. Parbrook[(1,2)] and Brian Corbett[(1)]

[(1)]*Tyndall National Institute University College Cork, Lee Maltings, Cork, Ireland.*
[(2)]*Department of Electrical and Electronic Engineering, University College Cork, Western Road, Cork, Ireland.*

Group-III nitride materials have been identified as having potential application for electronic devices including Field Effect Transistors for both microwave and power electronics. For many power applications reliability of GaN devices under high temperature operation (>200ºC) will be a critical factor. In this presentation we discuss the development of Schottky diodes based on free-standing GaN substrates for a protection diode application for the European Space Agency [1]. The diodes were subjected to high temperature long duration storage testing under forward current and reverse voltage biased conditions at temperatures of 300ºC to 400ºC in N_2 (Figure 1). Stability of the Schottky metalisation at temperatures up to 350 ºC was observed whilst degradation of the interconnect was the identified main failure mode at higher temperatures.

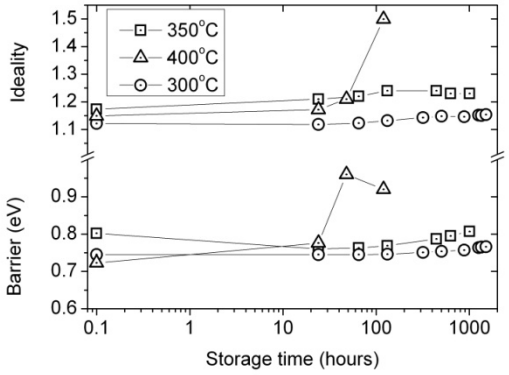


Figure 1: Temperature stability of barrier heights and ideality of diodes tested after storage (no bias) .Measurements taken at 25ºC.

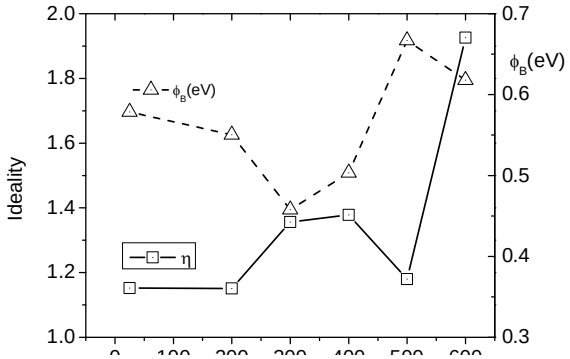


Figure 2: Change in barrier height and ideality with rapid thermal anneal temperature, showing improved properties for anneal temperatures around 500ºC

In addition, thermal annealing experiments showed that parameters such as Schottky barrier height and diode ideality can be strongly modified by selection of an optimum pre-storage anneal temperature of at least 500ºC to optimise and stabilise the Schottky characteristics. (Figure 2).

Recently Tyndall has invested in a new tool for the preparation of III-N materials by MOVPE. A brief description of the tool and possible future electronic device applications will be described.

[1] "Free-standing gallium nitride Schottky diode characteristics and stability in a high-temperature environment",

O'Mahony et al Semicond. Sci. Technol., 24 (2009) 125008

*Corresponding author: donagh.omahony@tyndall.ie.

Digital Control of Multi-Rail DC-DC Converter Systems with Non-Integer Switching Frequency Ratios

James Mooney, Simon Effler, Mark Halton and Abdulhussain E. Mahdi
Department of Electronic & Computer Engineering, University of Limerick, Ireland.

This poster examines the use of non-integer switching frequency ratios in digitally controlled DC-DC converters. In particular it deals with Digital Signal Processor based controllers that provide flexible control solutions for multi-rail DC-DC converter systems. A hardware modification to the interrupt controller of a standard DSP core is proposed that enables it to control multiple DC-DC converters with non integer switching frequency ratios. Improved performance compared with existing DSP based controllers has been demonstrated by applying the modified DSP to a three-rail power converter prototype. The modified DSP overcomes the drawbacks of conventional DSPs, which are attributable to large variations in the delay from when the Analog-to-Digital Converter samples the output voltage to when the duty cycle is updated. By incorporating modified interrupt control hardware in the DSP, the effects of a variable delay are minimized by significantly reducing the worst case sampling to duty-cycle-updating delay. Applying this DSP to a multi-rail system provides the designer with the flexibility to choose arbitrary switching frequencies for individual converters, thereby allowing optimization of the efficiency and performance of the individual converters. The DSP core has the potential to be applied in future multi-rail voltage regulator modules where the digital controller is integrated with the load.

HIGH-FREQUENCY COMPLEX PERMEABILITY ANALYSIS OF CONIFE FERROMAGNETIC THIN FILMS FOR INTEGRATED PASSIVES.

*Jeffrey F. Godsell, Santosh Kulkarni and Saibal Roy**
Tyndall National Institute, University College Cork, Lee Maltings, Prospect Row, Cork, Ireland.

To date CoNiFe films have been extensively investigated for use in magnetic recording applications. In this work CoNiFe thin films have been electroplated onto a Cu seedlayer using a pulse reverse plating technique to produce a nanocrystalline film structure (typical grain size ~20nm, fig 1 (b)). Here for the first time, the high frequency complex permeability of these films have been studied at relatively high bias fields, varying from 0 to 400 Oe with a focus towards integrated inductors/transformers for power supply on chip applications. At lower bias fields, a single Ferromagnetic Resonance (FMR) peak is observed while dual FMR peaks are apparent in the as-measured permeability spectra with increased bias field intensity. Compositional and structural analysis has been performed on the samples to analyse the microstructure in depth. Energy dispersive X-ray analysis, transmission electron microscopy, scanning electron microscopy imaging of the surface and of focused ion beam milled cross sections of the films are presented. Magnetic analysis including magnetic force microscopy, SHB real time hysteresis loop measurements, superconducting quantum interference device as well as Ryowa high frequency complex permeability (1MHz- 9GHz) measurements have been carried out. A slight compositional gradient across the film is suggested by EDX analysis. Contributing factors towards the FMR peak's bias field dependence in the as measured permeability spectra are presented and conclusions drawn.

*Corresponding author - Dr. Saibal Roy, email: saibal.roy@tyndall.ie Tel: +353-21-4904331

Acknowledgement: This work has been financially supported by Science Foundation Ireland Principal Investigator (SFI-PI) grant no - 06/IN.1/I98

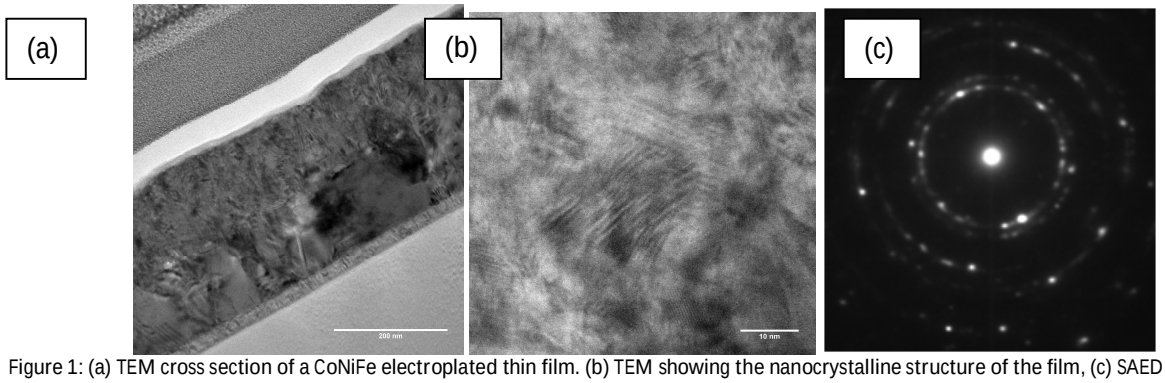


Figure 1: (a) TEM cross section of a CoNiFe electroplated thin film. (b) TEM showing the nanocrystalline structure of the film, (c) SAED showing FCC structure

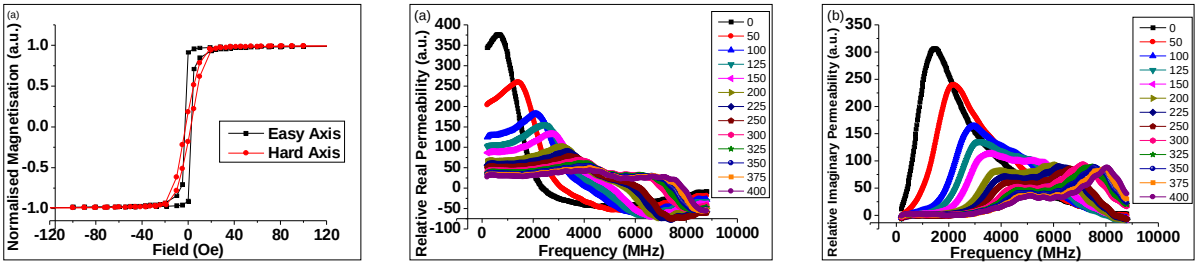


Figure 2: (a) Hysteresis loops in easy and hard axis direction; High Frequency Relative Permeability Spectra of a CoNiFe thin films versus frequency for various bias fields applied (in Oe), (b) real part of the complex permeability, (c) imaginary part of the complex permeability.

Engineered anisotropy in modulated magnetic films for miniaturized devices

S.P. Li, Jeffrey F. Godsell, and Saibal Roy

Microsystems Centre, Tyndall National Institute, University College Cork, Lee Maltings, Prospect Row, Cork, Ireland.

The properties of magnetic materials and devices are largely determined by magnetization configuration, while the magnetization configuration is strongly influenced by anisotropy. However, in most cases, anisotropies are defined at the "wafer level" and therefore fabrication of devices with different anisotropies is difficult. Lithographically patterned isolated micro/nano structures can be used to generate local anisotropy. But, the coercivity of such isolated micro/nano structures is orders of magnitude higher than that of unpatterned film and this requires high fields to drive the devices. Continuous films with modulation on the micro/nano scale have good potential to solve this problem. Surface modulation in one dimension (line pattern) has been demonstrated previously. Here we demonstrate a controlled anisotropy in a film by two-dimensional (2D) nanomodulation. The modulation is created by electroplating magnetic material onto a nanoimprint defined surface template. We show that such a facile technique allows one to generate desirable anisotropic magnetic properties, such as control of remanent magnetization, anisotropy field, and coercivity etc. without breaking the magnetic film's continuity. Micromagnetic simulation shows that the surface topography generated magnetic anisotropy is the consequence of a minimization of magnetostatic energy according to pattern symmetry. Thus, such pattered continuous films may potentially find applications in the integrated dual axis fluxgate sensors. Other example applications include miniaturized high frequency transformer or inductors.

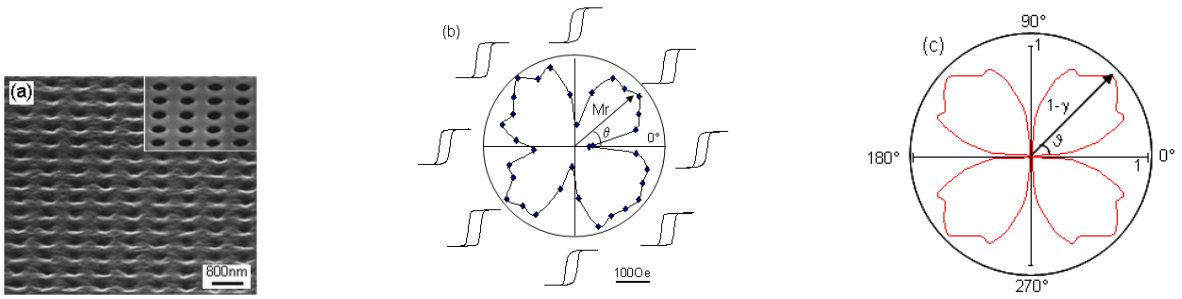


Fig.1 (a) Electrically plated $Ni_{45}Fe_{55}$ film and imprinted PMMA structure (inset); (b) Angle dependence of normalized remanence; (c) Simulated angle dependence of normalized magnetostatic energy(γ) plotted in inverse polarity.

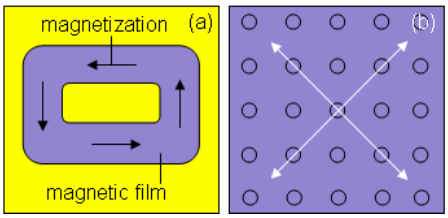


Fig.2. Schematic illustration of generation of artificial magnetization configuration. (a) Closed easy axis. (b)Multi-easy axes.

20MHz DC-DC Converter with Integrated Inductor on Si

Ningning Wang[1], Jason Hannon[2], Ray Foley[2], Kevin McCarthy[2], Kenneth Rodgers[1], Finbarr Waldron[1], Santosh Kulkarni[1], Saibal Roy[1], Cian Ó Mathúna[1]*
[1]Tyndall National Institute, University College Cork, Ireland, [2] Dept. of Electrical Engineering , University College Cork, Ireland, [3] Enterprise Ireland, Industry House, Rossa Avenue, Bishopstown, Cork, Ireland

With the increasing requirement for multi-voltage rails in portable electronics products, miniaturization and integration of the dc-dc converter is becoming an area of intense interest. Although there has been considerable recent progress in the integration of the active parts of such converters, significant miniaturization of the overall converter is retarded by the need to miniaturize and integrate the passive components. The size of the passive component is related to its value and the value of inductance and capacitance can only be decreased by using higher switching frequency for the converter. Only at high enough frequencies the values of inductance required are small, integration of the inductor on to the IC or into the package becomes practical, which consequently bring up the challenges in microsystems fabrication and advanced packaging techniques.

This work is to develop a system-in-package 20MHz dc-dc converter, which consists of a micro-inductor, Power IC with on-chip capacitor, discrete decoupling capacitors. The inductor was fabricated using CMOS compatible micro-fabrication techniques. It has a footprint area of 2.5 mm^2 and an inductance value of 160nH. The Power IC has a footprint area of 4mm2 featuring a on-chip decoupling capacitor.
The prototype was first demonstrated on a PCB board by placing all component side-by-side. The input voltage of the converter is 3.0 V and the output is 1.5 V. The tested peak efficiency of the converter is approx. 72%. All components are connected using wire bonds, which introduce significant parasitics into the converter. . The results of electrical modelling of the circuit will be presented and the impact of parasitics on the electrical performance of converter will be shown.

With the increasing converter switching frequency, parasitics introduced by wire bonds become more and more comparable to the impedance of actual components. In the longer term, the ideal solution to minimize or eliminate the parasitics would be to directly fabricate the micro-Inductor and capacitor, using a back-end CMOS process, on top of the active silicon that provides the control and the switches of the integrated power supply. An interdediate to demonstrate this stacked-on concept is to use stacked co-packaging approach. The measurement of results from a demonstration of a stacked co-packaging approach, based on wire bonding, will also be presented. This approach, not only reduces the parasitics introduced by interconnects, but also reduces the overall footprint of the system. The development of associated power system in package techniques, based on flip-chip stacking, embedded die in polymer, and monolithic integration directly on the power IC will also be presented and compared qualitatively in terms of performance.

AN IMPROVED CALCULATION METHOD FOR AC COPPER LOSSES IN POWER INDUCTORS INTEGRATED ON SILICON

Ningning Wang[*], *Sean Cian Ó'Mathúna*

Tyndall National Institute, University College Cork, Ireland,
[*]*Corresponding author, Ningning Wang, ning.wang@tyndall.ie, Tel: +353 21 4904418.*

The classical one-dimensional solutions such as Dowell's method[1] Perry, Bennet and Larson method, and Ferreira's method[2] are the most common methods to calculate the copper losses of multi-layer transformers and inductors. For transformers, the following assumptions are made in those classic one-dimensional methods:

1) The magnetizing current of transformers is negligible.
2) The flux is parallel to the winding layers and the magnetic fields only have one component directed in the y-direction.
3) Consequently, the magnetic field only varies in the x-direction and the current density has only one component along the z-direction, which only varies in x-direction.

However due to the assumptions made prior to the calculation, these classic one-dimensional methods are subject to some restrictions. In particular some inductors have a closed magnetic core in order to achieve a sufficient inductance within a certain area. It is not clear that the one-dimensional method would be still applicable for this structure.
The magnetic field distributions in two typical inductors, as shown in figure 1, have been investigated using the finite element method in this paper. Inductor (a) has windings sandwiched between the top and bottom magnetic layers, but the top and bottom magnetic layers are not connected. The structure of inductor (b) is similar to the previous one, but its top and bottom magnetic layers are connected by core legs to form a closed magnetic circuit[3].

The finite element analysis shows that the one-dimensional assumptions do not hold for inductor (b). The y-component of the magnetic field intensity along the centre of the inductor(b) is a saw tooth shape, which is very different from that of the inductor(a). Moreover, inductor (a) has a two-dimensional magnetic field distribution and the x-component of magnetic field intensity is not negligible.
According to the geometry of the inductor and using Ampere's law, the DC boundary condition of each conductor (x component or y component of magnetic field intensity, which is parallel to the corresponding surface of the conductor) can easily be calculated. The estimated y-component of magnetic field intensity on left and right edges of all conductors agrees very well with the values simulated using FEM.
Based on the magnetic field analysis, a 2-D analytical model has been developed to calculate the ac copper losses of inductors with closed magnetic core. Three inductors with various conductor aspect ratios are taken for example. The ac factor calculated using this method is compared to that from FEA and the comparison shows that this model accurately predicts the ac copper loss of the inductors. But huge errors are observed when using Dowell's Method or Ferreira's Method. Another advantage of this 2-D method is that it is capable to calculate the ac factor accurately even when the porosity factor is small.

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Structural and Electrical Analysis of Interface Control Layers of MgO or Al2O3 Deposited by Atomic Layer Deposition, at the high- κ/III-V Interface

A. O'Mahony[a], S. Monaghan [a], R. Chiodoa,[b], I. M. Povey [a], A. Blake [a], K. Cherkaoui [a], R. E. Nagle [a], É. O'Connor[a], R. D. Long[a], V. Djara[a], D. O'Connell[a], F. Crupi[b], P. K. Hurley[a] and M. E. Pemble[a]
[a] Tyndall National Institute, University College Cork, Lee Maltings, Prospect Row, Cork, Ireland.
[b] Università della Calabria, Via P. Bucci, 41C I-87036 Arcavacata di Rende (CS), Italy.

HfO2 and ZrO2 have emerged as attractive gate dielectric candidates due to their stability, high *k*-values and fa-vourable band-gaps. However, these oxides form poor interfaces with InxGa1-xAs (x = 0|0.53) substrates due to the presence of low quality, narrow band-gap III-V native oxides. The Al2O3 atomic layer deposition (ALD) process using TMA (Al(CH3)3) and H2O has reportedly a *self-cleaning* effect, leading to the reduction/removal of the III-V native oxides. However, devices employing Al2O3 as the main gate oxide are limited for scaling due to the relatively low *k*-value of Al2O3 compared to HfO2/ZrO2 oxides. This work reports the use of ~1 nm interface control layers (ICLs) of MgO and Al2O3 used in combination with HfO2 on GaAs and In0.53Ga0.47As, and also ~2 nm Al2O3 layers with ZrO2 on In0.53Ga0.47As.

Experimental and results

The structural and electrical effects of thin (~1-2 nm) Al2O3 or MgO (*k*~7.3-10, E**g**~7.3-8 eV) [11-12]) inter-face control layers (ICLs) deposited by ALD at the high-*k*/III-V interface, as part of an overall bi-layer structure on InxGa1-xAs (x = 0|0.53) with HfO2/ZrO2 as the high-*k* gate dielectric, are examined. The aims of the bi-layer approach are to establish if an improvement in the inter-face quality and structure is achieved; secondly if the incorporation of a thin MgO or Al2O3 ICL improves the metal-oxide-semiconductor (MOS) band structure.

The bi-layer approach as outlined in this work combines a thin ICL of a medium-k value, wide band gap material such as Al2O3 or MgO with a thicker high-*k* layer of HfO2/ZrO2 as the gate oxide, with the aim of achieving continued device scaling combined with the potential benefit of a wider band gap oxide *self-cleaning* the nar-rower band gap III-V native oxide during the ALD proc-ess. The HfO2/ICL/III-V bi-layer sample set consists of nominal 5 nm HfO2/1 nm MgO or Al2O3 ICL and corre-sponding control samples (nominal 5 nm HfO2), were deposited by ALD on 350 µm thick n-type GaAs (Si: ~3x1018 cm-3) substrates and 350 µm thick p-type GaAs (Zn: ~2x1019 cm-3) substrates or n-In0.53Ga0.47As/InP(100) (Si: ~3x1017 cm-3) surfaces. The ZrO2/ICL/III-V samples (nominal ~3 nm ZrO2/2 nm Al2O3) were deposited on n-In0.53Ga0.47As/InP(100) (S: ~4x1017 cm-3) or p-In0.53Ga0.47As/InP(100) (Zn: ~4x1017 cm-3) surfaces, which were pre-treated with HCl, NH4OH and (NH4)2S. Deposition of a 200 nm Pd metal gate completed the MOS structure.

Fig. 1(a) presents a HR-TEM micrograph of a Pd/ZrO2/Al2O3/In0.53Ga0.47As MOS device with a ZrO2 thickness of ~3.4 nm and Al2O3 ICL thickness of ~2.4 nm. The oxide physical thicknesses of these layers are in approximate agreement with the nominal thicknesses.

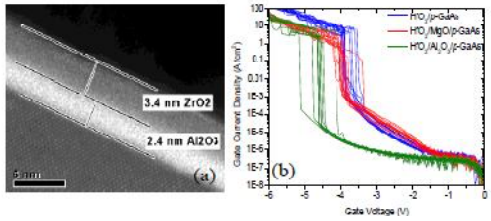

Fig. 1(b) presents JV analysis of the Pd/HfO2/MgO/p-GaAs, Pd/HfO2/Al2O3/p-GaAs, and Pd/HfO2/p-GaAs MOS devices. A significant reduction in leakage current density is observed for devices employing an Al2O3 ICL. This reduction in leakage current density with the incorporation of the wide bandgap Al2O3 ICL is indica-tive of an improvement in the band structure rather than just an increased thickness effect.

Publications

[1] O'Mahony *et al.*, *ECS Trans.*, in press.
[2] O'Mahony *et al.*, *Appl. Phys. Lett.* **97**, 052904 (2010).