Power SoC Vs SiP

Competitive Challenges in High-Volume Applications

Brian Molloy

brian.molloy@infineon.com    molloy@ieee.org
History – to understand rational of decision making

Processes for SiP Vs SoC Decision Making

Analysis of commercial challenges and trade-offs.

Conclusions / Recommendations
SiP History at Infineon
First complex SiP for Wireless in prod. In 1998

- **Learnings**: “Overengineered” SiP – at least for 1998!
- SiP comprised total 5 dies with digital and analog baseband, E²PROM, SRAM and Flash for cellular handset
SiP History at Infineon
GSM Power Amplifier Module in production in 2000

- 5 Layers Low-Loss Ceramic Multilayer
- Part Count: 7 Dies and 31 SMD’s
- One Amplifier Chain with GaAs-Die and Switched Output Matching

Learning's: Thermal Simulation
SiP - RF module for GSM handsets

- Driver: minaturisation
- Complete RF module in 10mm x 10mm
- 6 dies (transceiver, BAW filter, LDO die) integrated passives and SMD BAW

- Learnings: Codesign
Use Case
Virtual Prototyping

... Variants for System Integration ...
System-in-Package (SiP) Co-Design

- System driven flow
- Co-Design methodology for integration of the different components
- Trade-off checks and feasibility analysis for the various SiP possibilities
- Building the complete SiP with the interconnects: flip chip, wire bond, substrate, face to face
- Building of complete interconnect model for analysis
General concept of Virtual SiP Prototyping
SiP in Automotive and Industrial

- Infineon has a long track record for SiPs in Automotive and Industrial of more than 10 years with more than 50 different products
- Shipped Volume: several 100 million units
- Assembly technology: chip on chip and side-by-side on leadframe

Examples in Automotive:
- high current PROFET®: (N-channel vertical power FET with charge pump and diagnostic feedback with load current sense).
- Smart Motor Bridges (Bridges, Half Bridges)

Examples in Industrial:
- CoolSET
- Integrated PWM ControlIC + Power MOSFET
- Integrated PFC control-IC+ CoolMOS™ Power MOSFET
- Fast IGBT DuoPack™: Fast IGBT and anti parallel fast recovery diode
System Integration with multi-chip in a Package enables “intelligent digital control” of Lamps

Digital Smart Lamp Inverter

- Digital Control methods enable optimized closed loop control vs. analog concepts by changing operation-modes condition-based.
- Digital Power Management comprehensively simplifies optimizations throughout the whole switched mode power supply chain (PFC+PWM+Driver)

ICB1F02G

High Side Driver

to HS MOSFET

Controller and Low Side Driver

to LS MOSFET
ISOFACE™ PowerSiP

- Replaces Opto-coupled solution (9 Opto-couplers)
- 70% PCB area reduction

A lot of advantages compared to optocoupler
- No degradation over time
- Gain reliability
- High temperature range ... 150°C
- Very fast transmission (10 ... 100MHz)
- Low power consumption
ISOface™ – SiP in Multi-Chip Packaging (Chip-by-Chip-on-Chip)

Control and Protection Unit

Isolated top chip: 10µm Durimid & Coreless transformer
Our Core Competencies

High Integration 130nm

High Voltage Isolation on Chip

System in Package

System on Silicon

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Factors That Come Into Play

Cost Neutral or
- Performance is compelling
- Space saving is **required** and significant

Performance Neutral
- No performance penalty unless space saving or cost saving is compelling

Dual Source
- Unless cost, performance or space saving is compelling

Without differentiation (compelling cost, required space saving or performance) you will find yourself only gaining traction in niche markets ➜ low volume
Cost Neutrality
Front-End Technology Comparison

Optimos™
Power Process

High Density
CMOS Process

- High Density CMOS manufacturing is ~2X higher cost
**SiP Build-up Package Vs Standard leadframe**

- **SiP** requires more expensive package technology.
- **SoC** should target standard molded package for best cost.

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**ePTFE Substrate**

**SLC Build Up Substrate**

1X

>= 1.5 X
Cost Drivers in Package – Body Size

Price vs Body size

- 2 layers
- 4 layers
- 1-2-1 buildup
Substrate Cost Drivers

![Graph showing the relationship between price and number of vias for different substrate sizes. The graph indicates that as the number of vias increases, the price also increases. The graph includes two lines: one for LFBGA 8x8 and another for LFBGA 13x13. The points on the graph correspond to substrate sizes of 0.5mm, 0.65mm, 0.8mm, and 1.0mm.]
PCB Vs Bonder Placement
Speed Vs Accuarcy

Today we have 0.4 up to 1.0 mm PCB pitches and a component placing accuracy of +/- 30 µ up to +/- 70 µ (@100 k uph equipment).

But direct placing of IC’s with 30x30 µm pads (60 µm pitch) – would need a 10µ placing accuracy to get 50% connection area

60µ IC Pad Pitch

500 µ PCB Ball Pitch

10µ adjustment error: 50% overlap
But PCB placement = +/- 50 µ

Only Chip-Bonders can manage some10µ @ only 10 k uph
# Main Power Stage Configurations Today

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<th>DrMOS</th>
<th>iPS</th>
<th>CanPak</th>
<th>S3O8/SS08</th>
<th>SS08</th>
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<tr>
<th></th>
<th>20.6mm x 9.0mm</th>
<th>21.1mm x 8.9mm</th>
<th>21.5mm x 8.7mm*</th>
<th>25.2 mm x 7.6 mm*</th>
<th>27.6mm x 11.5mm</th>
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<tr>
<td></td>
<td>185.4 mm²</td>
<td>187.8 mm²</td>
<td>187.1 mm²</td>
<td>191.5 mm²</td>
<td>318.4 mm²</td>
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Cost Neutrality
Power Stage Cost Comparisons

- Approx equivalent performance
- Significant cost impact to integrate (whether SiP or SoC)
- SiP and Monolithic are attractive for applications where space is a crucial factor.
The high bar today for semiconductor conversion is >99%!

In Server $V_{\text{core}}$ DCDC we are above 92%
Interconnect Technologies
Thermo-mechanical wear out becomes critical
### Smartphone/Tablet PMU

> 17 Controllers integrated

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<thead>
<tr>
<th>White LED Boost Converter 5.6 V ... 25 V</th>
<th>3 LED PWM Drivers</th>
<th>5 Low Noise LDO's</th>
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<tr>
<td>USB v2.0 USB Charger</td>
<td>Vibra Motor Driver</td>
<td>10 General Purpose LDO's</td>
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<tr>
<td>Battery Charger</td>
<td>Voltage Scaling</td>
<td>2 DC/DC Step down Converter</td>
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<td>I²C I/F</td>
<td>Power ON</td>
<td>HandsFree Audio Amplifier</td>
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<td>Digital Reset</td>
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iPad is basically a large battery with a small PCB

- There is room for PCB increase – SiP/SoC is a hard sell
Tablet Power System Integration may follow the Smartphone Model

- Maximum leverage of semiconductor technology to integrate low-current power, digital power and smart-power functions.

- Maximum use of SiP technology to integrate Drivers, High-current MOSFET’s and passives.
Conclusion

SiP is established and will continue to grow into all areas of Power Management and Power Delivery.

SoC will gain Mass-traction once certain Triggers are Met
- Cost Neutral
  - Co-Design / Virtual Prototyping for product decision making
  - Passives over Active Area – minimum die size penalty
- Performance Neutral or Better
- Reliability
  - Needs more activity and focus

Decision Matrix
- In Research Space – please push the technology
- In Commercial Space – set a methodology and metrics to evaluate and find the ‘should do’ answer for your product.
We commit.
We innovate.
We partner.
We create value.
ENERGY EFFICIENCY
COMMUNICATIONS
SECURITY

Innovative semiconductor solutions for energy efficiency, communications and security.