Integrated Power Conversion –
The Switched Capacitor Approach

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Switched Capacitor Power Converters

- Only switches and capacitors
- Can support multiple input or output voltages/terminals
- Simple full integration in standard process
- Works well over a wide power range
  - Single mode, can adjust clock rate
  - No minimum load
- No inductive switching losses
- Stacked devices enable high voltage with low voltage processes
- Simple low freq model as an ideal transformer with Thevenin impedance
  - freq dependent loss and leakage
First Look

Magnetic boost/buck:

- 10-to-1 V conversion, 1A @ 1V
- S1, S2 rated for V-A product of V*I = 10 V-A
- Sum up to 20 V-A
- Need inductor, inductor loss, Inductive switching

10-to-1 Ladder Switched-Cap:

- 10-to-1 V conversion, 1A@1V
- 20 switches, each blocks 1V
- 18 switches handle 1/5 A
- 2 switches handle 9/5 A
- V-A product sums up to 36/5 =7.2 V-A
- Intrinsic CMOS device convenient
• Performance compared with switch GV$^2$ metric:

\[
\frac{G_{OUT}V_{OUT}^2}{\sum G_i V_{r,i(rated)}^2}
\]

• Since converters are bi-directional, graph applies equally to step-down converters

• Magnetic components modeled with zero conduction loss, and no switching loss impact
Reactive Components

- Fundamental Constraint on dc-dc’s:
  - Power scales with energy storage, parameterized by conversion ratio and ripple

- Buck:
  \[
  \frac{P}{f_s E_L} = \frac{4}{1-D} \cdot \frac{R_L}{(1+R_L)^2} = 4 \frac{G}{G-1} \cdot \frac{R_L}{(1+R_L)^2}
  \]
  - \( R_L \) current ripple ratio
  - \( G \) is current or voltage gain
  - Analogous constraint on input cap
  - Need cap at output for bypass
  - Buck is “efficient” topology – i.e. it has minimally rated inductor

- Example: 2-to-1 V @ 1A; f = 250 MHz
  - 3 turn 500 \( \mu m \) diam spiral inductor in 25 \( \mu m \) thick Cu with 25 \( \mu m \) width and spacing: \(~2.5 \, nH\) with \(~100 \, mohm\) dc resistance
    - \( R_L = 0.4 \)
    - 10 nJ/sq.mm peak
    - Eat at least 10% conduction loss.
  - No accounting for ac resistance, substrate loss, interconnect to this superlevel, nor inductive switching loss
Switched Cap

- Fundamental constraint on caps in S-C ckt analogous to that on L,C in buck
- Series-parallel topologies are “efficient” in utilization of cap energy
- Ladder & Dickson not too bad
- Voltage swing (ripple) amounts to charge sharing loss
- Caps:
  - M-I-M and Gate Cap: 5-10 nF/sq.mm @ 2 V: 20-40 nJ/sq.mm
  - Deep trench cap: 200-800 nF/sq.mm: 2 uJ/sq.mm, with 100’s MHz ESR corner

“A LOW SERIES RESISTANCE, HIGH DENSITY, TRENCH CAPACITOR FOR HIGH-FREQUENCY APPLICATIONS,”


Similar work by others, eg. IPDIA
## Discrete Inductors vs. Discrete Capacitors

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<td>3.4 x 3.0 x 2.0</td>
<td>0.049</td>
</tr>
<tr>
<td>Shielded inductor</td>
<td>Coilcraft</td>
<td>170µH @ 1.0A</td>
<td>11 x 11 x 9.5</td>
<td>0.148</td>
</tr>
<tr>
<td>Shielded inductor</td>
<td>Murata</td>
<td>1 mH @ 2.4A</td>
<td>29.8φ x 21.8</td>
<td>0.189</td>
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- Capacitors have >1000x higher energy density than inductors
Reactives comparison

- Derate inductor by 1000 X
- Explains superior reactive element usage in discrete cap example

\[ M_{SSL} = \left( \sum_{i \in caps} \left| \frac{i_{c,i}}{V_{c,i(rated)}} \right| \right)^2 \]
Ex. 1: Multi-Core On-Die VR
Motivation – Power Reduction

- Clear need for separate supplies to enable per-core power management.

How to efficiently support multiple voltage rails on the die?

100W - 1V - 100A - 1mΩ
(Power ~ 1W/mm²)
Ex. 1: Integrated SC Converter Prototype

- Implemented in 32nm SOI test-chip
- Flying cap: MOS, 32-way interleaved
- Supports 0.6V ~ 1.2V from 2V input

Die photo

\[
\begin{align*}
\text{n = 1/2:} & \quad \frac{Vi}{2V} \quad \frac{Vo}{1V} \\
\text{n = 2/3:} & \quad \frac{Vi}{2V} \quad \frac{Vo}{1.33V} \\
\text{n = 1/3:} & \quad \frac{Vi}{2V} \quad \frac{Vo}{0.67V}
\end{align*}
\]

H-P Le et al, ISSCC 2010
Measured Eff. vs. Topologies

**Efficiency vs. Vo**

- **f_{sw} vs. Vo**

**Settings:**
- $V_i = 2V$
- $R_L \approx 4\Omega$ at $V_o = 0.8V$
Examples with fully integrated native passives

- Capacitor constrained, ref [3] uses series-parallel
- Much higher power density and efficiency than buck
- Limited examples in plain CMOS processes

References:

Extra process steps allowed?

- Very high power density and efficiency expected if deep trench capacitor is used.
- Deep trench capacitors are more mature than on-chip magnetic material.
- SC converter can use existing decoupling cap as converter component, no extra overhead.

References:
Wireless Sensor Nodes & Energy Harvesting

Ex. 2: Self-Powered Active RFID Tag

- **Self-contained** (postage stamp footprint but only mm’s thick)
- **Fully integrated** IC (single die)
- **Small solar cell** harvests enough energy for 24 hour operation

---

**Solar Cell**
- 2cmx1cm
- **10µW** avg (Indoor)
- $V_{oc} = 2.4V$, $I_{sc}=10uA$

**Printed Battery**
- 1cmx1cm
- $V_{bat} \sim 1.1-1.8V$
- Integration w/ substrate

**Loads (on Single Die)**
- 50 µW RX
- 1mW TX
- **0.5V** Logic
- On-chip power management
Power Subsystem Diagram

Architectures: 3:1 to 2:1 adjustable S-C’s, clock speed adjusted for wake-up and again for transmit

John, Mervin
## Load Power Requirements

<table>
<thead>
<tr>
<th>Rail</th>
<th>Clk Rate</th>
<th>State (WkUp, TX)</th>
<th>Peak Load</th>
<th>Avg Load</th>
<th>Max Time</th>
<th>Ripple (mV)</th>
<th>Cls</th>
<th>Eng (uC)</th>
<th>Est Eff</th>
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<tbody>
<tr>
<td>Vdd1</td>
<td>100kHz</td>
<td>Sleep</td>
<td></td>
<td>4uA*</td>
<td>.4s</td>
<td>5mV</td>
<td>1.6</td>
<td></td>
<td>50%</td>
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<tr>
<td>Vdd2_Osc</td>
<td>400kHz</td>
<td>WkUp</td>
<td>15.5uA</td>
<td>13.5uA</td>
<td>4ms</td>
<td>1mV</td>
<td>20fF</td>
<td>0.06</td>
<td>75%</td>
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<td>100uA</td>
<td>4ms</td>
<td>50mV</td>
<td>10pF</td>
<td>0.4</td>
<td>75%</td>
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<td>Vdd2_TX</td>
<td>20Mhz</td>
<td>TX</td>
<td>8.5mA</td>
<td>7mA</td>
<td>10ms</td>
<td>50mV</td>
<td>20pF</td>
<td>70–0.7</td>
<td>75%</td>
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- Efficiency Estimates
  - Vdd1 assumes 90% SC, 75% LDO, 2uA Ref/Control
  - Vdd2_Osc assumes 85% SC, 90% LDO
  - Vdd2_RX assumes 85% SC, no LDO
  - Vdd2_TX assumes 80% SC, no LDO
  - Clock switching frequencies are roughly the minimum for each state
    - Clks are down-converted by the controller
Multi-Mode Duty-Cycled Operation

**Sleep Mode**
- Turn on Reg2
- Enable VDD_WkUp
- Reset Power Manager
- Batt_OK
- Check Battery Level
- Batt_Dead
- Reg1: Low power mode
- Recharge Battery
- STimer sends WakeUp Request
- STimer self-resets
- Store System State in Memory
- Disable Reg2
- Reset Sleep Timer (STimer)
- 400 ms

**WakeUp Mode**
- Reg2: Mid power mode
- PM On: Manage state
- RX On: Receive cmds
- PM sends Sleep/TX Request
- 4 ms

**TX Mode**
- Reg2: High power mode
- TX On: Transmit data
- PM sends Sleep Request
- 4 ms
Solar Cell/Battery Power Interface

- Solar Cell/Battery Charger
  - Comparator, runs at <1Hz to minimize power
    - Set battery max threshold (e.g. 1.4V or 1.9V)
    - Signals topology choice (i.e. 2:1, 3:1)
    - Detect battery state: Dead/Low/OK/Full
  - Voltage Reference shared with regulators
- Shunt Regulator
  - 2.5V NMOS, sized to meet max current (250μA) at rated Vbat (1.2-1.9V)
  - Blocking diode limits reverse leakage
    - Synchronous rectifier reduce Vd

![Diagram of solar cell/battery power interface]

- Vcell - Vbat + Vd
- Vbat = 1.2-1.9V
- Dump extra power
- Solar cell charges battery
- Time

John, Mervin
Example 3 – Point-of-Load: 12V-to-1.5V Dickson Circuit

Illustrates “tap-changing” technique for line regulation.

V.W. Ng, *A 98% peak efficiency 1.5A 12V-to-1.5V Switched Capacitor dc-dc converter in 0.18 um CMOS technology*, Master Thesis Report, EECS Dept, UC Berkeley, Dec. 2007, also in VLSI 2009 and ECCE 2009.
Expected efficiency over line/load

![Efficiency of the converter](image)
Regulation Converter model

Test IC realizing complete mode switching and fine scale regulation now in fab
Simulation
Conclusions

• SC converters very convenient for CMOS/ SOC integration
• Excellent utilization of switches and passive devices
• Chip and IC scale capacitors have higher useful energy and power density than inductors
• Ripple managed by extensive interleaving
• Clock scaling, on-line switch scaling, and drive amplitude techniques convenient for low and ultra-low power operation
• Regulation potential challenge
Ex. 3 - Ultra-low-power Conversion in PicoCube Wireless Sensor Node

PicoCube: A 1cm³ Sensor Node Powered by Harvested Energy, 2008 DAC/ISSCC Student Design Contest
PicoCube Power Management Chip Block Diagram

Analog/Control Circuits

- Current Reference
- Voltage Reference
- Feedback

Power Circuits

- Shaker
- Synchronous Rectifier
- Battery
- Linear Regulators
- Radio
- Microcontroller Sensors
- 0.7V (3:2) Converter
- 2.1V (1:2) Converter

PicoCube Converter Topology

Linear Regulators (LDOs) further regulate and reduce ripple on outputs.
Hysteretic Feedback

- Regulates output voltage
  - On/off clocking control
  - Thermostat-type control
  - Improves efficiency by reducing $f_{sw}$ for small loads

Converter leaves regulation for only large loads
Converter Performance

Regulation is effective at controlling output voltage and increasing efficiency at low power levels!
Why Not S-C?

- Difficult regulation?
- Not suited for high current/power? X
- Interconnect difficulty for many caps? X
- Voltage rating of CMOS processes? X
- Magnetic-based ckts = higher performance? X
- Ripple? X
SC Analysis: Simplest Example

- Slow Switching Limit (SSL):
  - Impulsive currents (charge transfers)
  - Resistance negligible (assume $R = 0$)
  - This (SSL) impedance is the switching loss!

- Fast Switching Limit (FSL):
  - Constant current through switches
  - Model capacitors as voltage sources ($C \rightarrow \infty$)

\[
i = f_{sw} \Delta q = f_{sw} C \Delta v
\]

\[
i = \frac{1}{4 R} \Delta v
\]

($\Delta v = V_{IN} - V_{OUT}$)
Analysis via Charge Multipliers

Capacitor Charge Multiplier:

$$a_{c,i}^j = \frac{\text{charge flow in cap } i, \text{ phase } j}{\text{output charge flow, both phases}}$$

Switch Charge Multiplier:

$$a_{r,i} = \frac{\text{charge flow in switch } i, \text{ when on}}{\text{output charge flow, both phases}}$$

Phase 1:

$$a_c^1 = \frac{1}{2}$$
$$a_{r,1} = \frac{1}{2}$$
$$a_{r,3} = -\frac{1}{2}$$

Phase 2:

$$a_c^2 = -\frac{1}{2}$$
$$a_{r,2} = \frac{1}{2}$$
$$a_{r,4} = -\frac{1}{2}$$
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$$a_{r,4} = -\frac{1}{2}$$
Output Impedance ~ Power Loss
M. Seeman, S. Sanders, IEEE T-PELS, March 2008

• An SC converter’s power loss is the sum of component energy (power) losses:

\[ P_{SSL} = f_{sw} \sum_{\text{capacitors}} \Delta q_i \Delta v_i = R_{SSL} i_{OUT}^2 \quad P_{FSL} = \frac{1}{2} \sum_{\text{switches}} R_i (2q_i f_{sw})^2 \]

• The converter’s output impedance can be determined in terms of just the charge multiplier components:

\[ R_{SSL} = \sum_{\text{capacitors}} \frac{(a_{c,i})^2}{C_i f_{sw}} \quad R_{FSL} = 2 \sum_{\text{switches}} R_i (a_{r,i})^2 \]
Output Impedance and Optimization

Tellegen’s theorem and energy conservation used to find $R_{\text{OUT}}$:

SSL: \[ R_{\text{OUT}} = \frac{1}{f_{\text{sw}}} \sum_{i \in \text{capacitors}} \frac{(a_{c,i})^2}{C_i} \]

FSL: \[ R_{\text{OUT}} = 2 \sum_{i \in \text{switches}} R_i (a_{r,i})^2 \]

Minimize output impedance while keeping component cost constant:

Cost constraint

Optimized components

Optimized output impedance

\[ E_{\text{TOT}} = \frac{1}{2} \sum_{\text{capacitors}} C_i v_{c,i,\text{rated}}^2 \implies C_i^* \propto \frac{a_{c,i}}{v_{c,i,\text{rated}}} \]

\[ R_{\text{SSL}}^* = \frac{1}{2E_{\text{TOT}} f_{\text{sw}}} \left( \sum_{\text{capacitors}} |a_{c,i} v_{c,i,\text{rated}}| \right)^2 \]

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\[ R_{\text{FSL}}^* = \frac{2}{A_{\text{TOT}}} \left( \sum_{\text{switches}} |a_{r,i} v_{r,i,\text{rated}}| \right)^2 \]

In the optimal case:

Capacitor voltage ripple and switch voltage drop are proportional to rated voltage

Output impedance proportional to the square of the \textit{sum of the component V-A prod...}
Comparing Converters

Need a metric to compare converters of different types!

Example: How much power can we get out of a converter with 10% voltage drop?

\[ P_{OUT} = I_{OUT} V_{OUT} = (0.1 G_{OUT} V_{OUT}) V_{OUT} = 0.1 \cdot G_{OUT} V_{OUT}^2 \]

Power performance related to GV^2

We can make a unitless performance metric by comparing converter GV^2 to component GV^2

“Slow-Switching Limit” (SSL) Metric: \[ \frac{G_{OUT} V_{OUT}^2}{f \sum_{caps} C_i V_{c,i(rated)}^2} \]

“Fast-Switching Limit” (FSL) Metric: \[ \frac{G_{OUT} V_{OUT}^2}{\sum_{switches} G_i V_{r,i(rated)}^2} \]
Ex. 3: Microprocessor SC Converter

- A power density of 1 W/mm² is achievable in 65nm process.
- A tiled design improves output ripple and ESR performance
- Creates a scalable IP platform
- Ideal for microprocessor supplies:
  - Ultra-fast transient response
  - Package I/O at higher voltage/lower current
  - Independent core voltage control
Design Optimization Example: 0.4 W/sq.mm

- Representative 0.13um tech
- 2.4-to-1.2V Conversion
- 1 sq mm M-I-M cap (2 nF)
- Losses
  - SSL (main caps)
  - FSL (conduction)
  - Gate cap
  - Cap Bottom plate
  - Junction cap
Switched Cap Take-Aways

• Theoretical performance exceeds magnetic-based converters, and this is being realized in research
• Very simple low power operation – reduce clk
• Integration convenient for v. low power app’s to v. high current app’s
• Moderate (high) voltage capability by stacking devices – triple-well, SOI
• Regulation challenges – nominal fixed ratio, but can operate with multiple Taps
• Further on-chip integration via aggressive clk scaling
• Tap Changing for Line Regulation – Feedforward

• Multi-mode Operation for Apps like Voltage Scaling
Output Impedance ~ Power Loss
M. Seeman, S. Sanders, IEEE T-PELS, March 2008

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Minimize output impedance while keeping component cost constant:

**Cost constraint**

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**Optimized components**

**Optimized output impedance**

$$R_{\text{SSL}}^* = \frac{1}{2 E_{\text{TOT}} f_{sw}} \left( \sum_{\text{capacitors}} a_{c,i} v_{c,i(\text{rated})} \right)^2$$

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Capacitor voltage ripple and switch voltage drop are proportional to rated voltage
Output impedance proportional to the square of the sum of the component V-A prod.
D.H. Wolaver, PhD dissertation, MIT, 1969 proves fundamental thms on dc-dc conv.:

\[ G = \text{voltage or current gain} \]

- **Switches (resistors):**

\[ - \sum_{k \in \text{dc-active}} v_k i_k \geq \frac{G-1}{G} P_O \]

- **Ladder/Dickson are optimal**

- **Reactive Elements:**

\[ \frac{1}{2} \sum_{k \in \text{reactive}} |v_k i_k| \geq \frac{G-1}{G} P_O \]

Meaning for 2-phase ckts:

\[ \sum_{k \in C} V_k q_k + \sum_{k \in L} I_k \lambda_k \geq \frac{1}{f} \frac{G-1}{G} P_O \]
• Performance compared with switch GV^2 metric:

\[ \frac{G_{OUT}V_{OUT}^2}{\sum G_i V_{r,i(rated)}^2} \]

• Since converters are bi-directional, graph applies equally to step-down converters

• Magnetic components modeled with zero conduction loss, and no switching loss impact
Regulation Considerations

- **Open-Loop Loadline Regulation**
  - Droop matching resistive output impedance effective for loadline VR type reg.

  ![Graph showing input and output voltage for an 8-phase 2-to-1 converter](image)

  **Dominant First Order Dynamics**

  **Simulation Example:** 8-phase 2-to-1 converter

- **Tap Changing for Line Regulation – Feedforward**
- **Multi-mode Operation for Apps like Voltage Scaling**
Comparative Energy Densities of Representative SMT Components

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<td>Collcraft</td>
<td>100 μH @ 0.10 A</td>
<td>3.4x3.0x2.0</td>
<td>0.049</td>
</tr>
<tr>
<td>Shielded</td>
<td>Collcraft</td>
<td>170 μH @ 1.0A</td>
<td>11x11x9.5</td>
<td>0.148</td>
</tr>
<tr>
<td>Shielded</td>
<td>Murata</td>
<td>1 mH @ 2.4A</td>
<td>29.8x21.8</td>
<td>0.180</td>
</tr>
</tbody>
</table>

>1000:1 greater energy density ratio (cap:ind), in small discretes

M. Seeman, PhD Dissertation, EECS Dept, UC Berkeley, 2009
Switch Utilization – Conduction Loss Comparison

- Performance compared with switch GV2 metric:
  \[ \frac{G_{OUT} V_{OUT}^2}{\sum G_i v_{r,i(rated)}^2} \]

- Magnetic components modeled with zero conduction loss, and no switching loss impact

![Diagram showing the comparison of different converter types with FSL metric and conversion ratio. The diagram includes lines for Ladder/Dickson, Ideal transformer ckt: 1/32, Multi-ratio series-parallel, Boost/buck, Ladder, Dickson, Doubler, Series-Parallel, Fibonacci, and Boost Converter.]
Reactive Component Comparison:
D.H. Wolaver, PhD dissertation, MIT, 1969: fundamental thms on dc-dc conv.:

\[ G = \text{voltage or current gain} \]

\[ \frac{1}{2} \sum_{k \in \text{reactive}} |v_k i_k| \geq \frac{G - 1}{G} P_o \]

“Time avg of absolute value of V-A prod.”

Meaning for standard 2-phase ckts:

\[ \sum_{k \in C} V_k \Delta q_k + \sum_{k \in L} I_k \Delta \lambda_k \geq \frac{1}{f} \frac{G - 1}{G} P_o \]

Vdc-deltaQ \hspace{1cm} Idc-deltaFlux
Utilization of Reactive Elements:

\[ \text{SC: } 0.02 \cdot \frac{G_{OUT}V_{OUT}^2}{f \sum_{\text{caps}} C_i v_{c,i}^2(\text{rated})} \quad \text{Versus} \quad \text{Mag: } 0.001 \cdot \frac{P_{OUT}}{f \cdot \frac{1}{2} LI^2} \]
The Submicron Opportunity

- Rate device by ratio: $G_s V_s^2 / C V_g^2$
  - Essentially an Ft type parameter for a power switch reflecting power gain, exposes opportunity in scaling
- Suggests that we should look for opportunities to build our cktts with scaled CMOS based devices, but:
  - Low voltage rating per device
  - Inadequate metal/interconnect for high current?
## Comparison with Other Work

<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology</strong></td>
<td>130nm Bulk</td>
<td>32nm Bulk</td>
<td>45nm SOI</td>
<td>32nm SOI</td>
</tr>
<tr>
<td><strong>Topology</strong></td>
<td>2/1 step-up</td>
<td>2/1 step-up</td>
<td>2/1 step-down</td>
<td>2/3, 1/2, 1/3 step-down</td>
</tr>
<tr>
<td><strong>Capacitor Technology</strong></td>
<td>MIM</td>
<td>Metal finger</td>
<td>Deep trench</td>
<td>CMOS oxide</td>
</tr>
<tr>
<td><strong>Interleaved Phases</strong></td>
<td>16</td>
<td>32</td>
<td>1</td>
<td>32</td>
</tr>
<tr>
<td><strong>C_{out}</strong></td>
<td>400pF (= C_{fly})</td>
<td>0</td>
<td>Yes</td>
<td>0</td>
</tr>
<tr>
<td><strong>Converter Area</strong></td>
<td>2.25 mm²</td>
<td>6678 μm²</td>
<td>1200 μm²</td>
<td>0.378 mm² (1.4% used for load)</td>
</tr>
<tr>
<td><strong>Efficiency (\eta)</strong></td>
<td>82%</td>
<td>60%</td>
<td>90%</td>
<td>81%</td>
</tr>
<tr>
<td><strong>Power density @ \eta</strong></td>
<td>2.09 mW/mm²</td>
<td>1.123 W/mm²</td>
<td>2.185 W/mm²</td>
<td>0.55 W/mm²</td>
</tr>
</tbody>
</table>

Charts: 2-1 V & 1-2 V functions

- H-P Le, ISSCC 2010, 32 nm SOI
- Breussege, VLSI 09, 130 nm bulk
- Somasekhar, VLSI 09, 32 nm bulk
- Projected, 400 fF/sq.um, 32 nm tech
Comparison with Magnetic Designs

Ladder-type switched-cap converter

Series-Parallel SC converter

Transformer-bridge converter

Boost or Buck converter

Switch sizes optimized for a given conversion ratio $n$ for each converter
Test Chip Layout in Triple-Well 0.18 µm CMOS9

- Switches at periphery and numerous bond-pads and bond-wires are to reduce series resistances
- Solder bump reduces die size
Design vs. Measured Performance

<table>
<thead>
<tr>
<th></th>
<th>Design</th>
<th>Est.</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{OUT}@1\text{MHz}$</td>
<td>210mΩ</td>
<td>287mΩ</td>
</tr>
<tr>
<td>Fixed Loss</td>
<td>0.3mW</td>
<td>2.1mW</td>
</tr>
<tr>
<td>Freq-dep Loss</td>
<td>7.5mW</td>
<td>5.5mW</td>
</tr>
<tr>
<td>Peak eff</td>
<td>95%</td>
<td>93%</td>
</tr>
<tr>
<td>Eff at 1A</td>
<td>85%</td>
<td>83%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Contribution to $R_{FSL}$</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>All switches</td>
<td>51mΩ</td>
</tr>
<tr>
<td>On-chip metal</td>
<td>39mΩ</td>
</tr>
<tr>
<td>Capacitor $R_{ESR}$</td>
<td>15mΩ</td>
</tr>
<tr>
<td>Bond-wire</td>
<td>65mΩ</td>
</tr>
</tbody>
</table>
POL Package Concept: Flip Chip Packaging Scheme
* The TI SC has a much lower conversion ratio of 3:1
Regulation

- Regulation can be achieved by
  - Changing switching frequency (SSL), or switch modulation (FSL)
  - Changing conversion ratio
- Circuit in figure supports 4 different conversion ratios
  - By tapping at different nodes of the circuit at different phase
Freq mod state machine

If $V_{SG} > 1.3$
   $CLK_{TARGET} = 9$
   (2.5MHz)
else if $V_{SG} > 0.8$
   $CLK_{TARGET} = 20$
   (1.25MHz)
else if $V_{SG} > 0.6$
   $CLK_{TARGET} = 100$
   (250kHz)
else
   $CLK_{TARGET} = 500$
   (0Hz)
Ex. 1: Fully Integrated Power Delivery for High-Performance Digital ICs

The need

Use fully integrated reconfigurable Switched-Capacitor DC-DC converter

ISSCC 2010

82% Effi. at 0.55W/mm²
3 reconf. topologies