Gate-Charge Recovery for Light-Load Efficiency Improvement in High-Frequency DC-DC Converters

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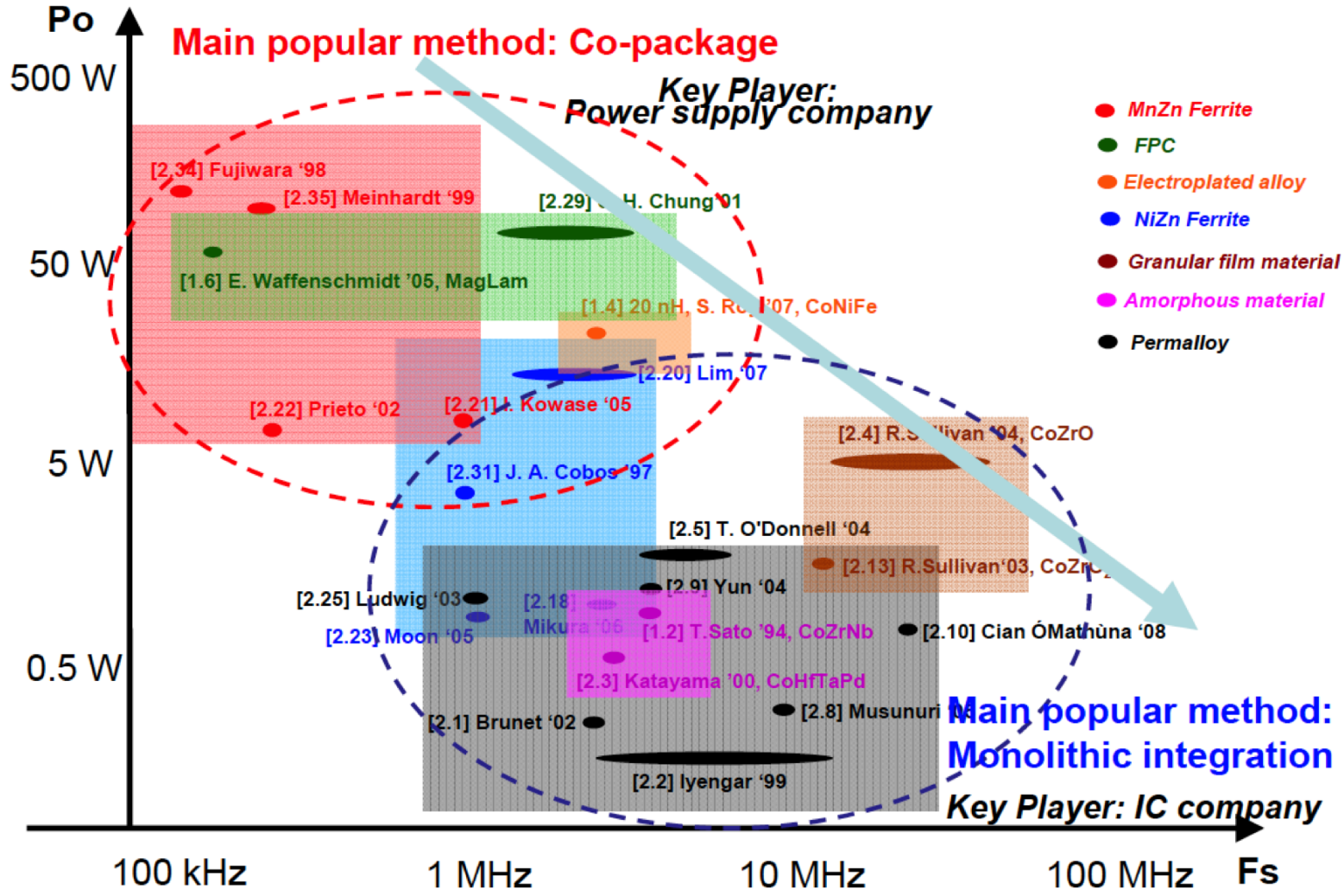
Outline

- Motivation: light-load efficiency in mobile devices
- Existing gate-drive power optimization techniques (fixed/variable frequency)
- Proposed gate charge recycling using output capacitor as the storage element
- Precision closed-loop calibration of gate driver timing for charge recycling in 0.13 μm CMOS
- Conclusion

Source, PSMA, APEC'09

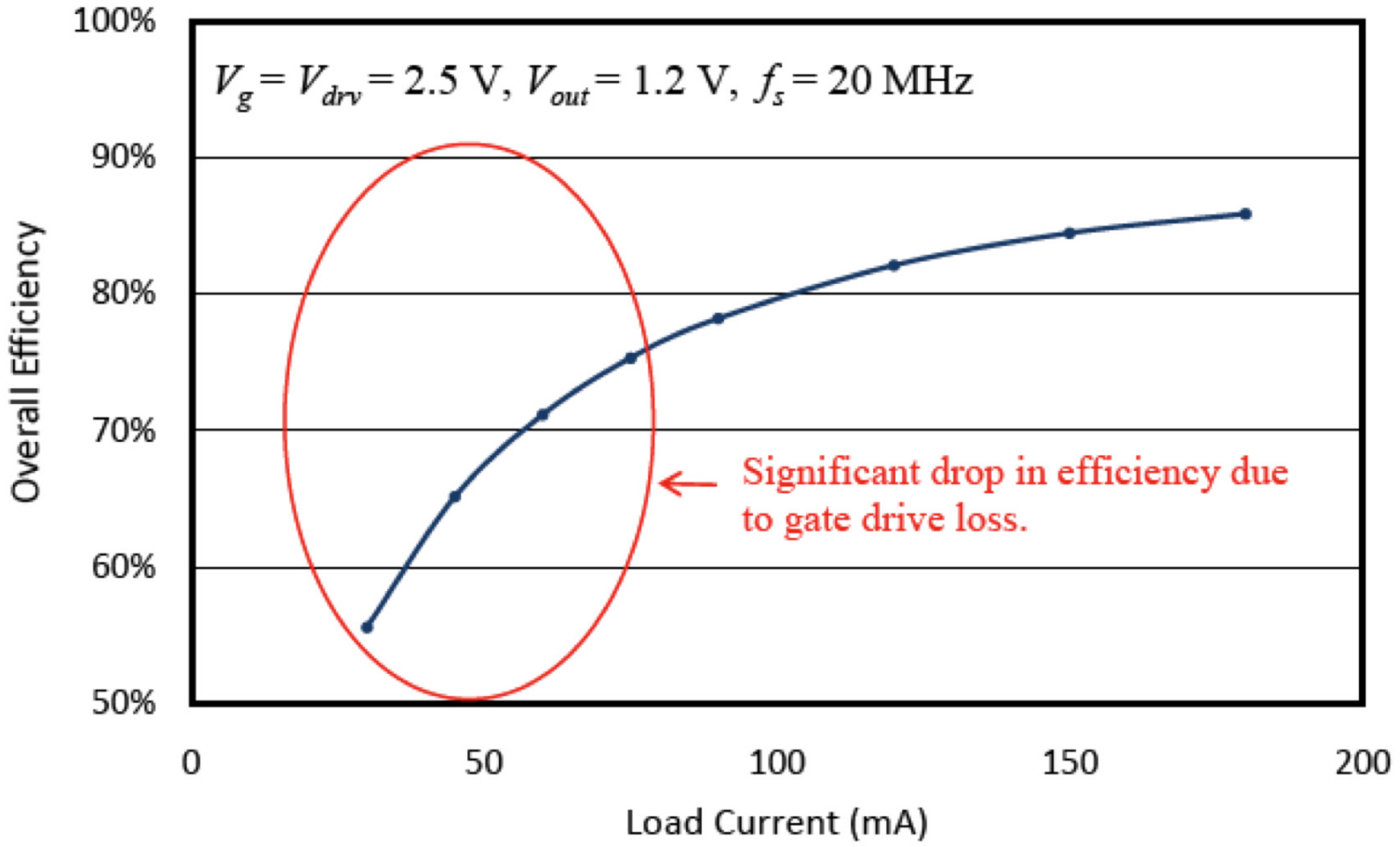
SMPS Landscape



Source, PSMA, APEC'09

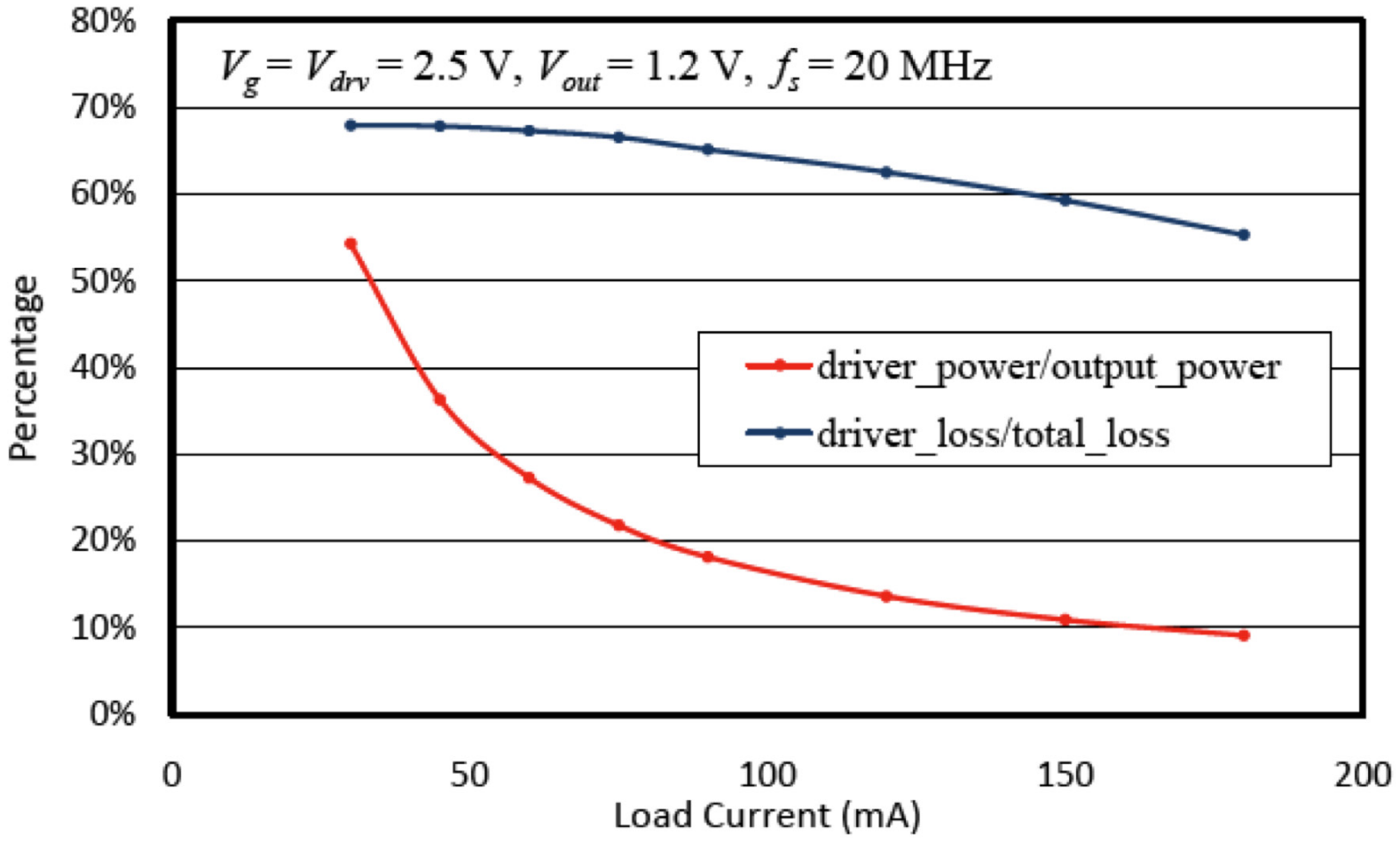
Light-Load Efficiency of 20 MHz Buck Converter

- Simulated light-load efficiency of 20 MHz buck converter designed in 0.13 µm CMOS technology. Significant efficiency drop below 100 mA.



Gate Drive Loss Limits Converter Efficiency

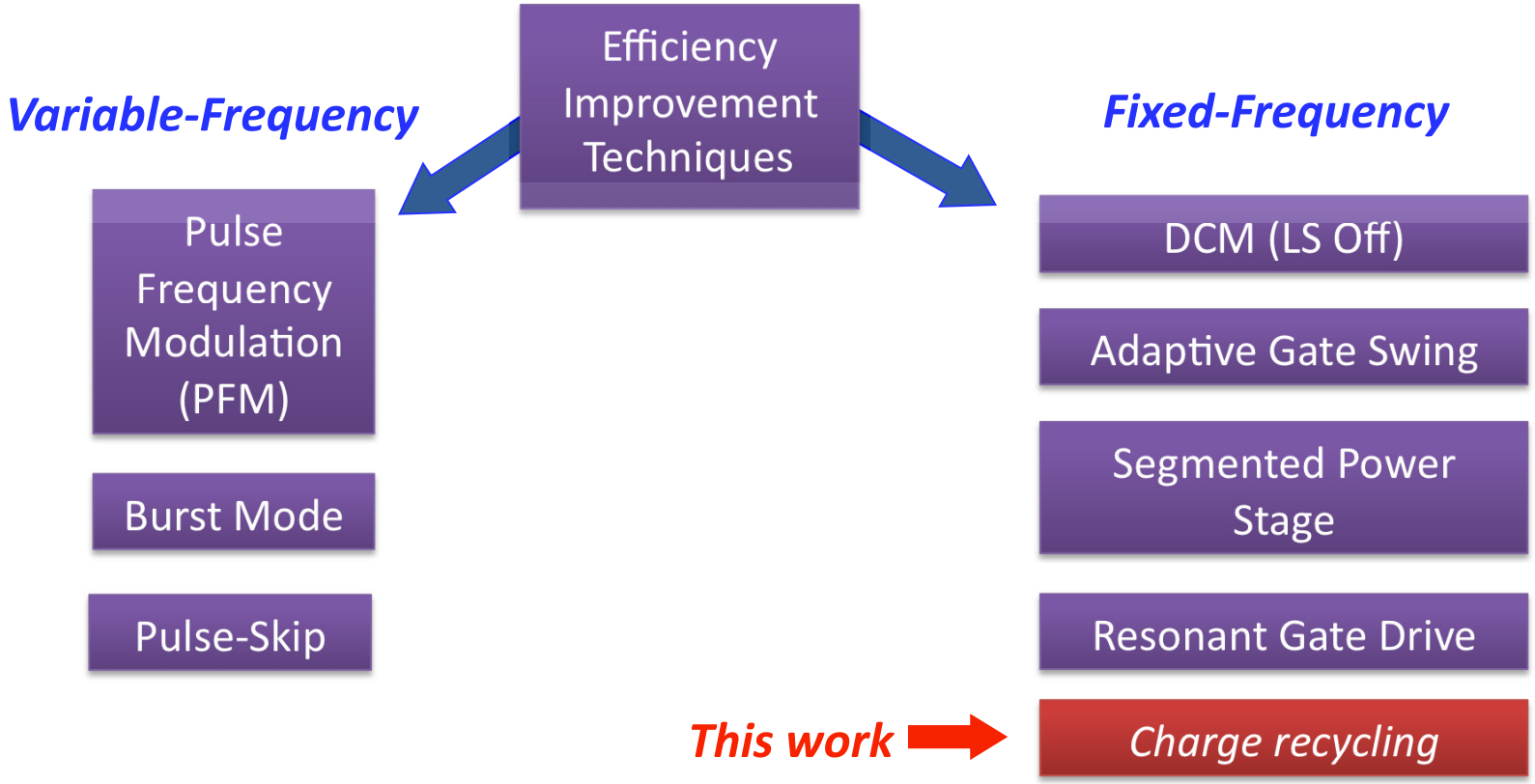
- At light load, > 60% of the total loss is gate drive loss!



Light Load Efficiency Improvement Techniques

- Light-load efficiency improvement techniques are divided into 2 categories
- Certain applications do not permit variable frequency operation (EMI)

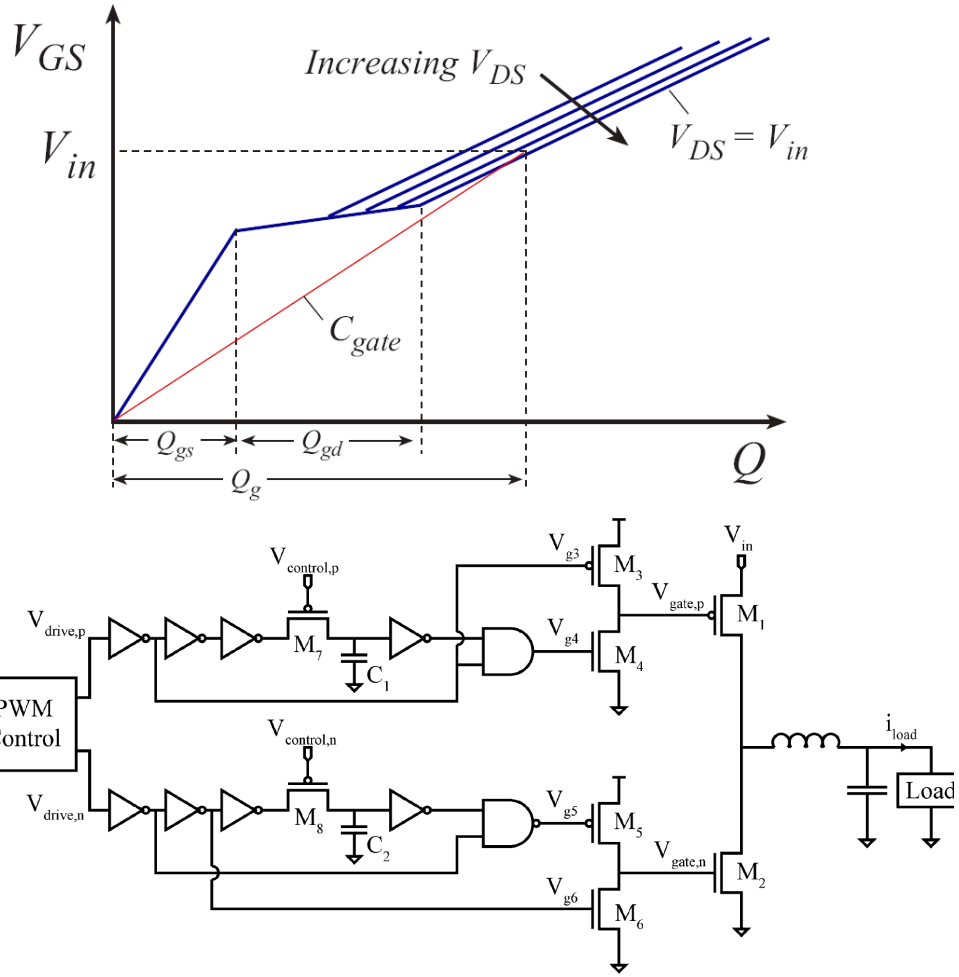
$$P_{gate} = Q_{gate} \cdot V_{dr} \cdot f_s$$

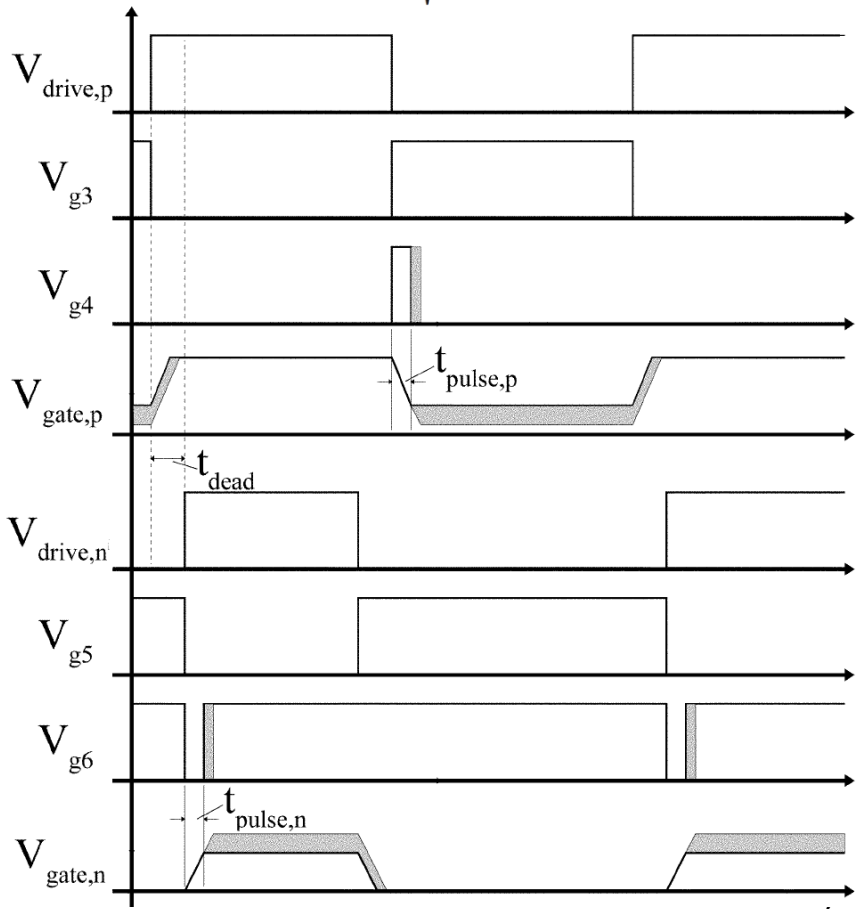


Adaptive Gate Swing (AGS)

- Adaptive gate charge control using RC timing circuit:

$$V_{g,opt} = \sqrt{\frac{D\Delta i_L^2}{3kC_gV_{in}f_s}} + |V_{th}|$$

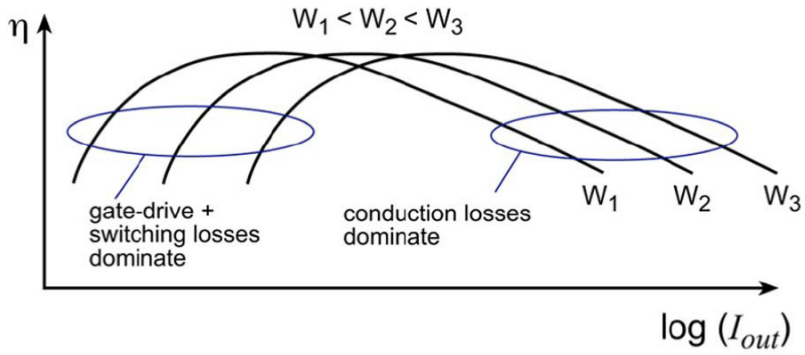


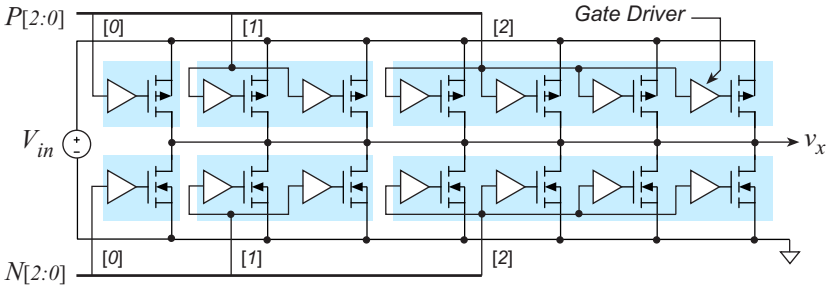


Source: Mulligan et. Al. IEEE Power Electronic Letters 2005

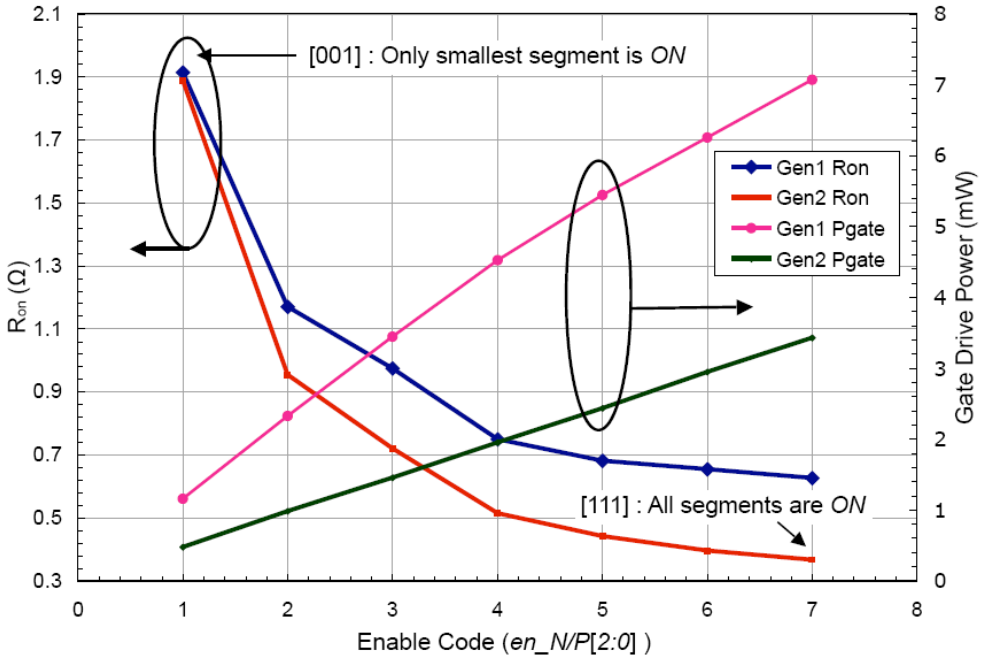
Segmented Power Stage (SPS)

- 3-bit, binary weighted segmentation at 4 MHz:





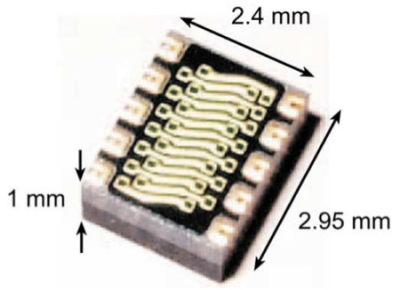
- P_{gate} is reduced by 6.3×
- $R_{on,N}$ increased by 2.4×, $R_{on,P}$ increased by 3.1×

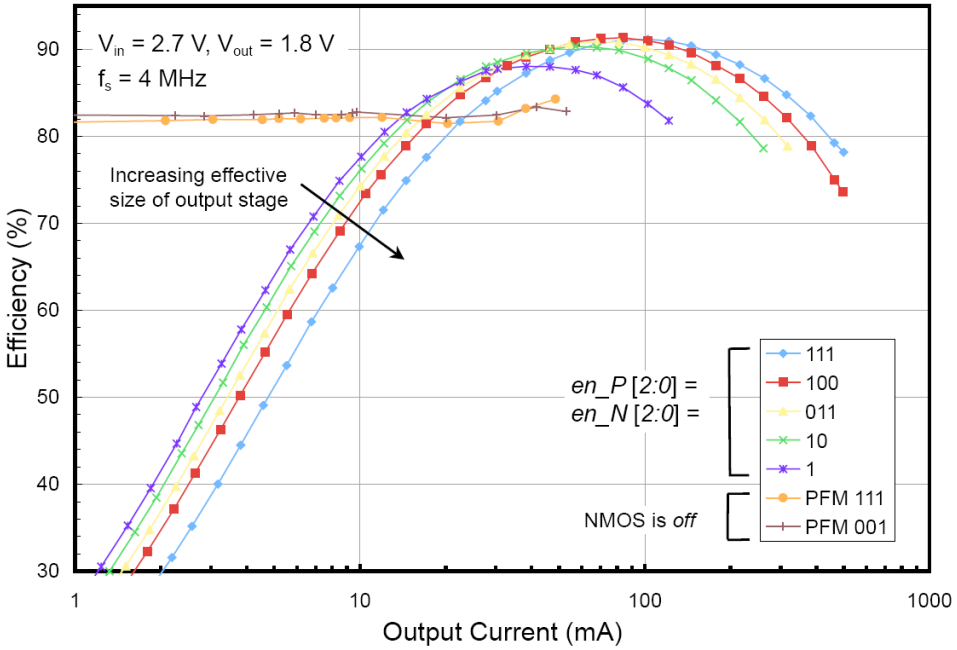


Source: Trescases et. al. ISPSD'06

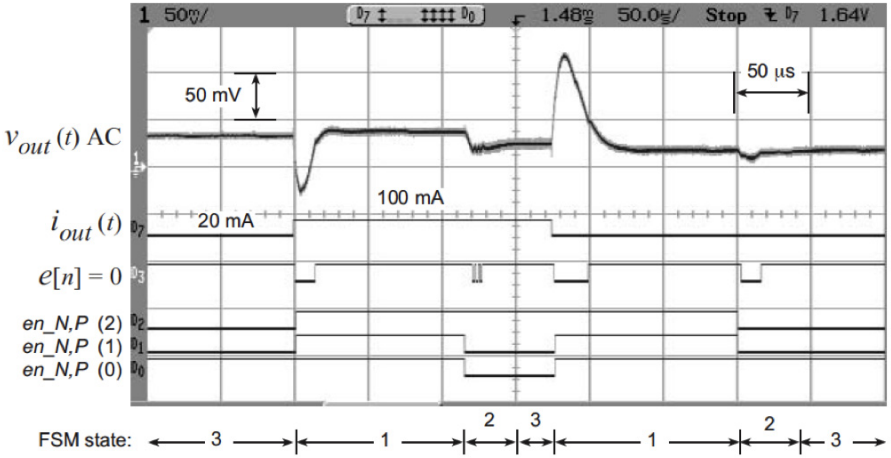
Segmented Power Stage (SPS)

- Experimental efficiency for 3-bit, binary weighted segmentation at 4 MHz





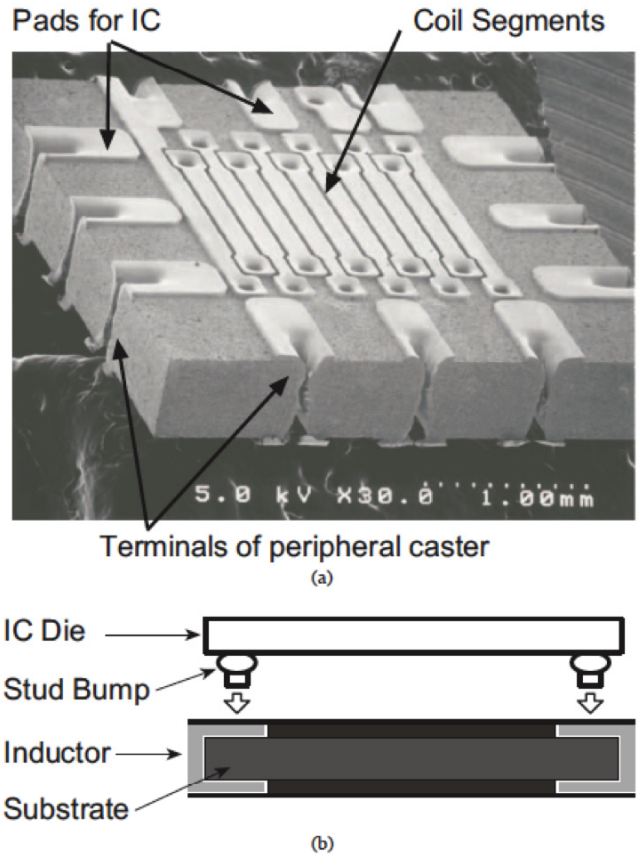
Dynamic Segment Control in Closed-Loop

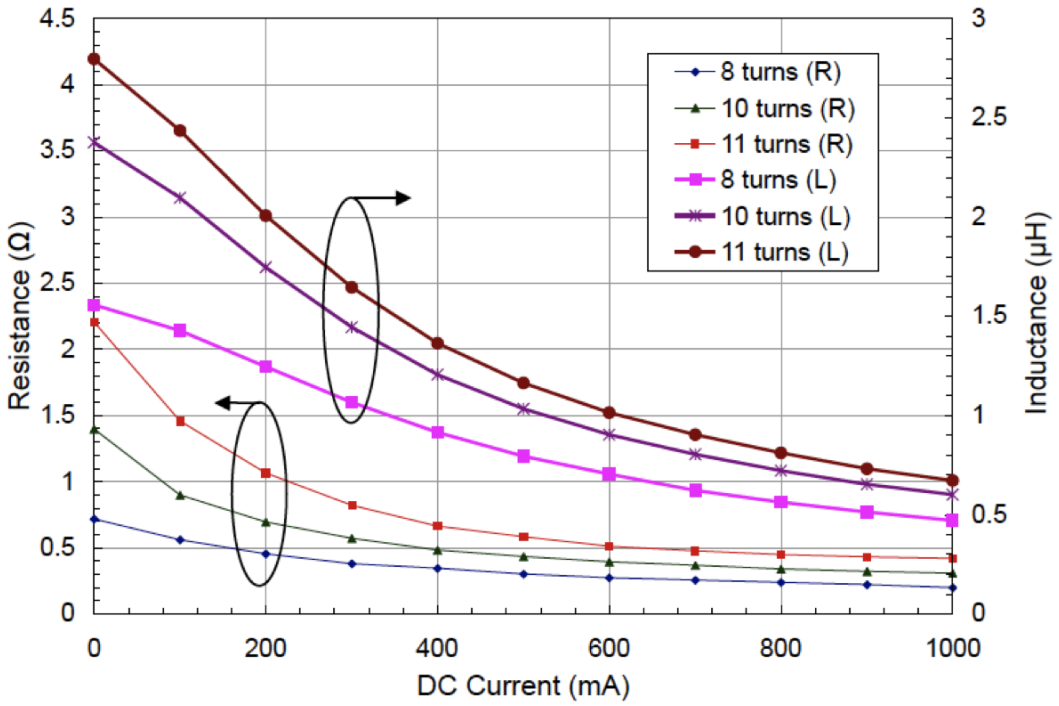


Source: Trescases et. al. ISPSD'06

Fuji Electric CSM

- Chip scale module for HF DC-DC converter

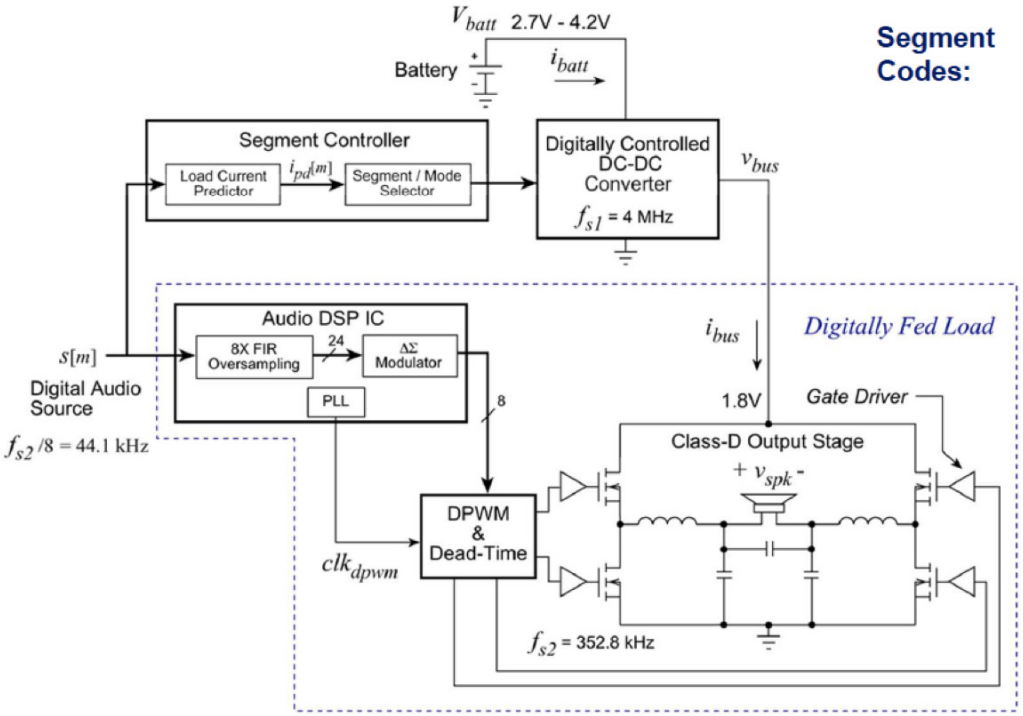




Source: Trescases et. al. ISPSD'06

System Power Management with SPS

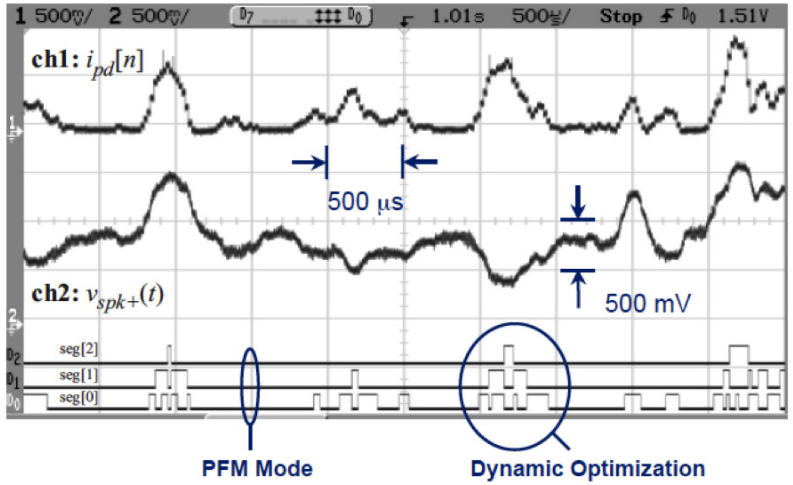
- Application in digital class-D audio:

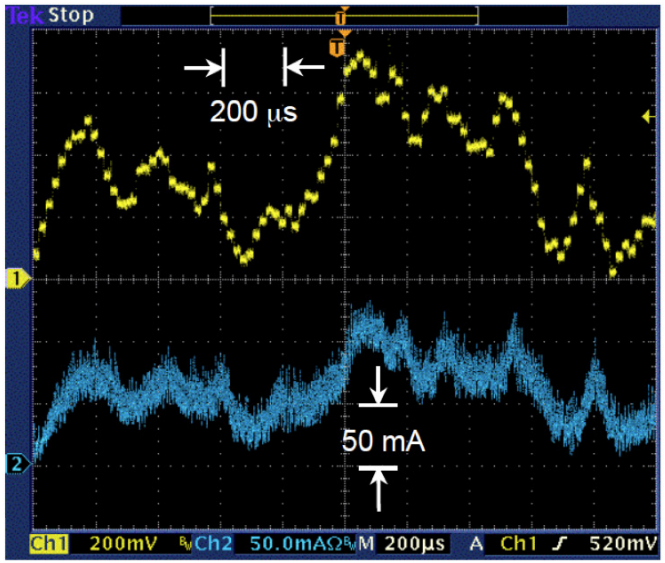


Predicted Current:

Speaker Voltage:

Segment Codes:

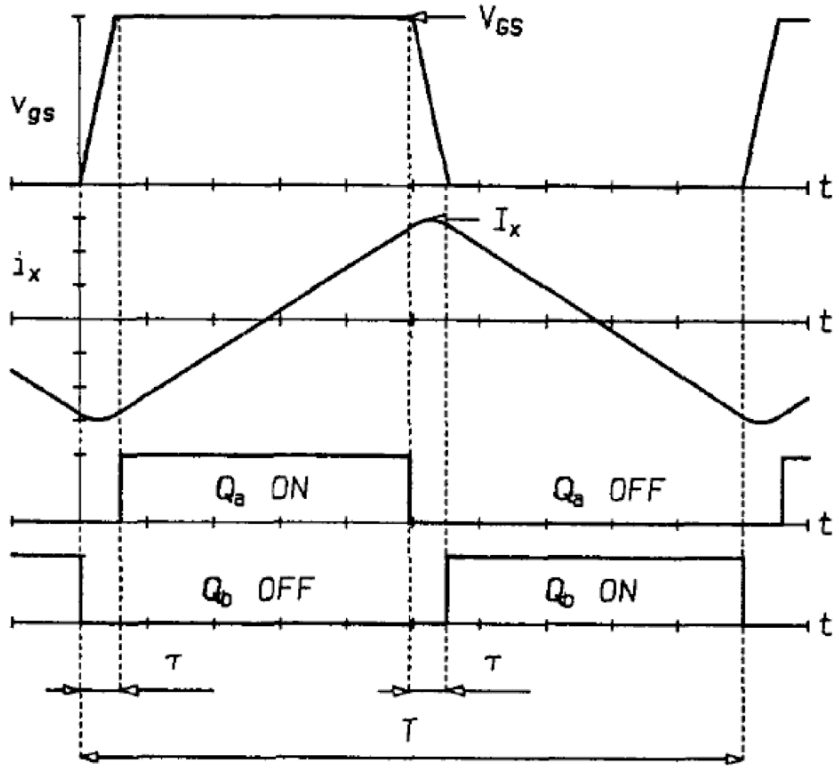


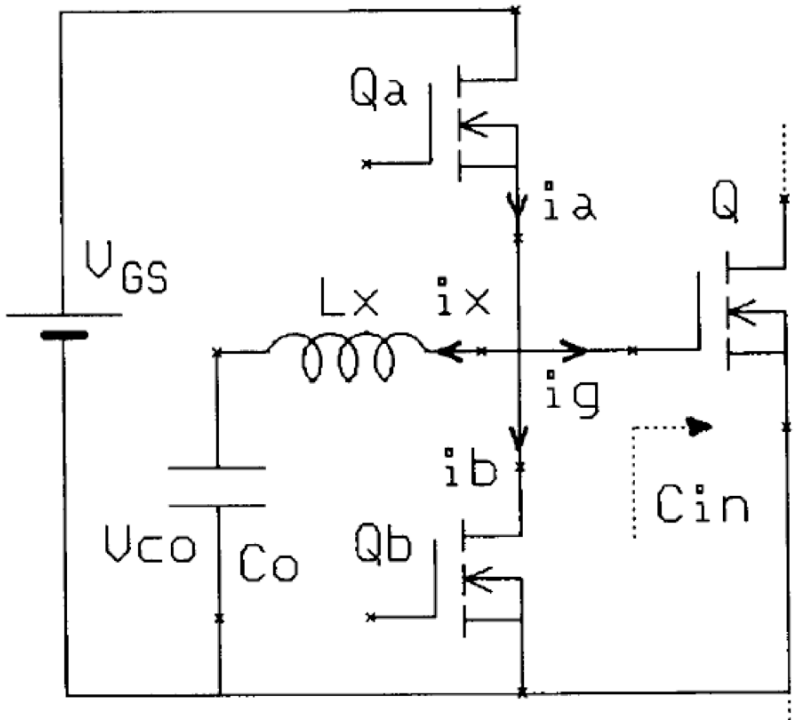


Source: Trescases et. al.TPE'08

Resonant Gate Drive

- Original resonant gate driver:

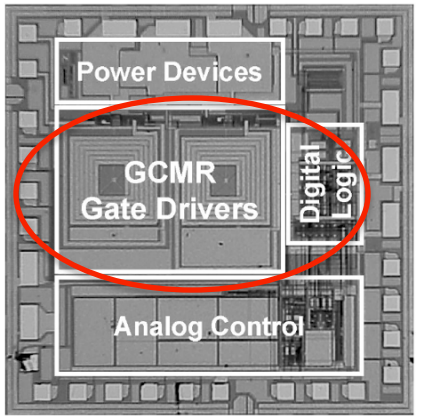


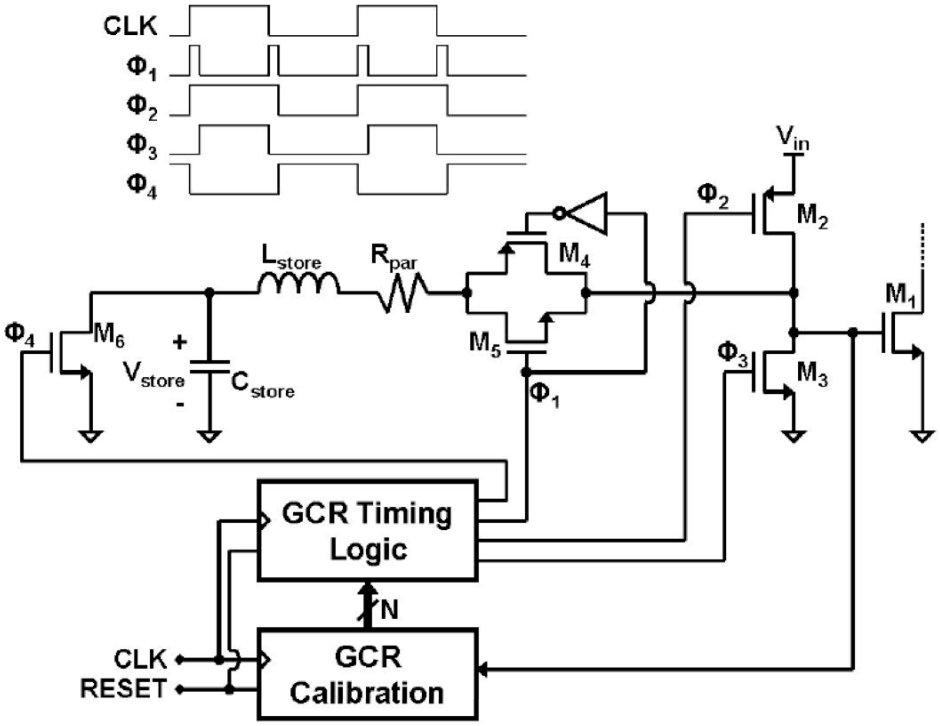


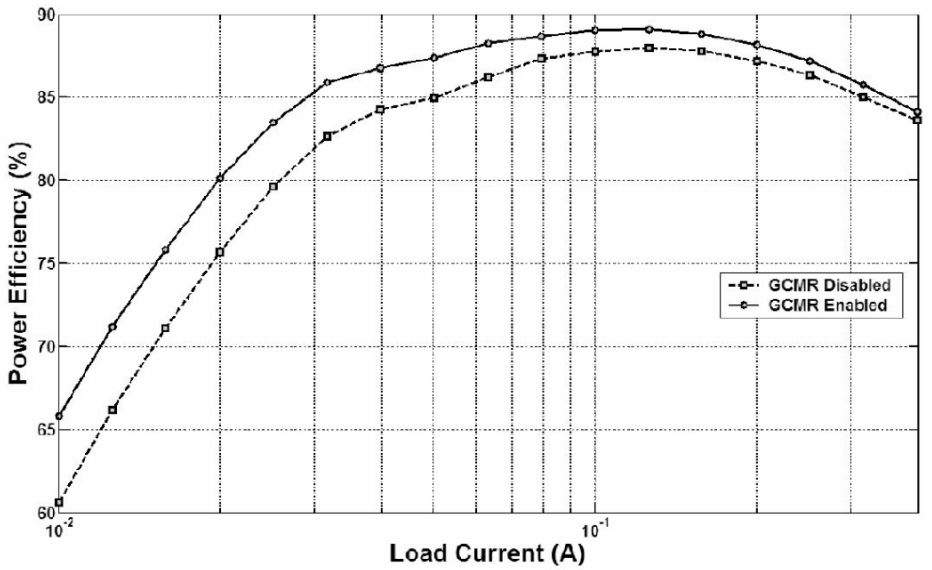
Source: Maksimovic, PESC 1991

Charge Recovery

- Uses on-chip C_{store} (85 pF + 35 pF total)+ L_{store} (22 nH x2)
- Approx 5 % efficiency improvement at 3 MHz operation
- Additional energy storage components dominate the layout

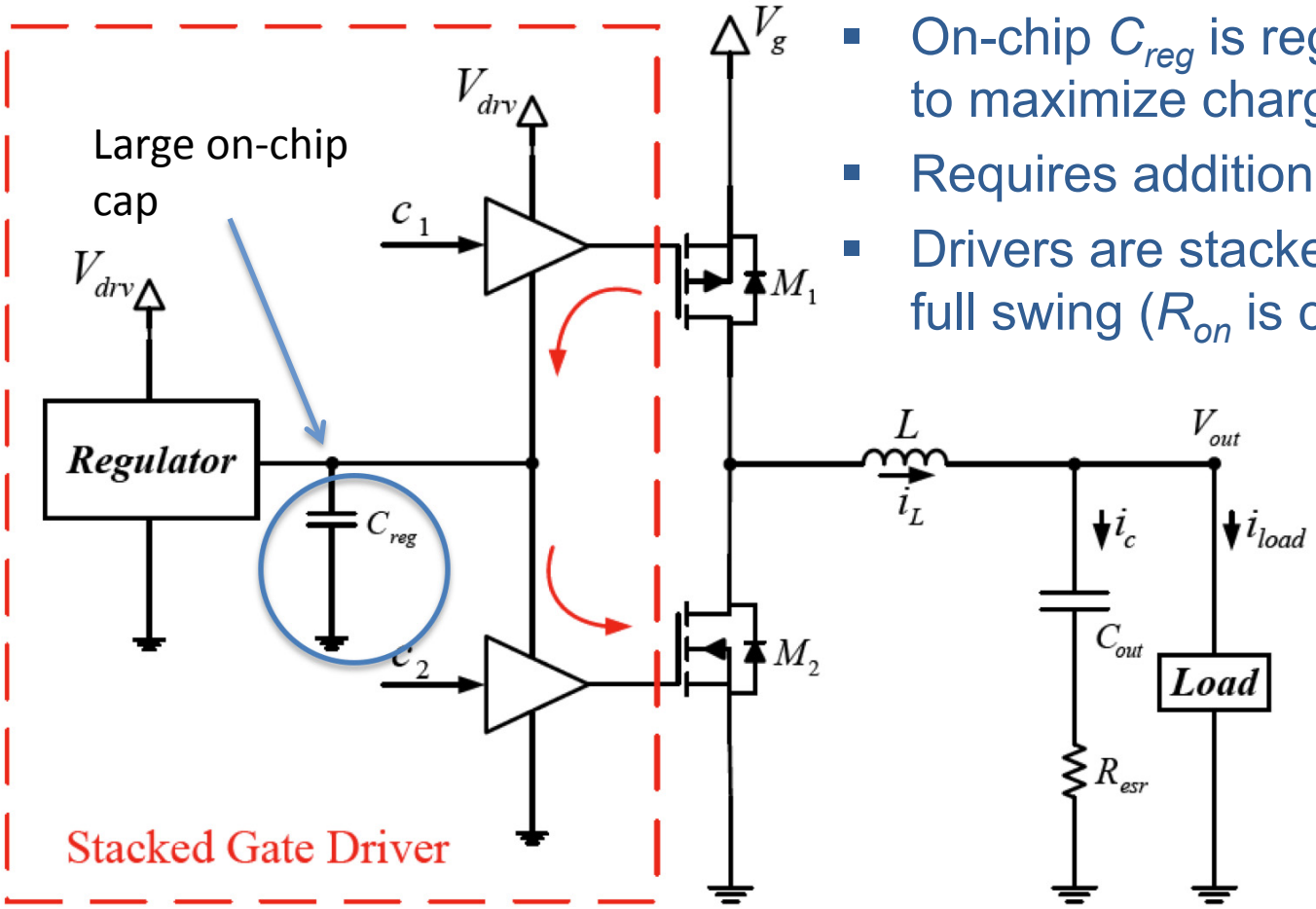






Source: Mulligan et. al. ISSCC'07

Existing Gate-Charge Recycling Technique



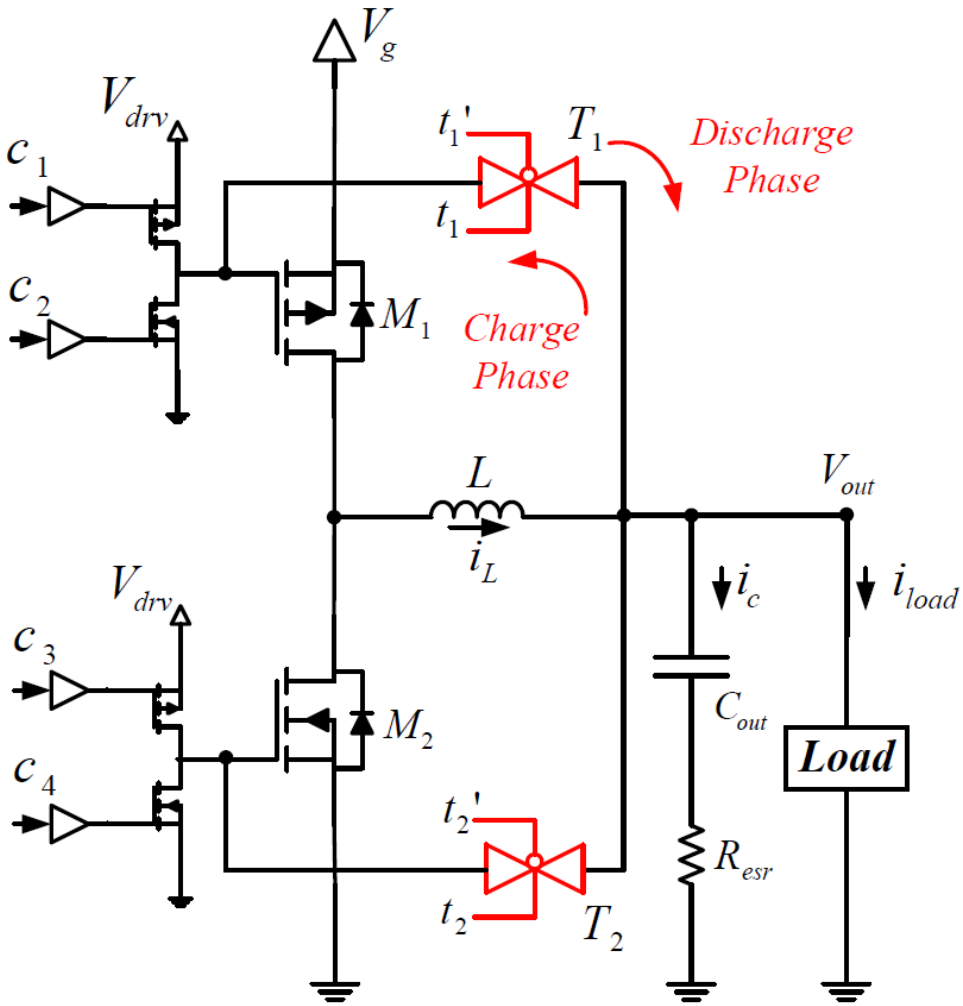
- On-chip C_{reg} is regulated at mid-rail to maximize charge recycling
- Requires additional linear regulator
- Drivers are stacked and don't reach full swing (R_{on} is compromised)

[1] J. Xiao et. al. JSSC 2004.

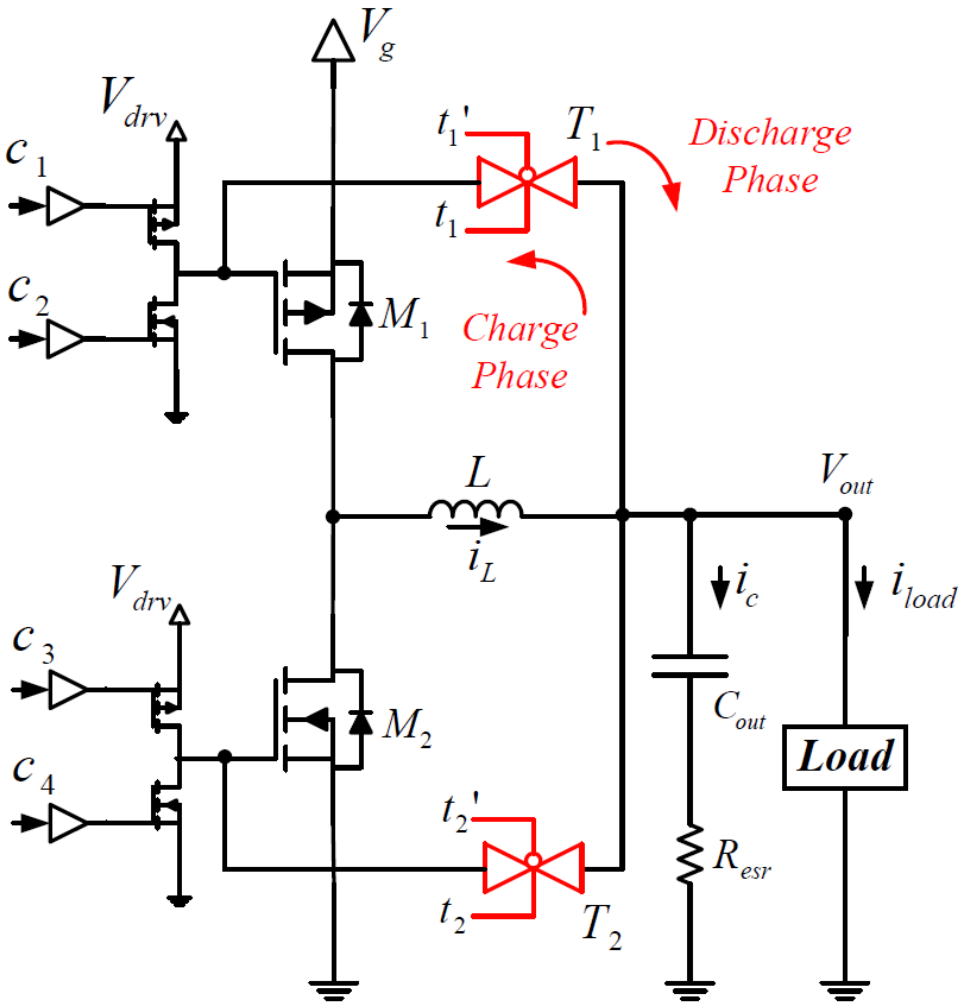
[2] M. Alimadadi, et al. IEEE PESC 2008.

Proposed Gate-Charge Recycling Technique

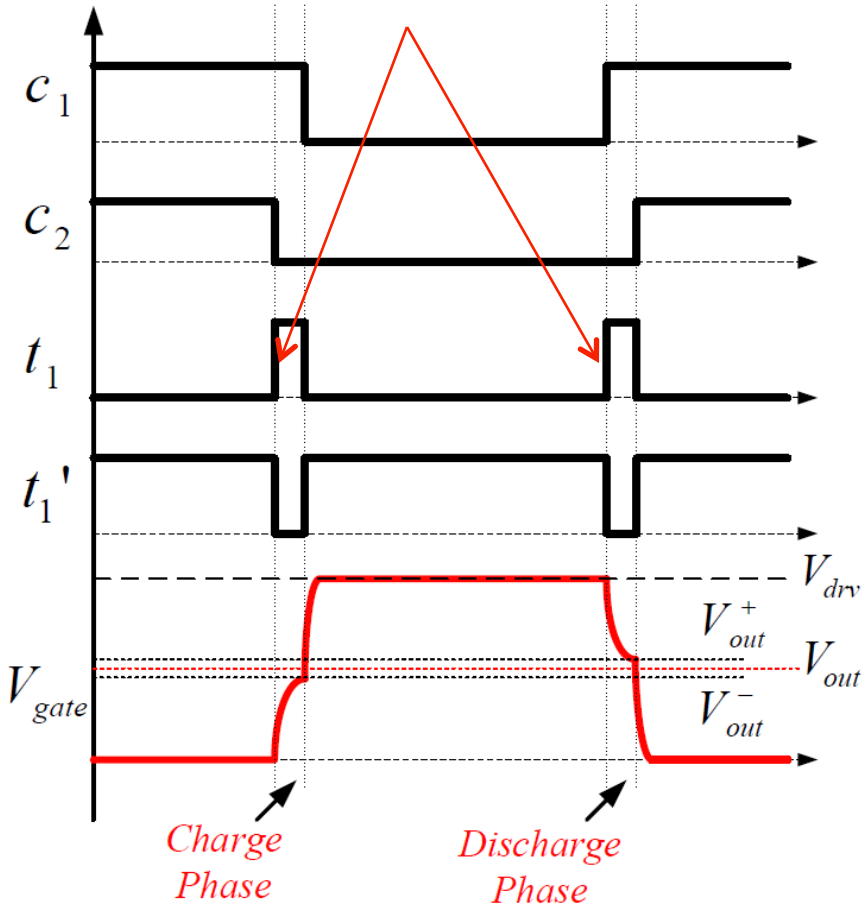
- No on-chip energy storage needed
- C_{out} is used as energy storage
- No additional linear regulator required
- Additional dynamic power consumption due to transmission gates
- Main drivers can be reduced in size
- Power savings depends on V_{out}



Proposed Gate-Charge Recycling Technique

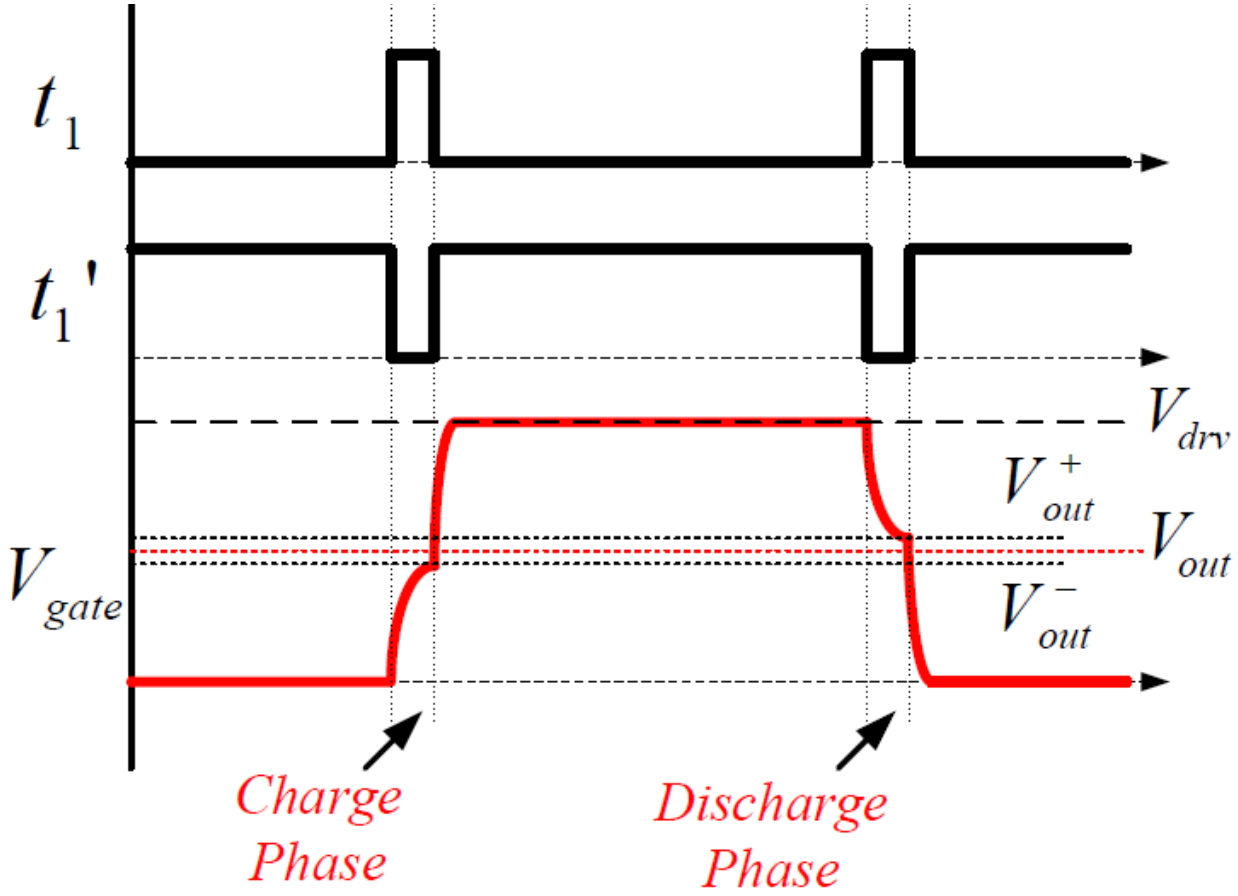


Precision timing control required

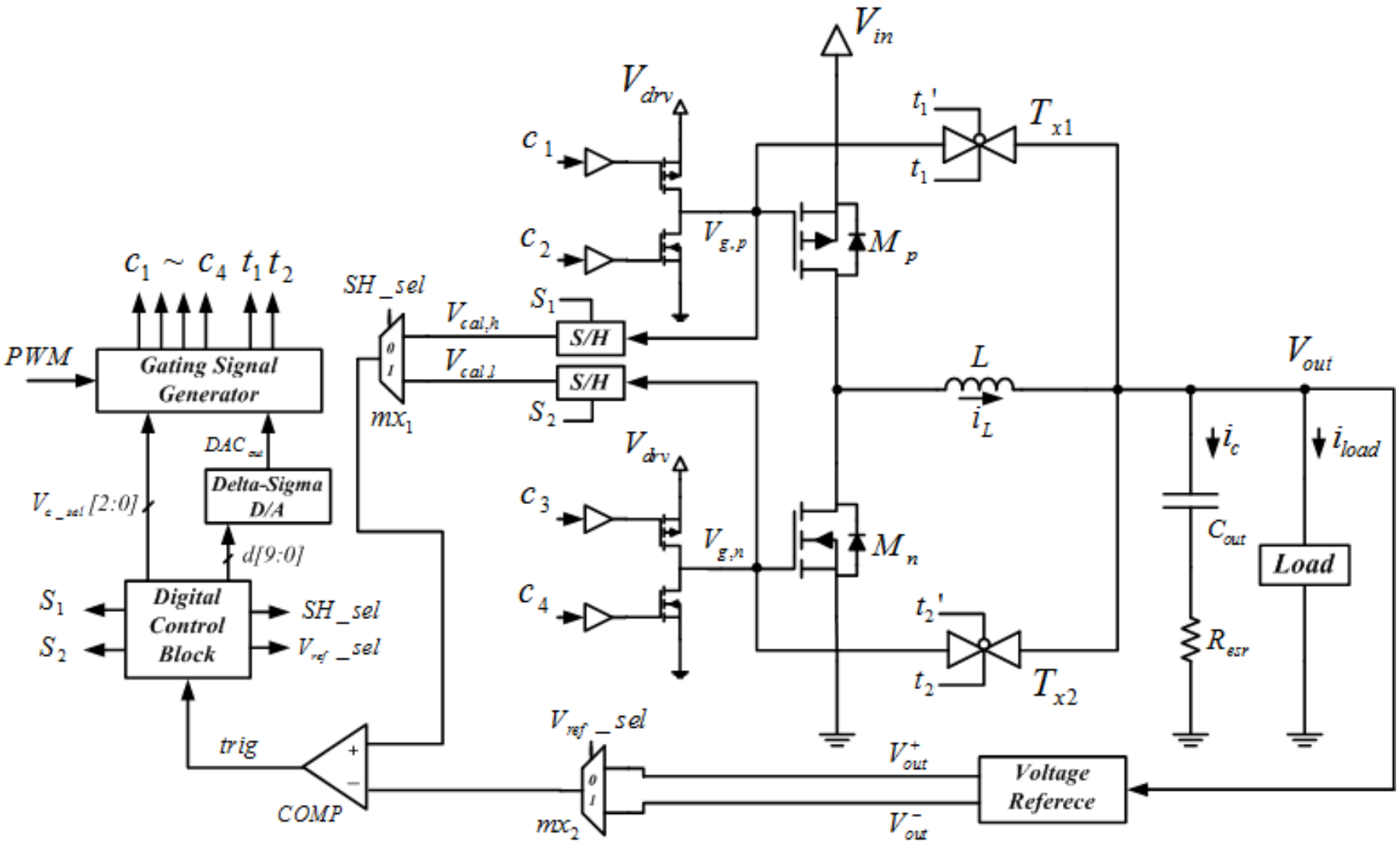


Proposed Gate-Charge Recycling Technique

- Basic control scheme: adjust t_1 so that V_{gate} reaches:
  - V_{out-} at the end of the charge phase
  - V_{out+} at the end of the discharge phase

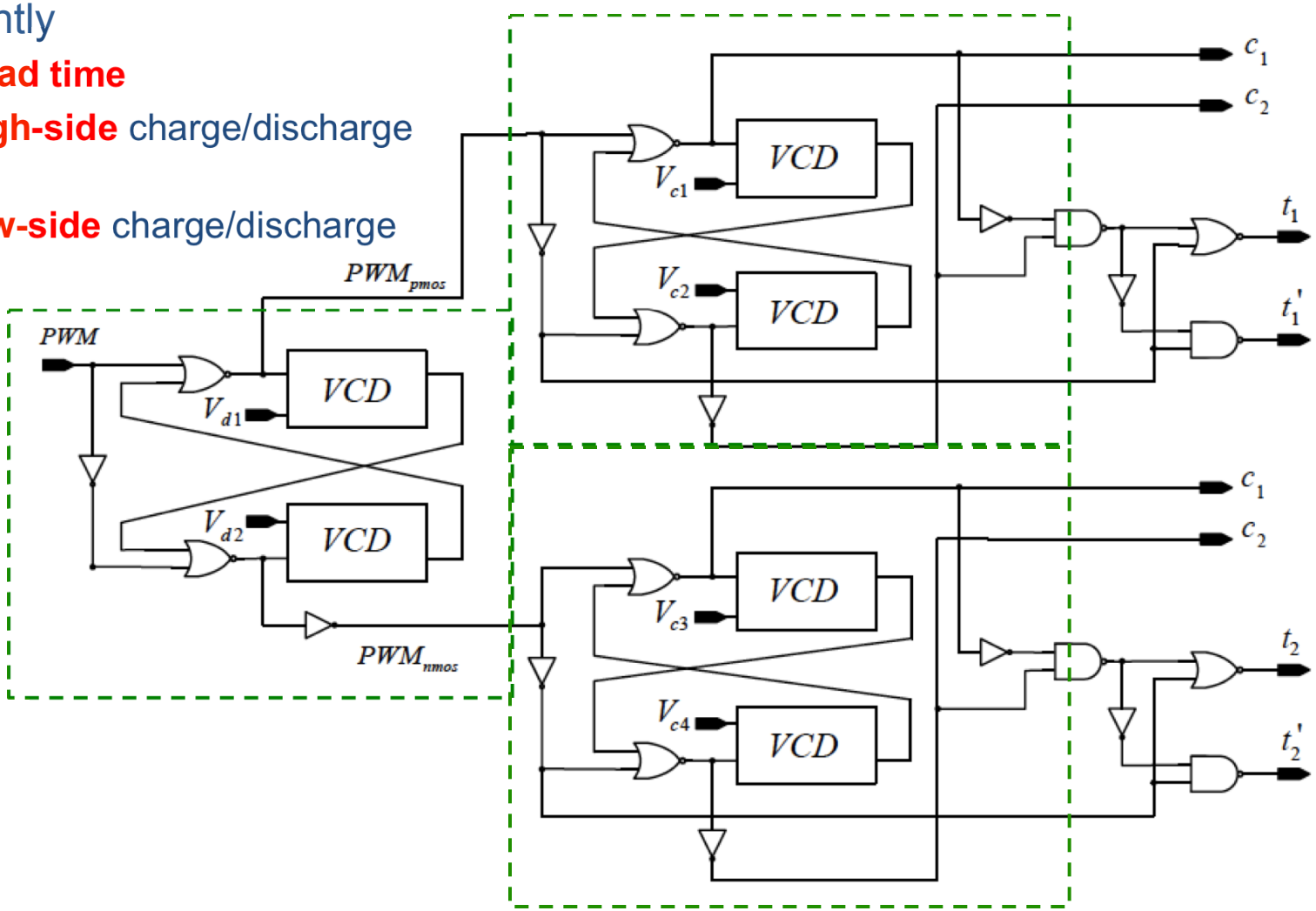


Full System Architecture with Calibration

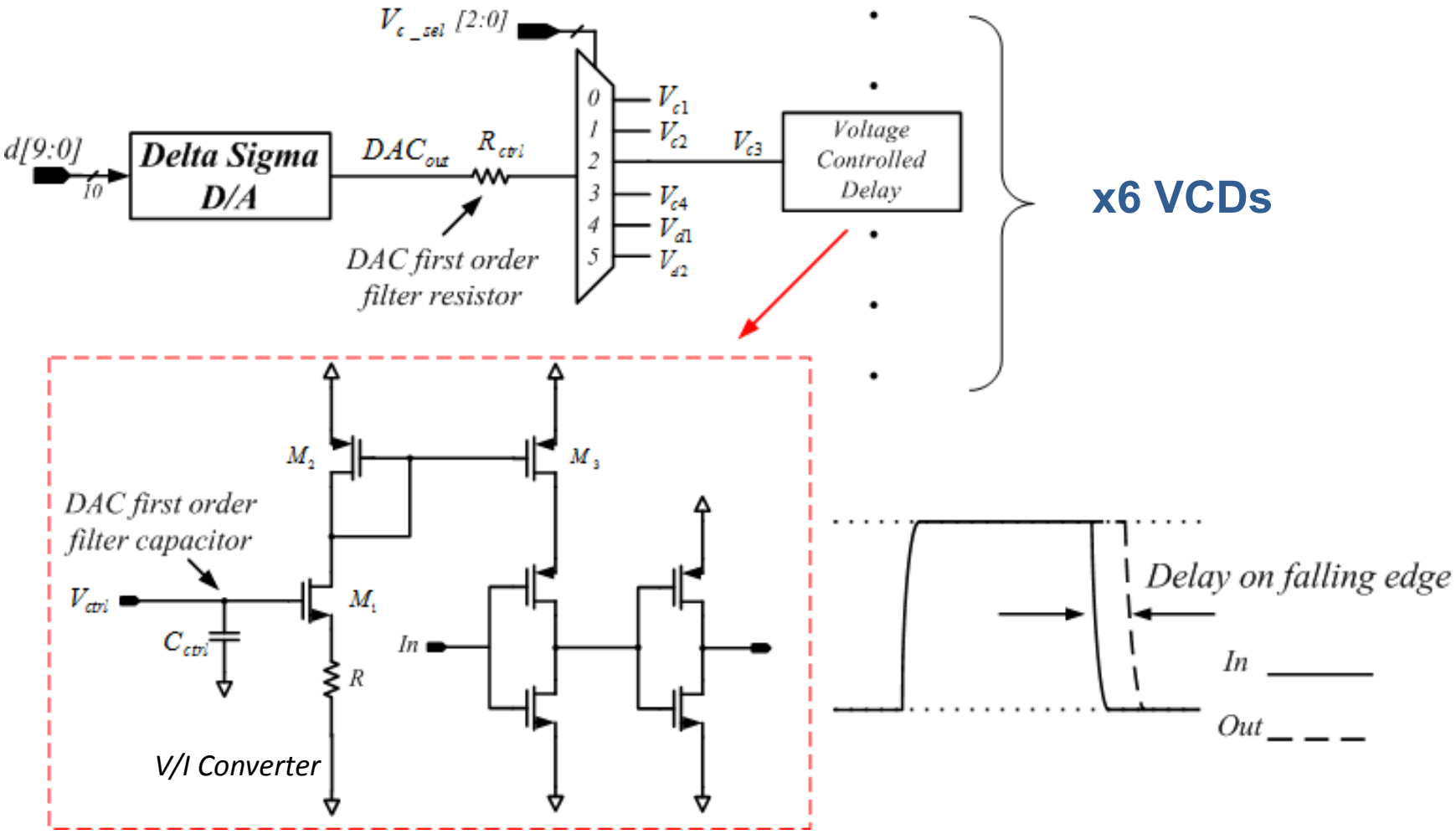


Gating Signal Generator

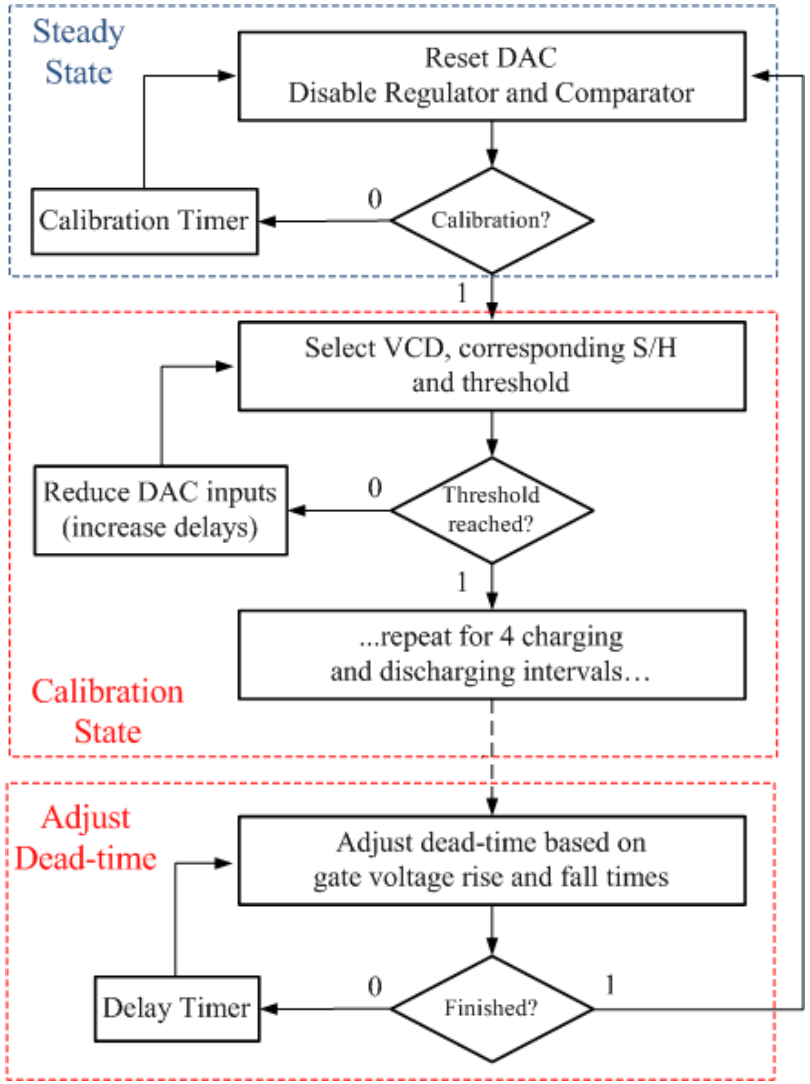
- Total of 6 VCDs are calibrated independently
  - 2 for **dead time**
  - 2 for **high-side** charge/discharge timing
  - 2 for **low-side** charge/discharge



Voltage Controlled Delay



Charge Recycling Calibration Scheme



→ **Charge recycling circuitry is put into sleep mode**

→ **Charge recycling circuitry is operational, which includes:**

- **Comparator**
- **Voltage reference**
- **Delta Sigma D/A**

Converter Specification (designed in 0.13 µm CMOS)

Specification	Value	Units
Input Voltage, V_g	2.5	V
Driver Voltage, V_{drv}	2.5	V
Output Voltage, V_{out}	0.8 to 1.6	V
Rated Load, I_{load}	300	mA
R_{on} for $M_{1,2}$	185, 90	mΩ
Q_{gate} for $M_{1,2}$ @ 2.5V	230, 120	pC
R_{on} for T_{x1} pmos, nmos	1.4, 2.5	Ω
R_{on} for T_{x2} pmos, nmos	2.8, 3.5	Ω
Output Capacitor C_{out}	1	µF
Total Capacitor ESR R_c	10	mΩ
Filter, L	1.5	µH
Inductor DCR, R_L	100	mΩ
Switching Frequency, f_s	20	MHz
DAC Clock Frequency, DAC_{clk}, adjustable	67 to 140	MHz
VCD Range	0.2 to 1.5	ns
Dead-time Range	0.5 to 2	ns
Total calibration time	< 20	µs
Re-calibration period	5	ms

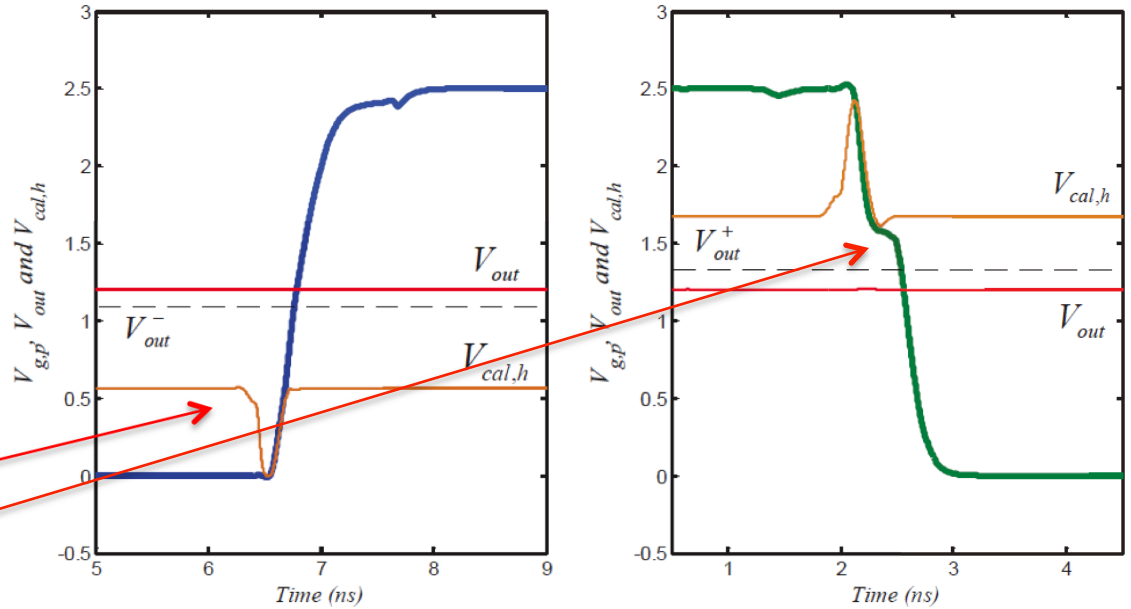
T_{x1} and T_{x2} are < 10x smaller than M_p and M_n

requires calibration every 5 ms

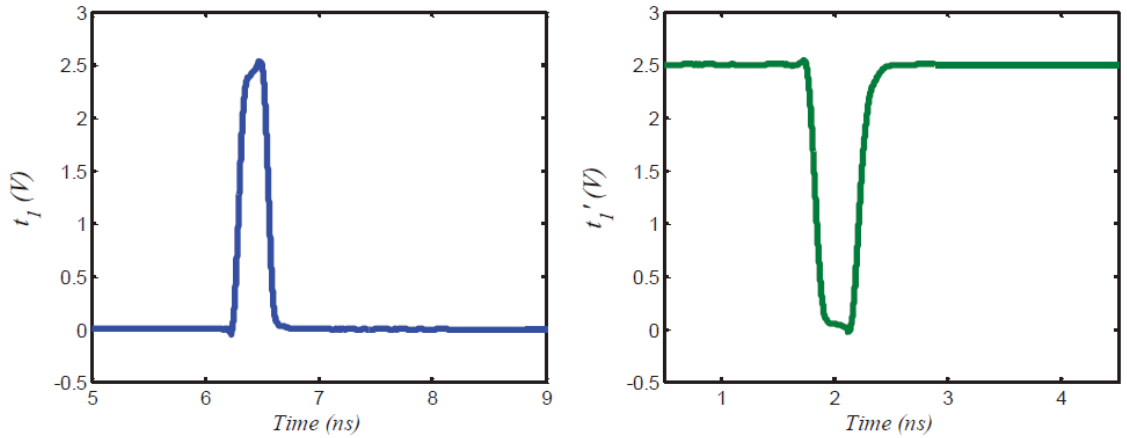
Simulation Results: Before Calibration

High-side MOSFET
Gate drive waveforms:

TX off too soon
(partial charge sharing)
$V_{cal,h} < V_{out}^-$
$V_{cal,h} > V_{out}^+$



Transmission gate
Control:

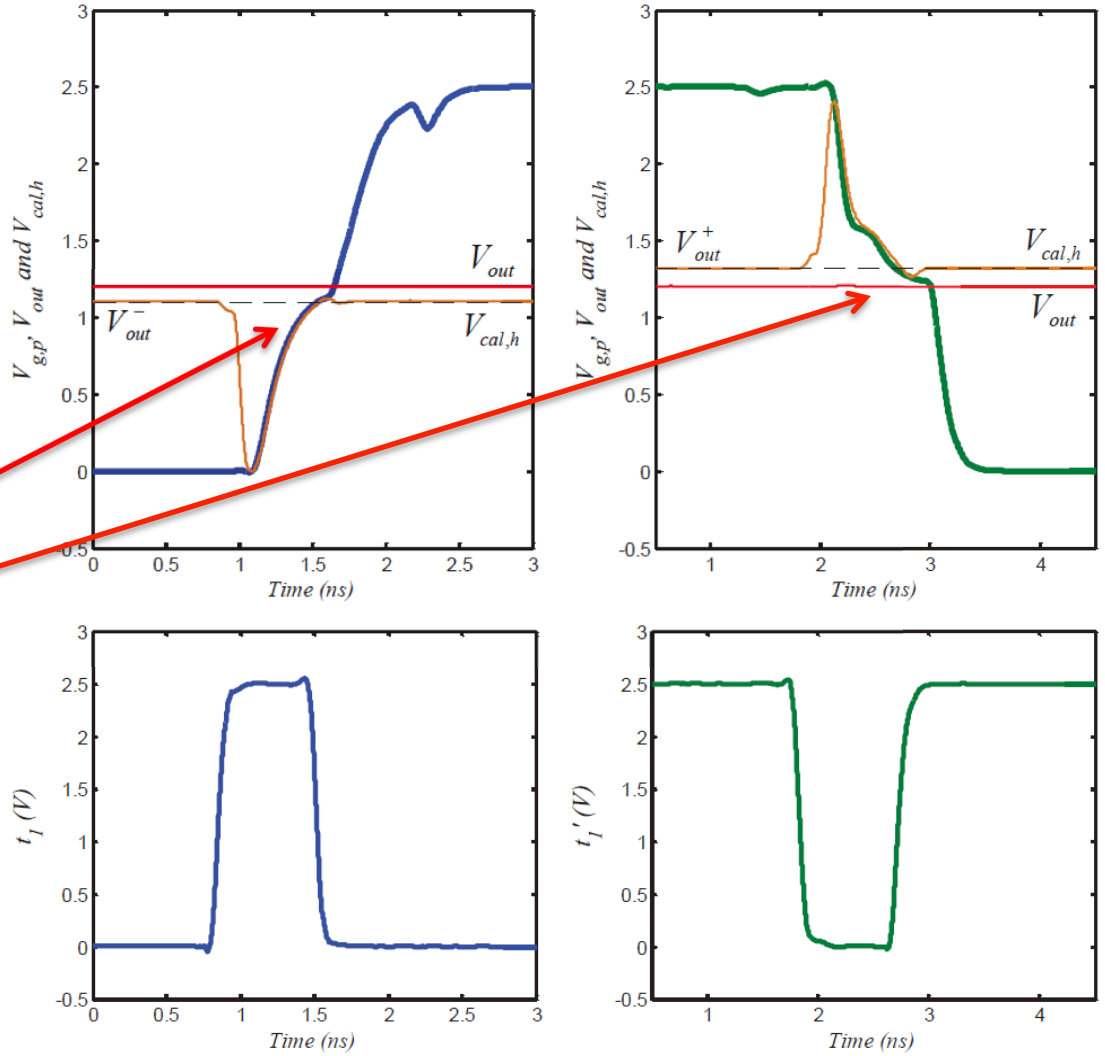


Simulated Waveforms: After Calibration

High-side MOSFET
Gate drive waveforms:

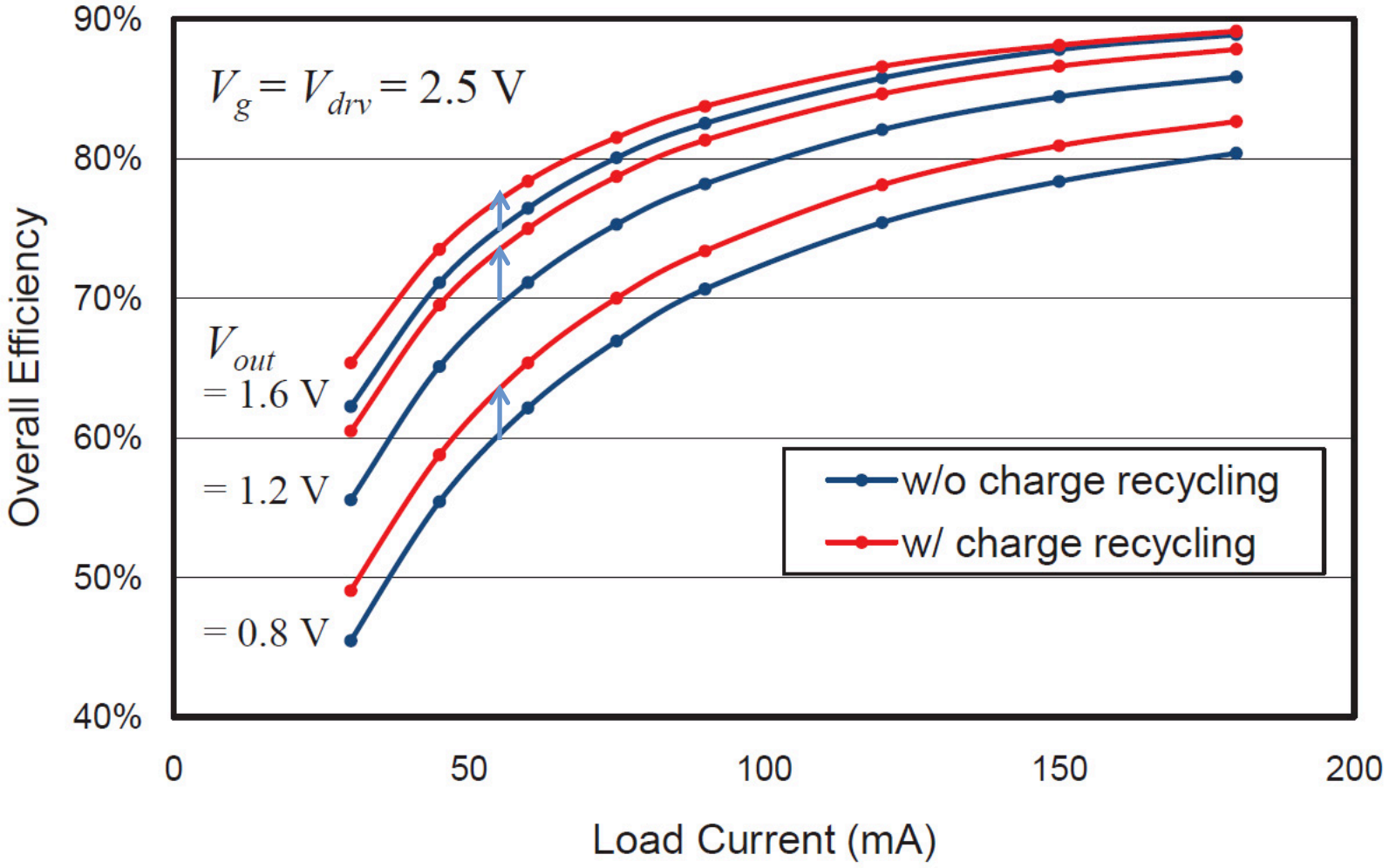
Proper control of TX
$V_{cal,h} = V_{out}^-$
$V_{cal,h} = V_{out}^+$

Transmission gate
Control:



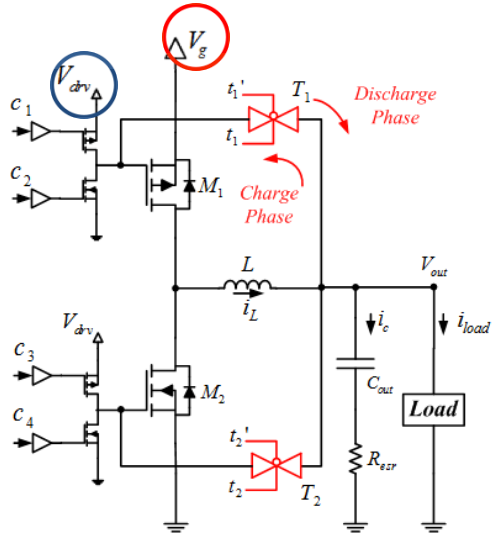
Simulated Overall Efficiency Improvement

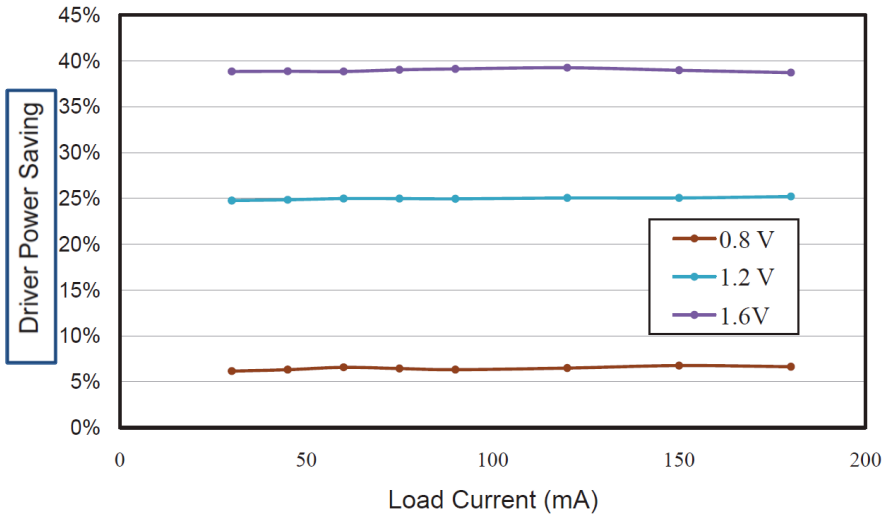
- Efficiency vs. load current from 15-180 mA (closed loop control)
- **25 %** reduction in gate-drive power – 5 % efficiency improvement

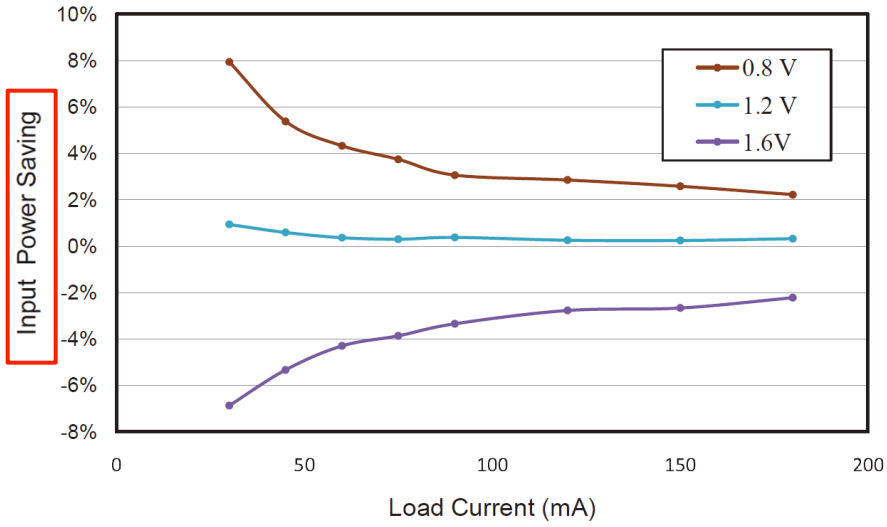


Deeper Look: Power Savings vs. V_{out}, I_{out}

- **V_{out} < ~ V_g/2:**
  - Net charge transfer from V_{drv} to V_{out}
  - Power from V_g is reduced
- **V_{out} > ~ V_g/2**
  - Net charge transfer from V_{out} to V_{drv}
  - Power from V_g is increased

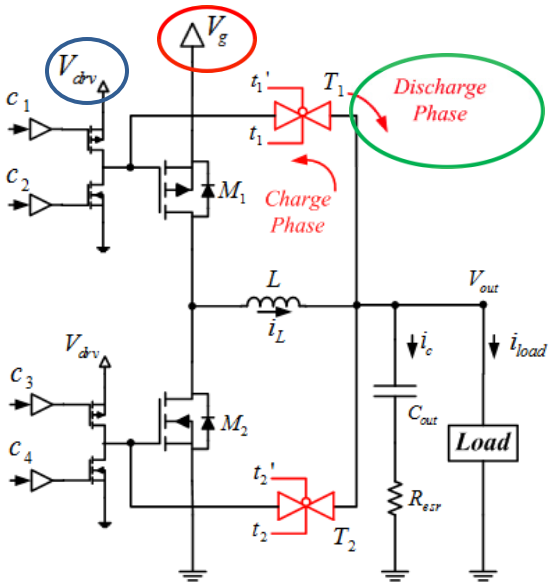


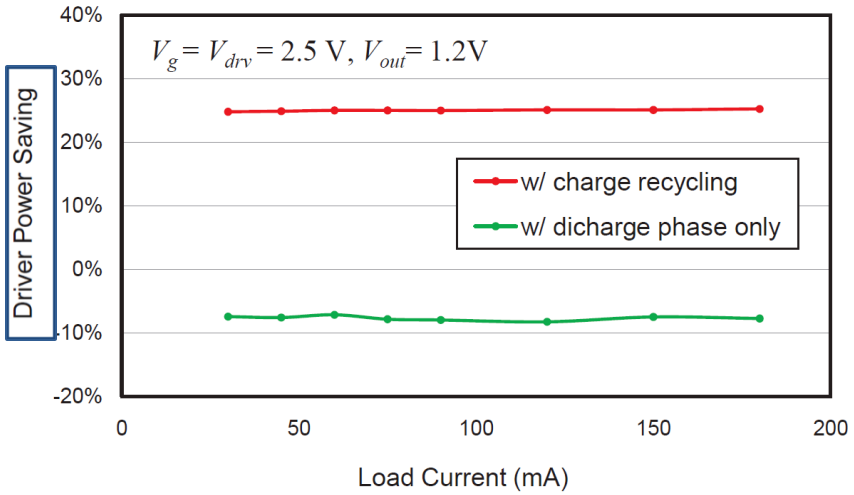


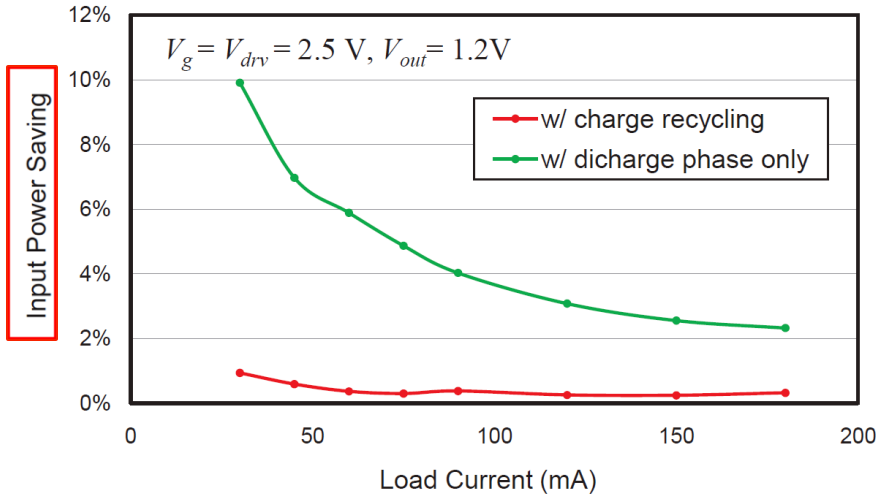


Power Savings with Discharge Phase Only

- Discharge phase provides no savings in driver power
- TX gate is only used once per cycle (potential savings)
- Input power is reduced since the driver power is transferred to the output

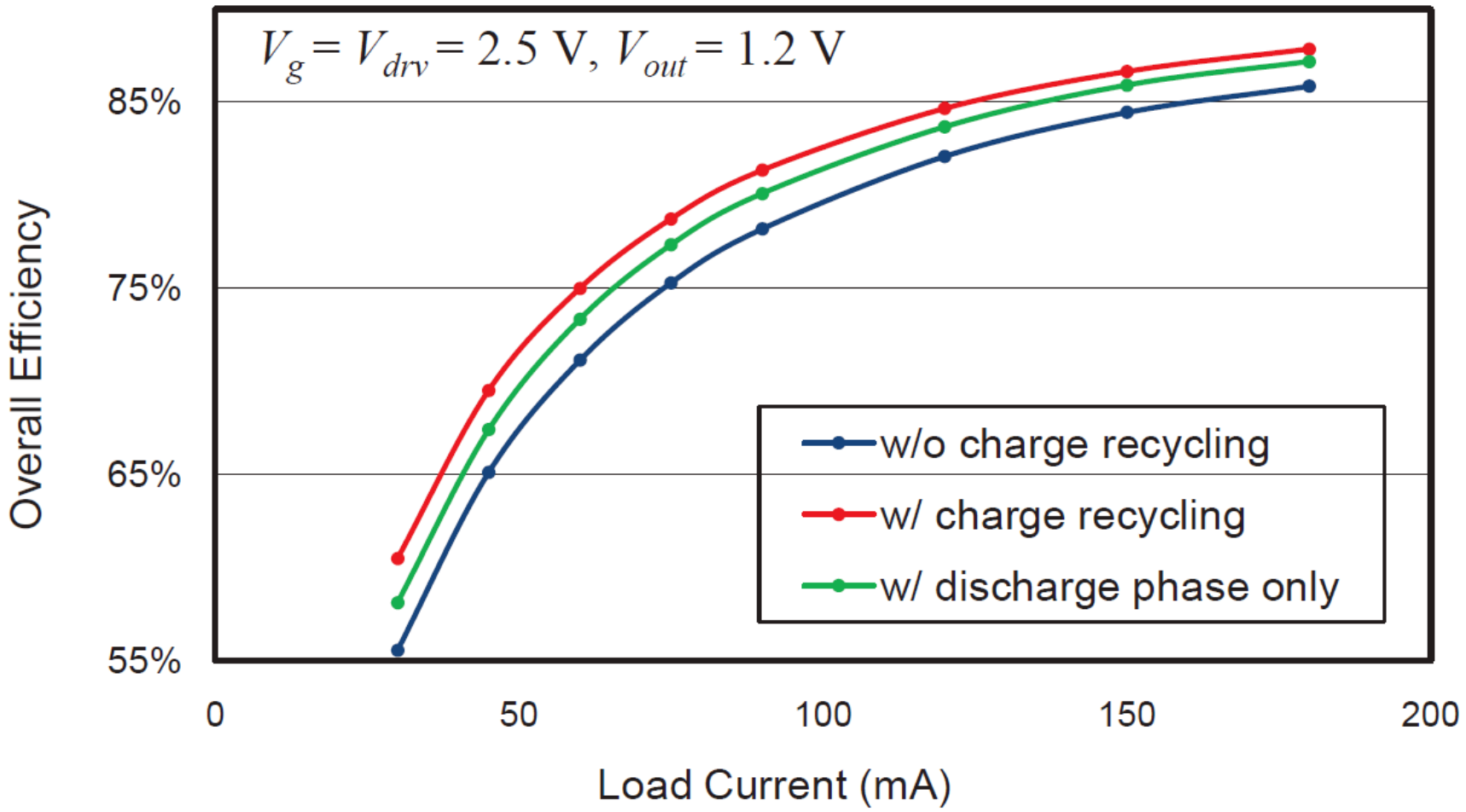






With Discharge Phase Mode Only

- Light-load efficiency curve with discharge phase operating only



Conclusions

- Gate-drive loss becomes significant for dc-dc converters that operates beyond 10 MHz.
  - Over 60% of total loss is gate-driver loss in this 20 MHz converter design
- Gate-charge recycling needs to be achieved by a close-loop control scheme to provide optimal power savings at various operating conditions.
- Compatible with
  - variable frequency techniques (PFM, burst-mode, etc.)
  - adaptive gate swing to achieve further power savings
- The proposed technique provides a solution without additional magnetic components with 5% overall efficiency improvement and equivalent of 25% in driver power saving, without increasing R_{on}
- Conducted EMI from gate driver is moved from input to output
- On-chip experimental results coming soon