Small Area Power Converter for Application to Distributed On-Chip Power Delivery

Eby G. Friedman
Agenda

- Motivation
- Point-of-load voltage regulator
- Distributed on-chip power delivery
- Distributed 3-D rectifier
- Conclusions
Agenda

- Motivation
- Point-of-load voltage regulator
- Distributed on-chip power delivery
- Distributed 3-D rectifier
- Conclusions
Power Delivery in Modern ICs

- Typical power delivery
  - Off-chip power supplies provide current
    - Low quality voltage regulation
      - Slower response time
      - $IR$ and $Ldi/dt$ voltage drops
  - Large number of dedicated I/O pads
    - Increases with the number of voltage domains
Power Delivery in Modern ICs

- **On-chip power delivery**
  - Multi-supply voltage processors
  - Need higher efficiency
    - Reduced parasitic impedances
  - Enhanced voltage regulation
    - Smaller parasitic voltage drops
    - Faster load regulation
  - Size of existing on-chip supplies is large
    - Small voltage regulators are required
Power Delivery in Modern ICs

- Typical power delivery
- On-chip power delivery
- Proposed power delivery

- Smaller on-chip power supplies
- Fast algorithms for power grid analysis
  - More efficient design and analysis of highly complex circuits
- Design methodology for simultaneously placing decoupling capacitors and distributed power supplies
  - Enhanced load regulation
    - Point-of-load voltage regulation
  - Increased power efficiency of overall system
Agenda

- Motivation
- Point-of-load voltage regulator
- Distributed on-chip power delivery
- Distributed 3-D rectifier
- Conclusions
Typical On-Chip Voltage Regulation

- Existing on-chip power supplies
  - Large on-chip area requirement
    - Difficult to implement multiple voltage domains
      - Several power supplies are required
  - Slow response time
    - Parasitic impedances degrade response time
  - High parasitic voltage drop
    - Power supplies are far from the load circuitry
      - Large parasitic impedance between power supply and load circuits
Point-of-Load Voltage Regulation

- Small local point-of-load power supplies solve these problems
  - Small on-chip area
  - Fast response time and low parasitic voltage drop
    - Small parasitic impedance between power supply and load circuitry
      - Voltage is generated close to the load circuitry
  - More robust voltage regulation
    - Small output DC voltage shift for different current demands
      - Maximum output current demand of each power supply is small
Feedback–Active Filter Based Converter

- Feedback is within active filter structure
  - Fast transient response to the load changes
    - Similar to LDO

- Effective regulation of the output voltage
  - Small changes in the supply voltage
    - Sharp output load transients
Choice of Filter Topology

- **Filter types**
  - Butterworth
  - **Chebyshev type I**
  - Bessel
  - Chebyshev type II
  - Elliptic
  - ...

- **Filter configurations**
  - Sallen-Key
    - No DC current path
      - From input to output
      - To the ground
    - Multiple feedback
      - DC current path between input and output
      - No DC current path to ground
    - Twin-t and bridged-t feedback
      - DC current path from input to output
      - DC current path to ground
    - ...

- **Chebyshev type I**
  - Faster transition than Butterworth and Bessel
  - No zeros needed in the transfer function

- **Sallen-Key configuration is used**
  - No DC current path
    - Minimize the static power dissipation
Test Chip – Test Set-Up and Die Photo

- 110 nm CMOS TSMC/Kodak technology
- Five different test circuits have been fabricated
  - Three circuits with internal PWM module to provide the input signal
  - Two circuits with input signals supplied from an off-chip signal generator

Experimental Results - Load Regulation

- Current slope = 1 amp/µs
  - No ringing
    - Stable operation
- Response time = 72 ns

Current efficiency = 99%
# Example DC-DC Voltage Converters

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Type</strong></td>
<td>Buck</td>
<td>LDO</td>
<td>LDO</td>
<td>LDO</td>
<td>SC</td>
<td>SC</td>
<td>Hybrid</td>
</tr>
<tr>
<td><strong>Year</strong></td>
<td>2003</td>
<td>2005</td>
<td>2007</td>
<td>2008</td>
<td>2010</td>
<td>2010</td>
<td></td>
</tr>
<tr>
<td><strong>Technology (nm)</strong></td>
<td>80</td>
<td>90</td>
<td>350</td>
<td>350</td>
<td>45</td>
<td>32</td>
<td>110</td>
</tr>
<tr>
<td><strong>Response time (ns)</strong></td>
<td>87</td>
<td>-----</td>
<td>270</td>
<td>300</td>
<td>120-</td>
<td>1200</td>
<td></td>
</tr>
<tr>
<td><strong>On-chip area (mm²)</strong></td>
<td>12.6</td>
<td>0.098</td>
<td>0.264</td>
<td>0.045 + off-chip capacitor</td>
<td>0.16</td>
<td>0.374</td>
<td>0.026</td>
</tr>
<tr>
<td><strong>V_{out} (V)</strong></td>
<td>0.9</td>
<td>0.9</td>
<td>1.8-3.15</td>
<td>1.0</td>
<td>0.8 – 1.0</td>
<td>0.66 – 1.33</td>
<td>0.9</td>
</tr>
<tr>
<td><strong>ΔV_{out} (mV)</strong></td>
<td>100</td>
<td>90</td>
<td>54</td>
<td>180</td>
<td>-----</td>
<td>-----</td>
<td>44</td>
</tr>
<tr>
<td><strong>I_Q (quiescent current) (mA)</strong></td>
<td>-----</td>
<td>6</td>
<td>0.02</td>
<td>0.095</td>
<td>-----</td>
<td>-----</td>
<td>0.38</td>
</tr>
<tr>
<td><strong>I_{max} (mA)</strong></td>
<td>9500</td>
<td>100</td>
<td>200</td>
<td>50</td>
<td>8</td>
<td>205</td>
<td>140</td>
</tr>
</tbody>
</table>


Agenda

- Motivation
- Point-of-load voltage regulator
- Distributed on-chip power delivery
- Distributed 3-D rectifier
- Conclusions
Interactions within On-Chip Power Grid

- Complicated interactions
  - Tens of power supplies
  - Hundreds of decoupling capacitors
  - Millions of load circuits
Simultaneous Co-Design Methodology for Effective Power Delivery

- A change in the design process of power distribution networks is necessary
  - Increased number of on-chip power supplies
  - Increased number of on-chip voltage islands
  - Stringent noise constraints with supply voltage scaling

- Efficient co-placement of power supplies and decoupling capacitors
  - Reduced power dissipation and power/ground noise
    - Reduce thermal problems
  - Decrease the total size of the required decoupling capacitors to maintain a target noise constraint
  - Multi-voltage design process will be easier

- Need fast and efficient algorithm for synthesis
Closed-Form Expressions of Effective Impedance

- Infinite uniform resistive grid
  - Identical resistance, R

- Models power or ground distribution network

- Effective resistance between arbitrary points is utilized in power grid analysis

**Exact solution**

\[
R_{(A,B)} = \int \frac{(2 - e^{\imath n \alpha} \cos(n \beta) - e^{\imath m \alpha} \cos(m \beta))}{\sinh(\alpha)} \, d\beta
\]

**Asymptotic solution**

\[
R_{(A,B)} = \frac{1}{2 \pi} \ln(n^2 + m^2) + 0.51469
\]

* Maximum error < 3% (for an adjacent node)

---

Point-of-Load Supply vs. Decoupling Capacitance

<table>
<thead>
<tr>
<th></th>
<th>On-chip power supply</th>
<th>On-chip decoupling capacitor</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Area</strong></td>
<td>Greater area requirement</td>
<td><strong>Smaller</strong> area requirement</td>
</tr>
<tr>
<td><strong>Response time</strong></td>
<td>Slower response</td>
<td><strong>Faster</strong> response</td>
</tr>
<tr>
<td><strong>Power efficiency</strong></td>
<td>Limited efficiency due to the active devices and parasitic impedances</td>
<td>Power loss <strong>only</strong> due to parasitic impedances</td>
</tr>
<tr>
<td><strong>Maximum supplied current</strong></td>
<td><strong>High</strong></td>
<td>Limited to the size of the capacitor. Decay and recharge rate of the capacitor should be considered</td>
</tr>
</tbody>
</table>

- Developed fast algorithm for power grid analysis
  - Reduces the time required to optimize the locations of multiple power supplies and decoupling capacitors
  - Considers physical distance among circuit components and power grid characteristics in the co-placement methodology
  - Incorporates the distinctive properties of the power supplies and decoupling capacitors

Simplified Model of Power Grid Interactions

- **Physical separation** affects the current supplied from the
  - Power supplies
  - Decoupling capacitors

\[ I_l = i_{dl} + i_{pl} \]

\[ i_{dl} = \frac{i_{pl}\left(R_{pl} + L_{pl}\frac{dV_c(t)}{dt}\right) - CR_{vd}\frac{dV_c(t)}{dt} - CL_{vd}\frac{d^2V_c(t)}{dt^2}}{R_{vd} + R_{dl} + (L_{vd} + R_{dl})\frac{dV_c(t)}{dt}} \]
Effective Region of Influence of Power Sources

- Effective region exhibits elliptic shape
  - Long radius is determined by the effective impedance among components

\[ r_l = \frac{K \times C}{R_{(x_1, y_1)} + k \times L_{(x_1, y_1)}} \]
Elliptic Shape of Effective Region

- Power supply
  - Connected at $N_{(10,10)}$
- Four decoupling capacitors
  - Connected at $N_{(6,14)}$, $N_{(17,17)}$, $N_{(5,5)}$, and $N_{(18,2)}$
- Load current
  - Uniformly distributed
  - $t_r \rightarrow 100$ ps
  - $t_f \rightarrow 300$ ps

- SPICE simulation
  - $r_{i_2}/r_{i_4} = 1.2$
- Analytic model
  - $r_{i_2}/r_{i_4} = 1.15$
  - Error < 5 %
Effect of Load Characteristics on Effective Region

- **Four power supplies**
  - Connected at $N(3,10)$, $N(10,3)$, $N(10,17)$, and $N(16,10)$

- **Five decoupling capacitors**
  - Connected at $N(3,3)$, $N(3,17)$, $N(10,10)$, $N(17,3)$, and $N(17,17)$

- **Effective regions strongly depend on**
  - Transition times of load devices

- **Decoupling capacitors are more effective**
  - When transition time of load current is faster

- **On-chip power supplies are more effective**
  - When transition times are slower
Agenda

- Motivation
- Point-of-load voltage regulator
- Distributed on-chip power delivery
- Distributed 3-D rectifier
- Conclusions
Specialized circuits for integrated power supply within 3-D structures
Distributed 3-D Rectifier

- Exploits the rectifier portion of a buck converter
  - Generates and distributes power supplies in 3-D integrated circuits
  - Eliminates the need for on-chip inductors
- Rectifier is composed of transmission lines
  - Terminated with lumped capacitances
- Inter-plane structure is connected by 3-D vias
- Low pass behavior
  - $RC$-like characteristics
Transfer Function Comparison

- Both filters exhibit similar characteristics in the MHz frequency range
  - **LC filter**
    - Inductor ESR
    - Output resistance of power MOSFETs
  - **Distributed filter**
    - Interconnect resistance
    - Output resistance of power MOSFETs
    - Multiple poles due to distributed nature of the filter
    - Simultaneous current distribution and signal filtering
Rectifier Design

- 5% voltage ripple
- Equal interconnect lengths on each plane
- Equal capacitors on each plane
- Length = 1 mm
  - 100 lines in parallel
- C = 4.2 nF/plane
  - 10 fF/μm²
- Area
  - 0.42 mm²/plane

\[
V_{pp} = 4.4\% \text{ of } V_{dd2}
\]
Schematic of Distributed 3-D Rectifier
3-D Power Delivery Test Circuit

Power distribution networks
Distributed rectifier

On-chip capacitors

Plane C (upper)
Plane B (middle)
Plane A (bottom)

Interconnects
Switched current loads
Interconnects

Ring oscillators and buffers
Power supply noise measurement circuit
Density of On-Chip Capacitance

- Capacitive density
  - 10 fF/μm² in the MITLL 150 nm 3-D technology
  - Increases with technology

Circuit area is reduced to 0.08 mm²
Agenda

- Motivation
- Point-of-load voltage regulator
- Distributed on-chip power delivery
- Distributed 3-D rectifier
- Conclusions
Conclusions

- An ultra-area efficient on-chip voltage regulator appropriate for point-of-load implementation
  - 0.026 mm² on-chip area
  - > 99% current efficiency
  - Fast response time, 72 ns
  - Low DC voltage shift, 44 mV (< 5%)
    - At maximum current demand
- Simultaneous co-placement of point-of-load local power supplies and decoupling capacitors
  - Exploits similarities and differences between power supplies and decoupling capacitors
  - Determines the effectiveness regions considering
    - Physical distances among components
    - Power/ground parasitic impedances
  - Work in progress
- Distributed power supply for 3-D ICs
  - Exploits the distributed passive filter and TSVs within a 3-D system
  - Currently in test