



Magnetics on Wafer
Transitioning From Prototype to Manufacturing

International Workshop on Power Supply on Chip

Session 4a: Integrated Passives: Magnetics

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Overview

◆ Today Ready for Commercialization

- Magnetic Material on Silicon
 - CMOS compatible fabrication process
 - 20 MHz and higher operation
- DC-DC Device With Integrated Inductor
 - Assembly using existing MCM manufacturing process
 - Standard JEDEC qualification & reliability tests
- Targets
 - Operating voltages 5V or below
 - Output power 10W or below
 - Low profile, small footprint, low cost

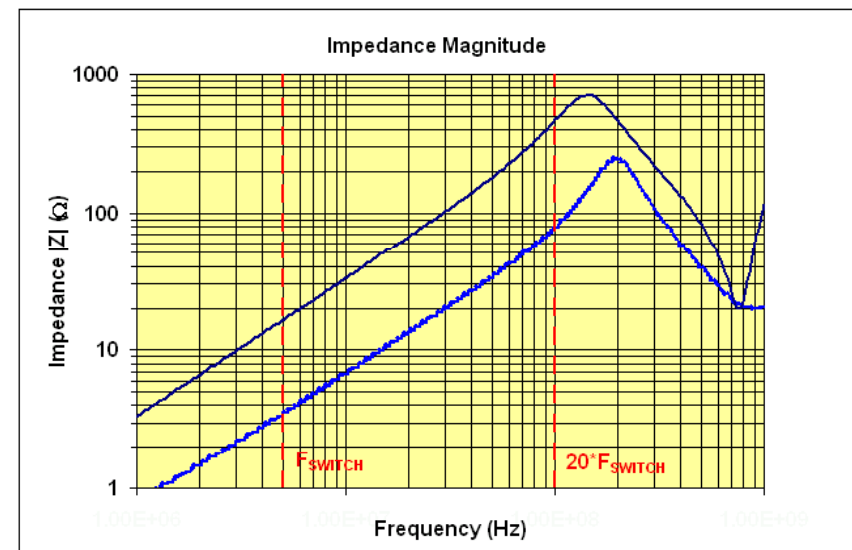
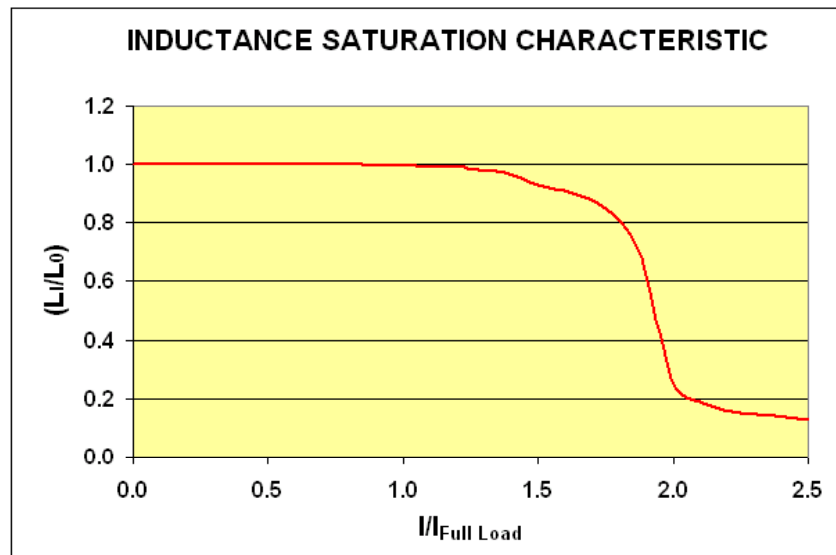
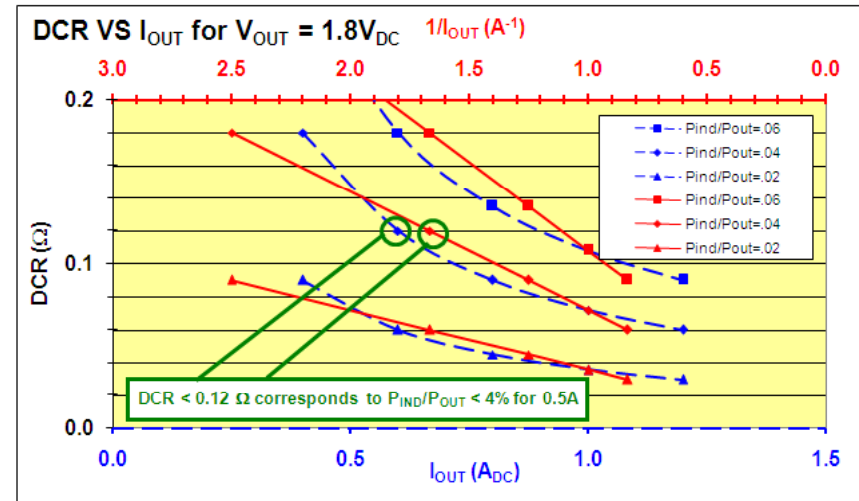
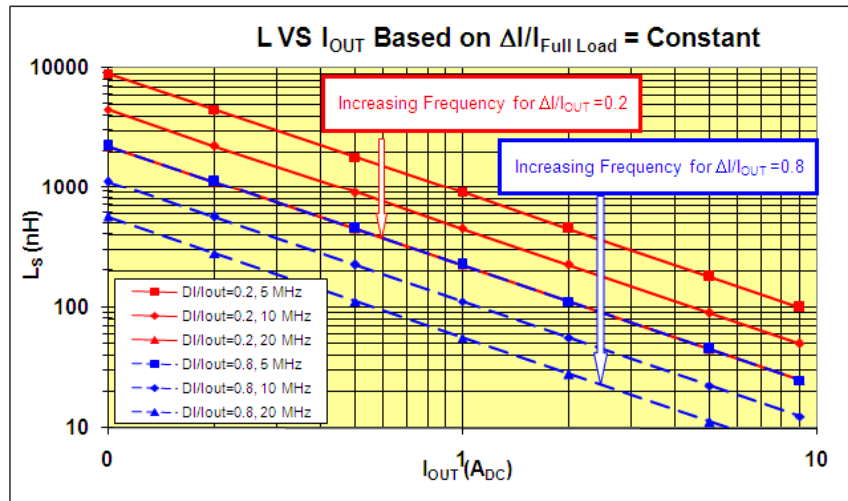
◆ Tomorrow In Development

- Continue to Increase Level of Integration
- Magnetic Material and Conductors on Silicon
- Migrate Multiple Die to Monolithic Single Die

Agenda

- ◆ Motivation
- ◆ Trend Lines for Usable Electrical Parameters
- ◆ Manufacturing Strategy For Commercialization
- ◆ Manufacturing Process Challenges
- ◆ Next Steps
- ◆ Summary

Traditional Inductor Design Criteria (Electrical Parameters)



Inductor Design Criteria

(Surveying Small Signal Parameters to Fit Power Loss Budget)

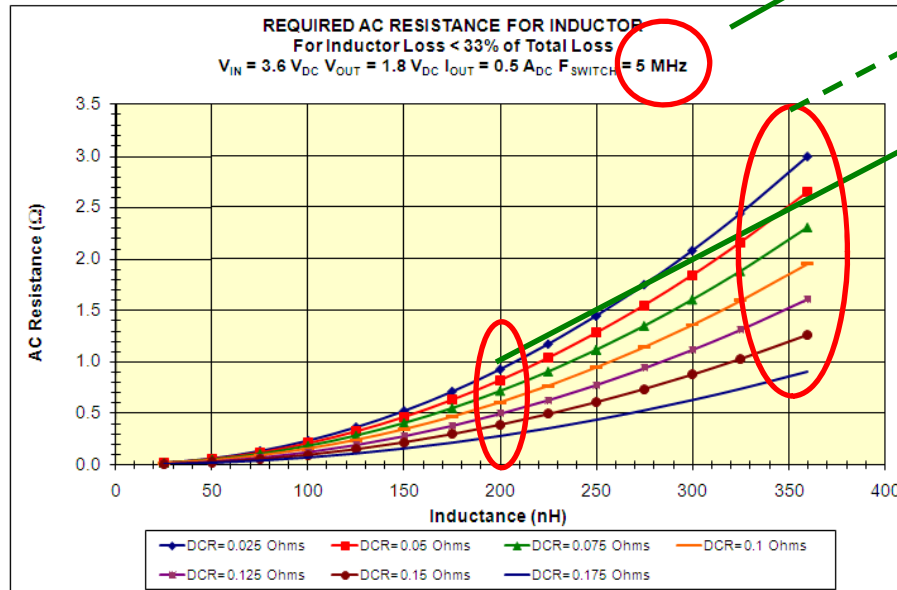
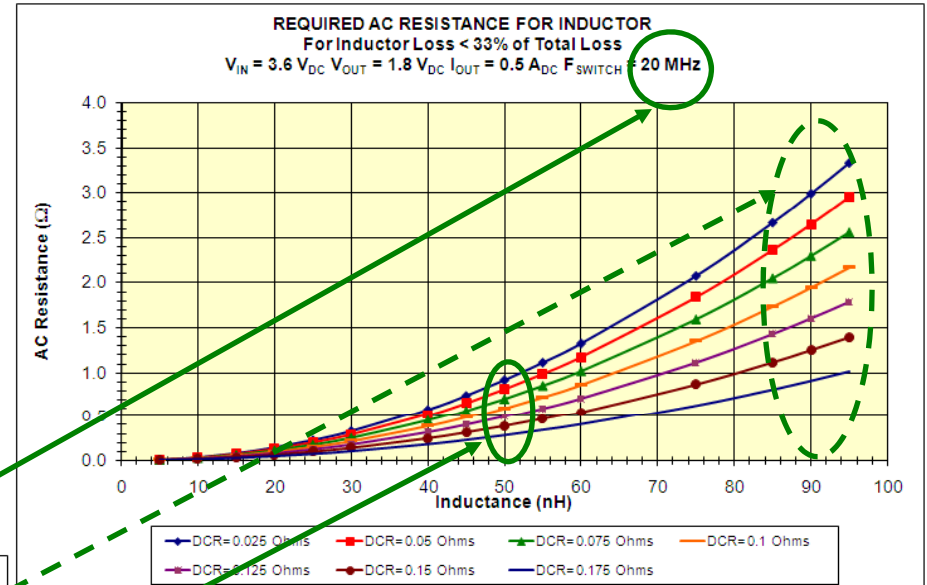
5 MHz

$$L_S = 200 \text{ nH DCR} = 0.1 \Omega$$

$$R_S = 0.6 \Omega$$

$$L_S = 360 \text{ nH DCR} = 0.1 \Omega$$

$$R_S = 2.0 \Omega$$



20 MHz

$$L_S = 50 \text{ nH DCR} = 0.1 \Omega$$

$$R_S = 0.6 \Omega$$

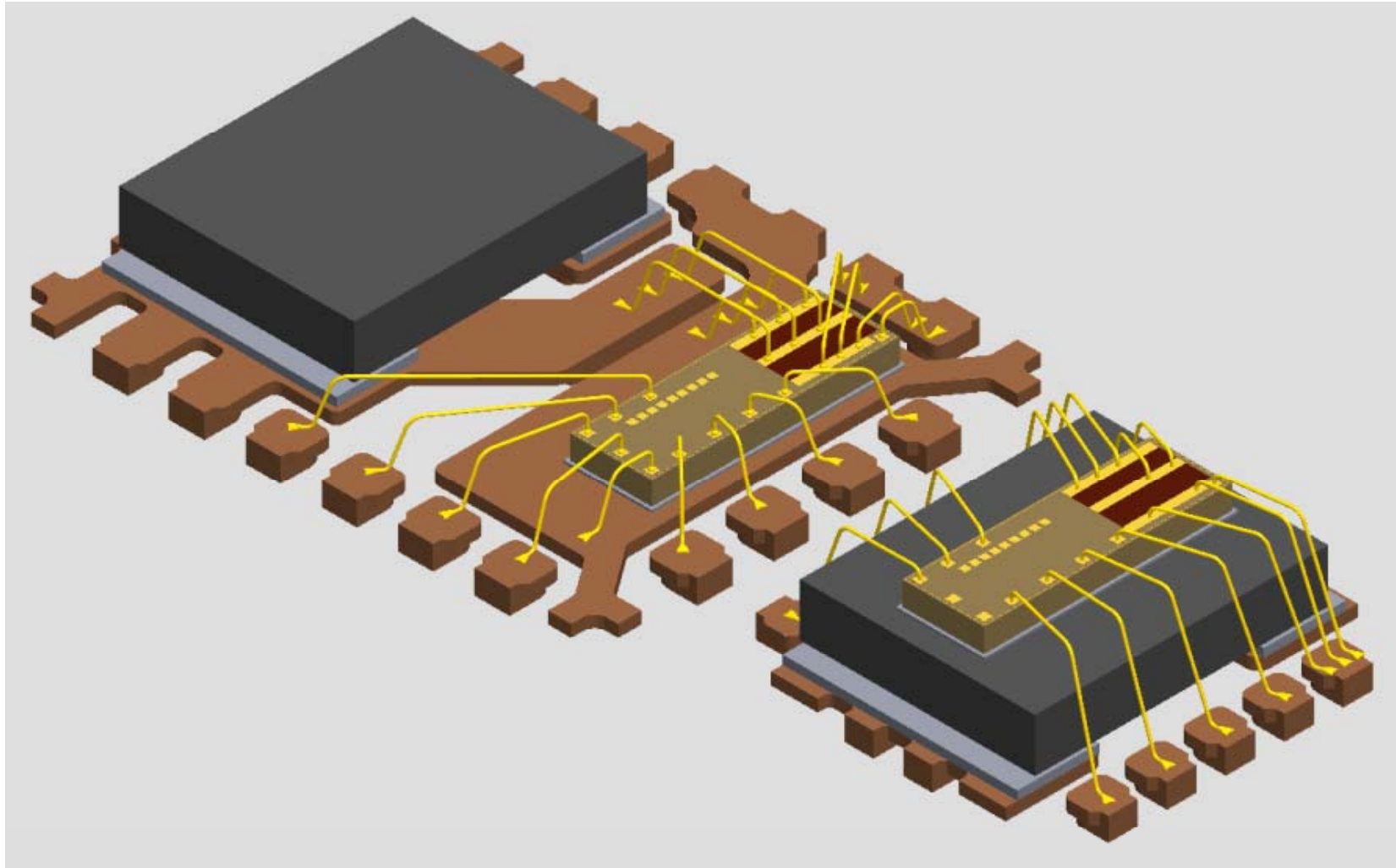
or

$$L_S = 90 \text{ nH DCR} = 0.1 \Omega$$

$$R_S = 1.9 \Omega$$

PSiP Construction: In Volume Manufacture Today

(Side by Side Vs Stacked Assembly Approach)



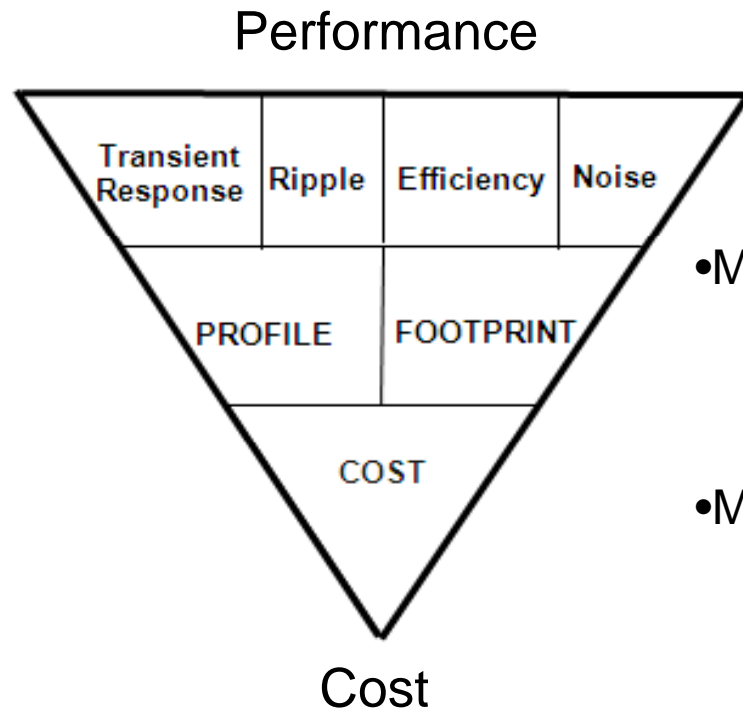
MAGNETICS ON WAFER

(Commercialization Strategy)

- ◆ Continue the Integration Trend Established by PSiP
 - Address size and performance that are beyond limits of discrete magnetics
 - Low profile
 - Noise performance
 - Transient performance
 - Device footprint
- ◆ Initially Target Products to
 - Proliferate aspect ratio (inductor footprint), turns (inductance, DCR, current rating, power losses) to accommodate different applications
 - Establish the process control, quality and reliability track records
- ◆ Develop Technical Improvements as the Manufacturing Process Matures
 - Layering of magnetic and conductor layers
 - Improve technical performance

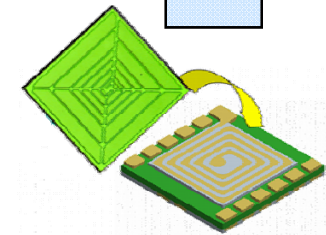
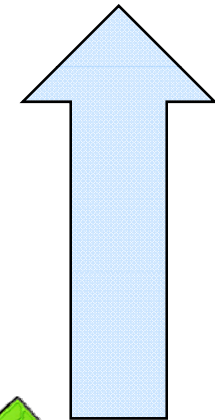
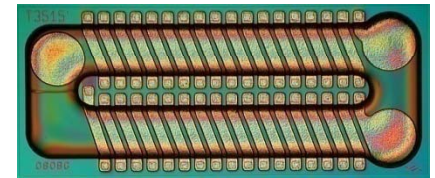
Wafer Level Inductor Construction

(Fabrication Options [Design Trade-Offs])



- Magnetic/Conductor Structure
 - Toroid
 - Shell (sandwiched)
 - Planar Coil with Mirror
 - Meander
- Magnetic Structure
 - Multi Layer (Laminated)
 - Single Layer
- Magnetic Anisotropy
 - Annealed
 - Geometric
 - None

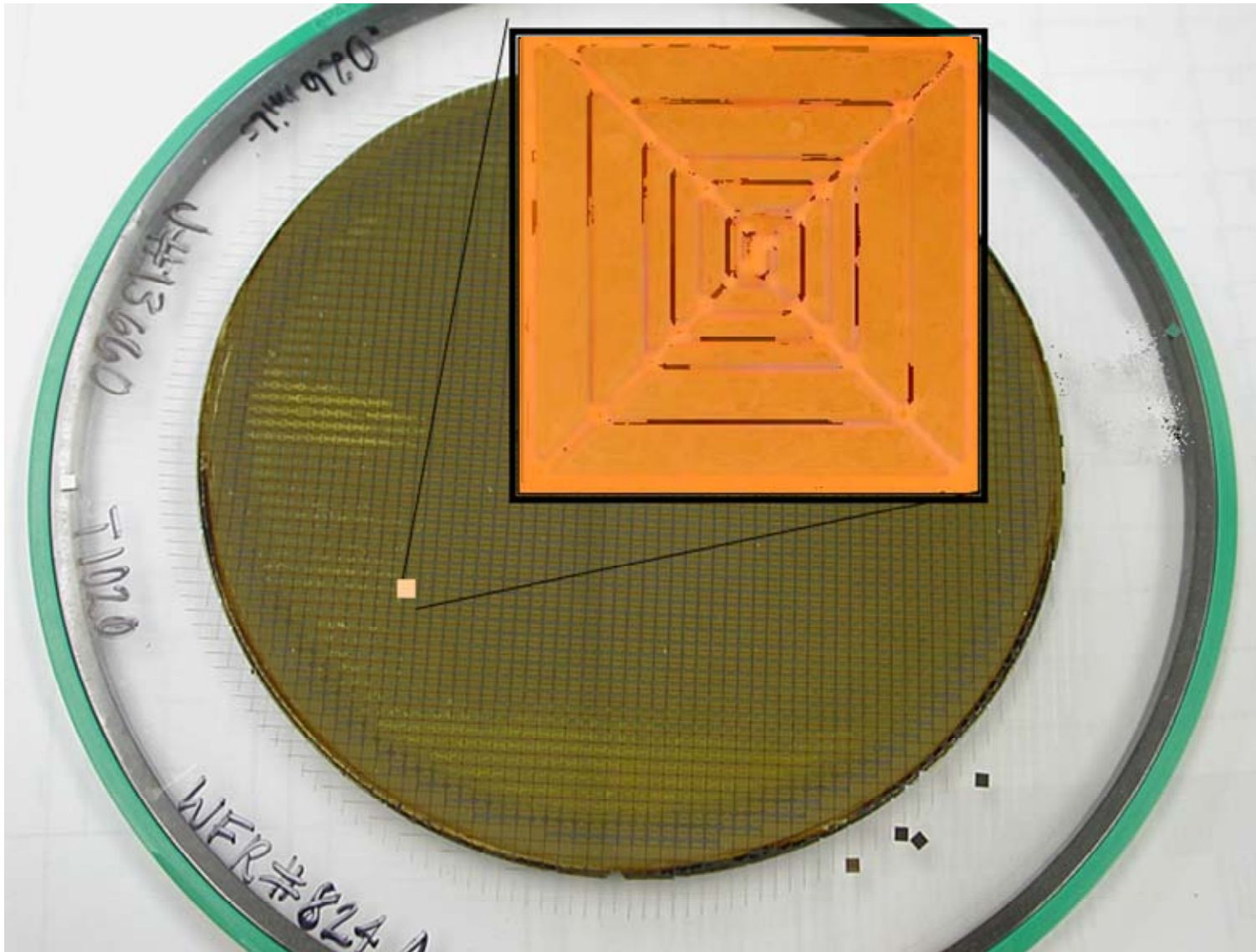
COMPLEX



SIMPLE

Technology Enabling Magnetic Material On Silicon

(Wafer Level Magnetics Approach thru Manufacturing Trials and Qualification)



Manufacturing Process Challenges For Magnetic Alloy (Wafer Manufacturing Process)

◆ Stress

- Impact on front end assembly processes – back grind, dicing
- Impact on electrical characteristics

◆ Magnetic Alloy Consistency

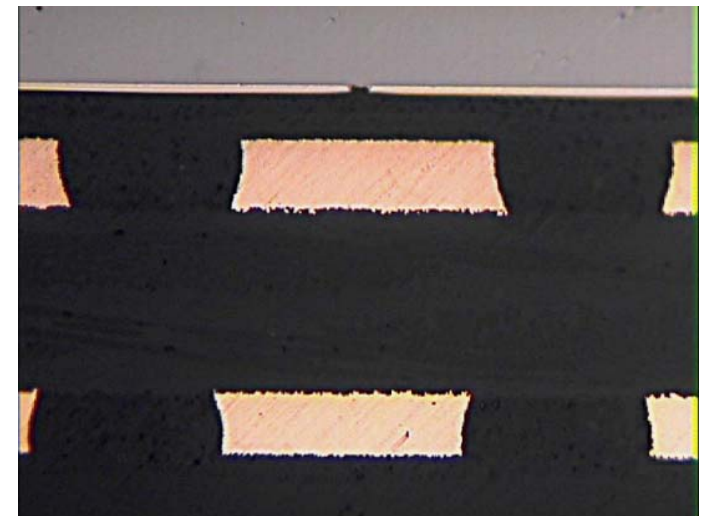
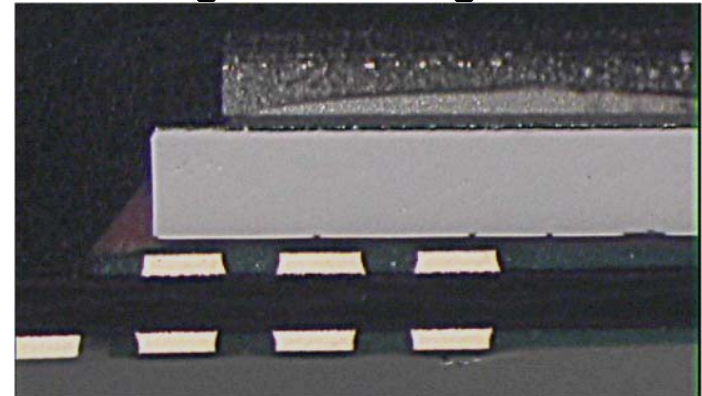
- Composition
- Thickness

◆ Optical Inspection Standards

- Impact on electrical performance
- Impact on reliability

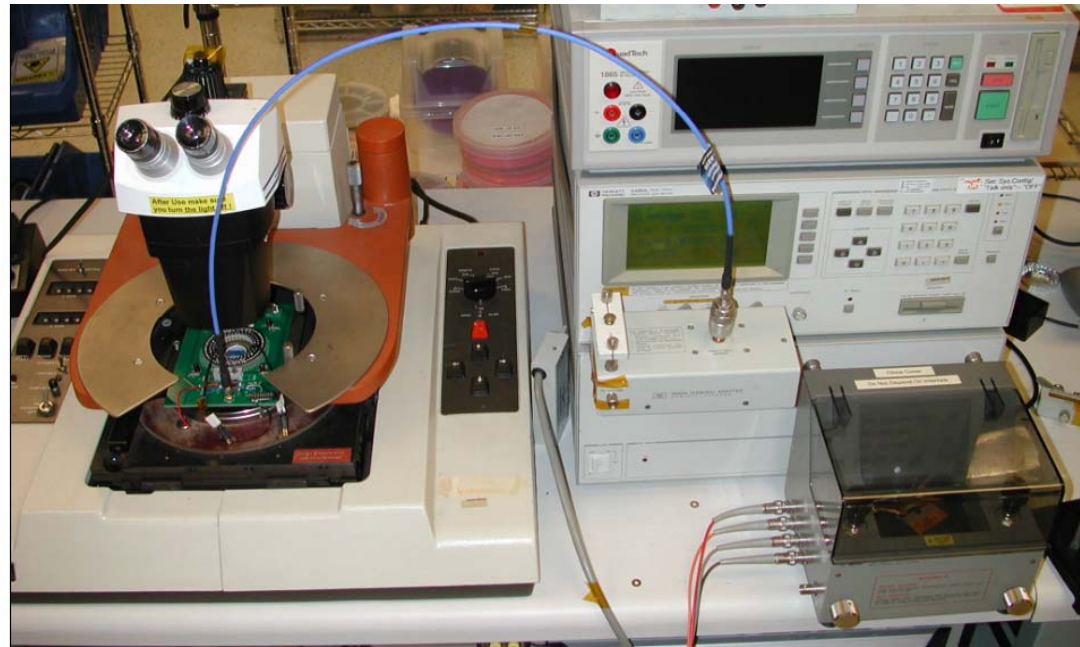
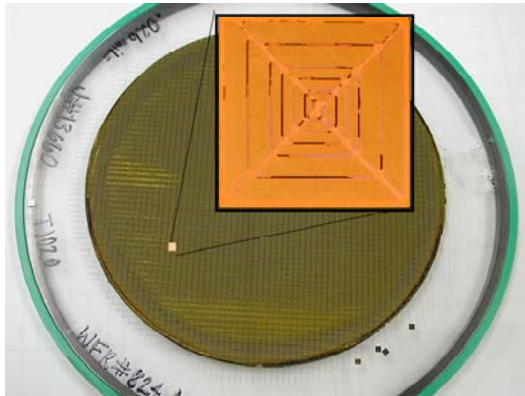
◆ Electrical Parameter Verification

- Magnetic Coupling (magnetic material)
- Galvanic Connection (inductor on wafer)



Manufacturing Process Challenges

(Wafer Manufacturing Process – Electrical Verification)



Manufacturing Process Challenges

(Effects of Magnetic Alloy Thickness Variation)

◆ L_0 Distribution

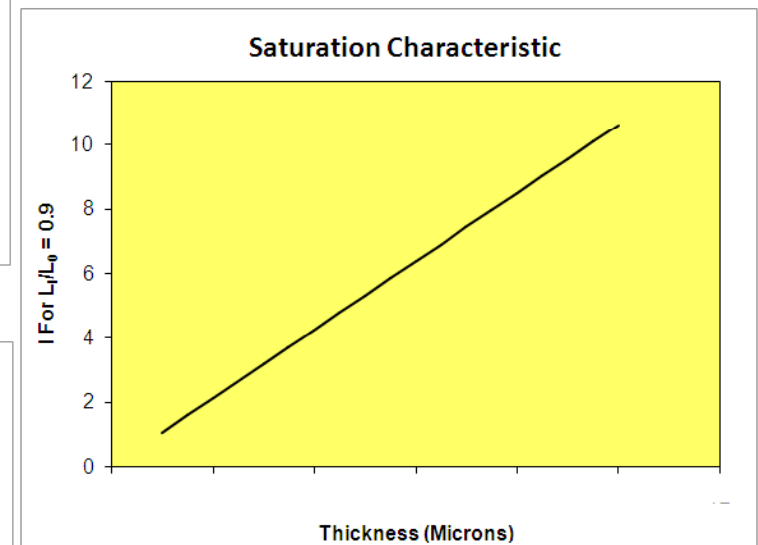
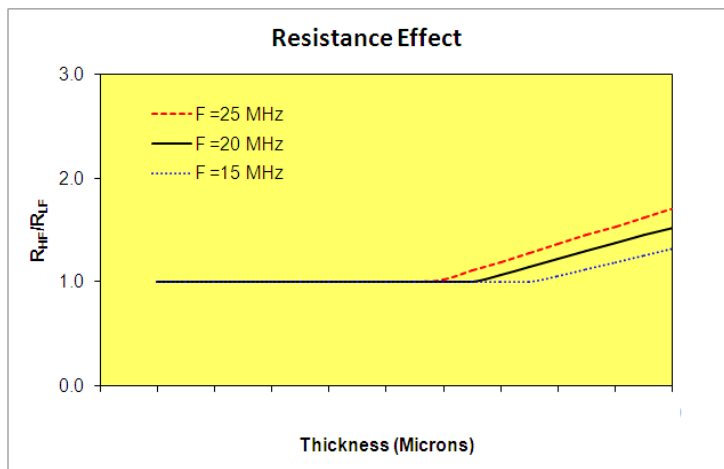
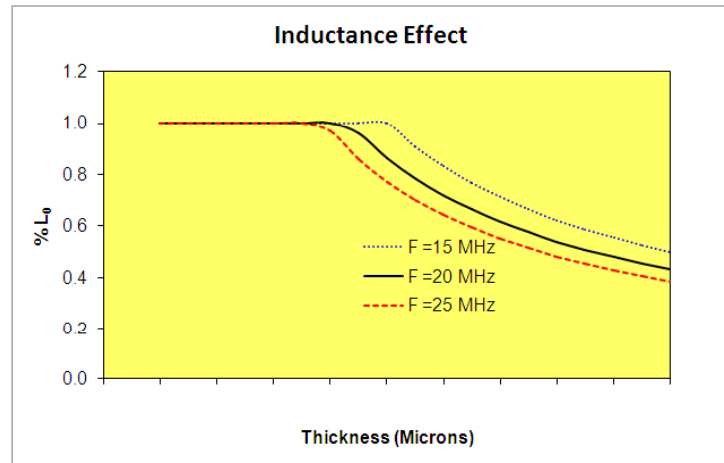
- Thick ↑
- Thin ↓

◆ L Vs I

- Thick ↑
- Thin ↓

◆ L_s & R_s Vs F

- Thin ↑
- Thick ↓



Manufacturing Process Challenges For Magnetic Alloy

(Device Packaging & PWB Assembly Processes)

◆ Temperature Stress

- Die Attach Cure
- Wire Bonding
- Molding
- JEDEC Reliability Standards

◆ Physical Stress

- Encapsulation Compound
- Temperature Cycle

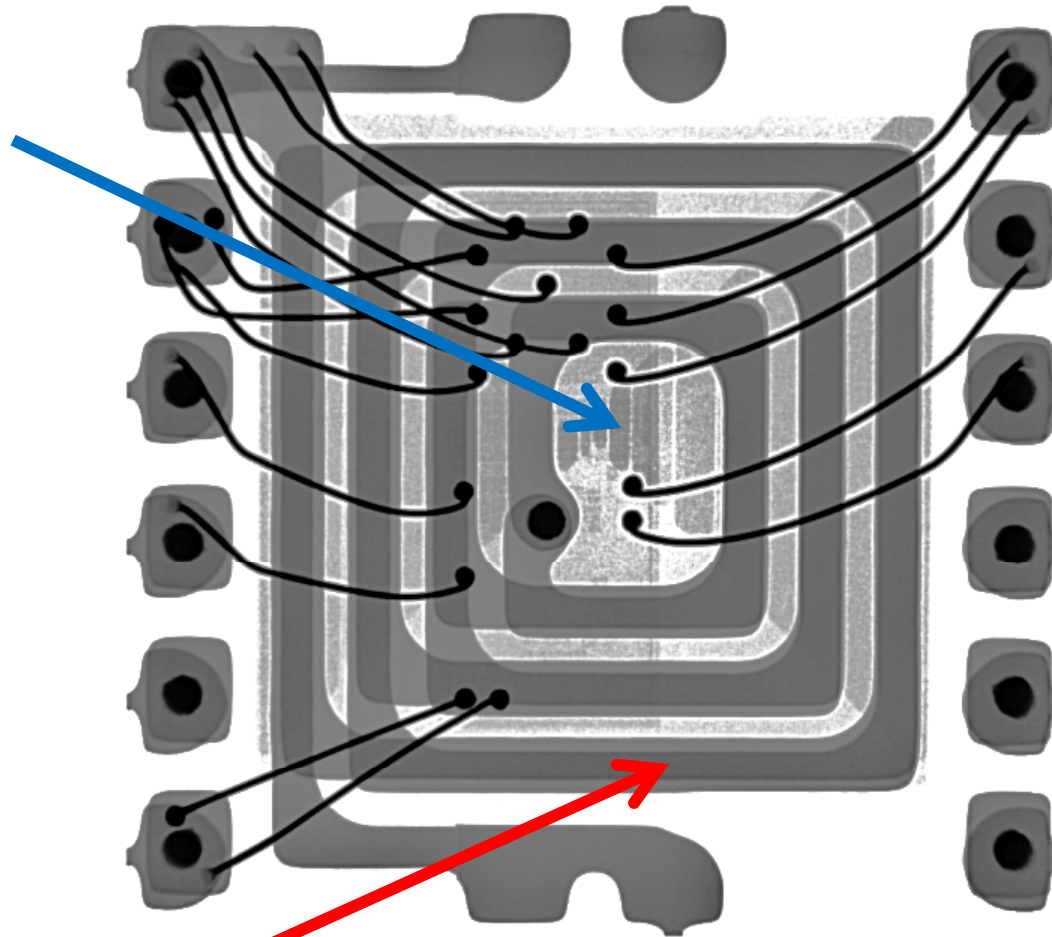
◆ Potential Effects

- Temperature Stress – Hard vs Easy Axis Orientation
- Physical Stress - Magnetostriction

Construction

(X-Ray Image of Stacked Device)

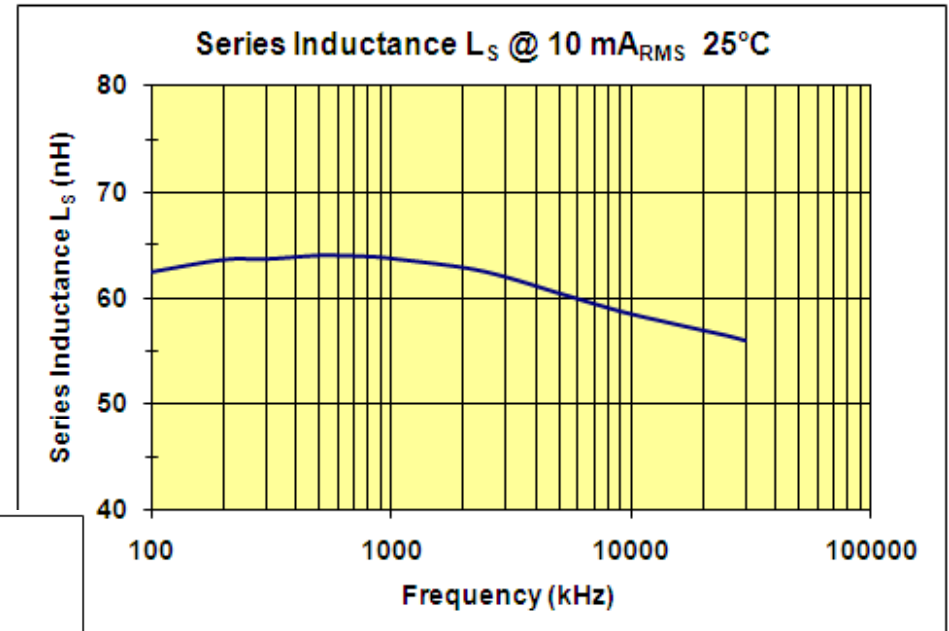
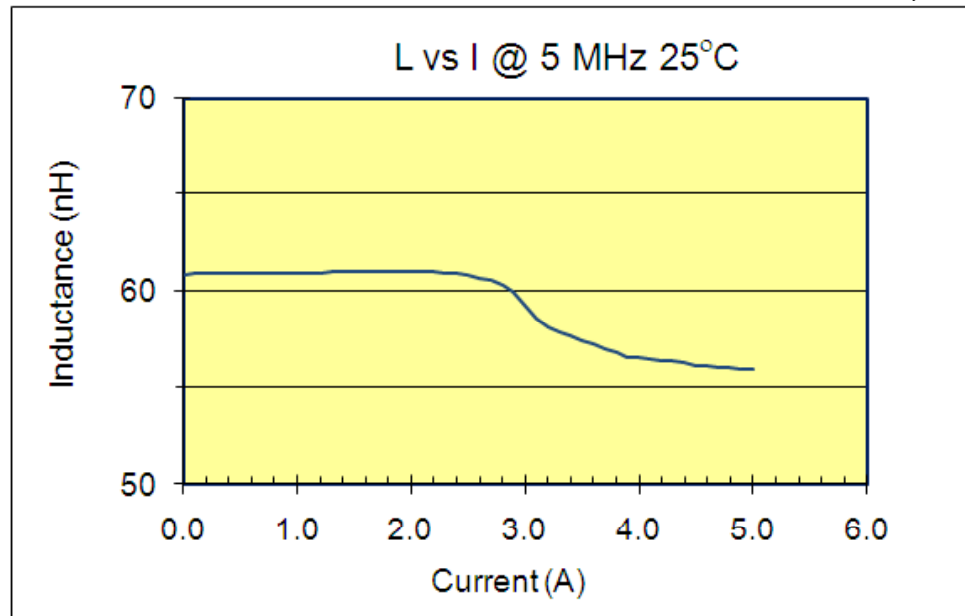
Inductor Die
Magnetic Material



Inductor Windings

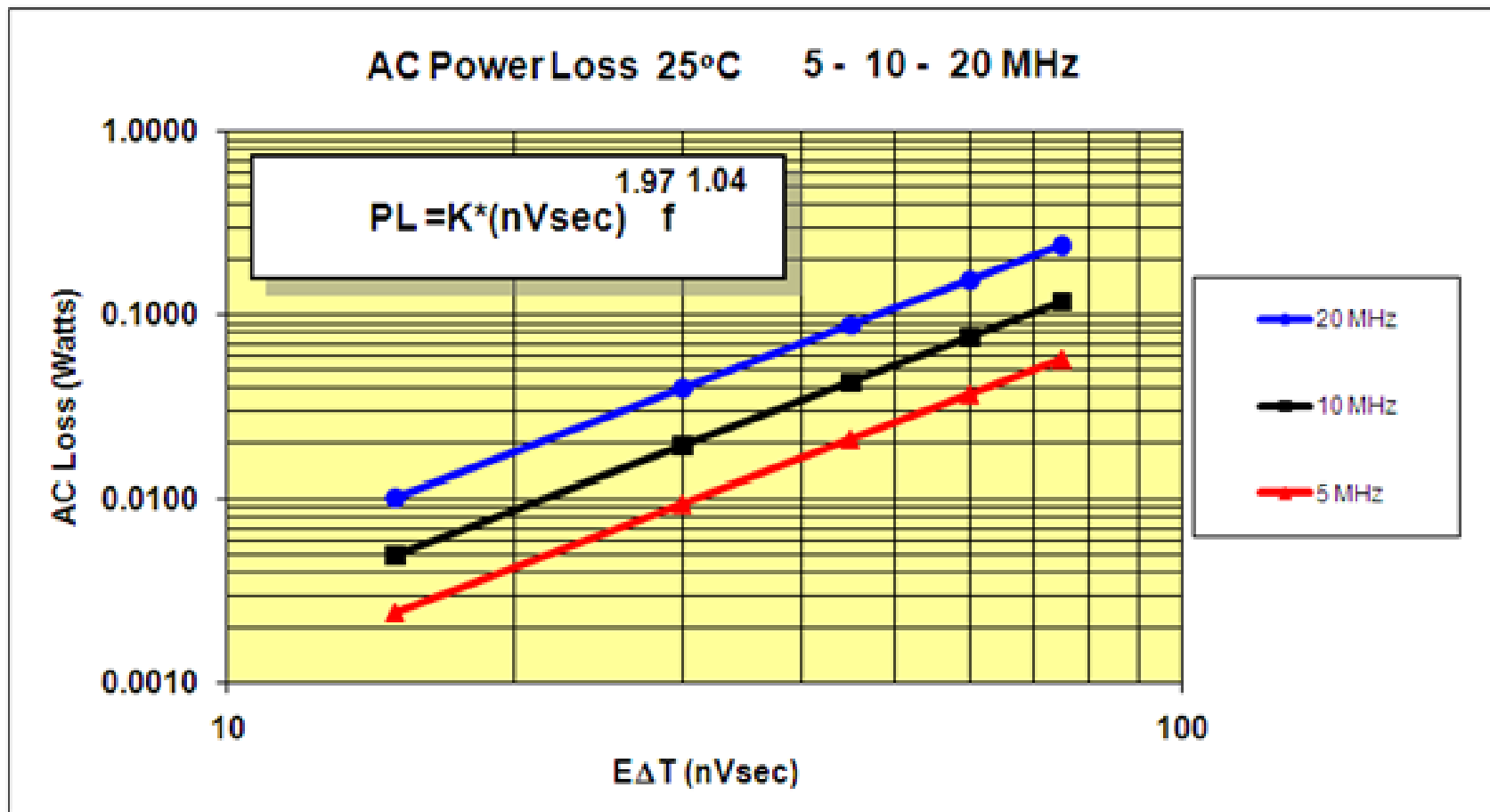
Inductor Level Performance

(Small Signal Characteristics)



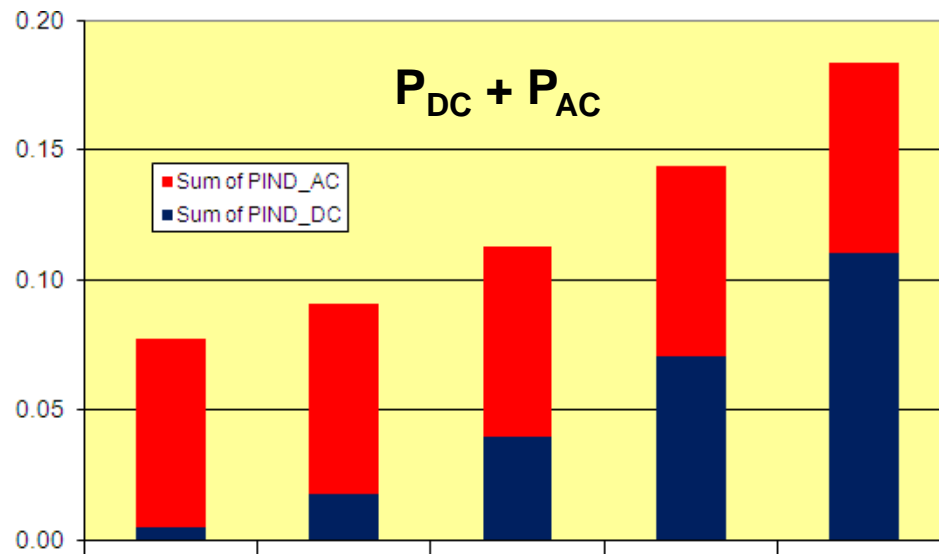
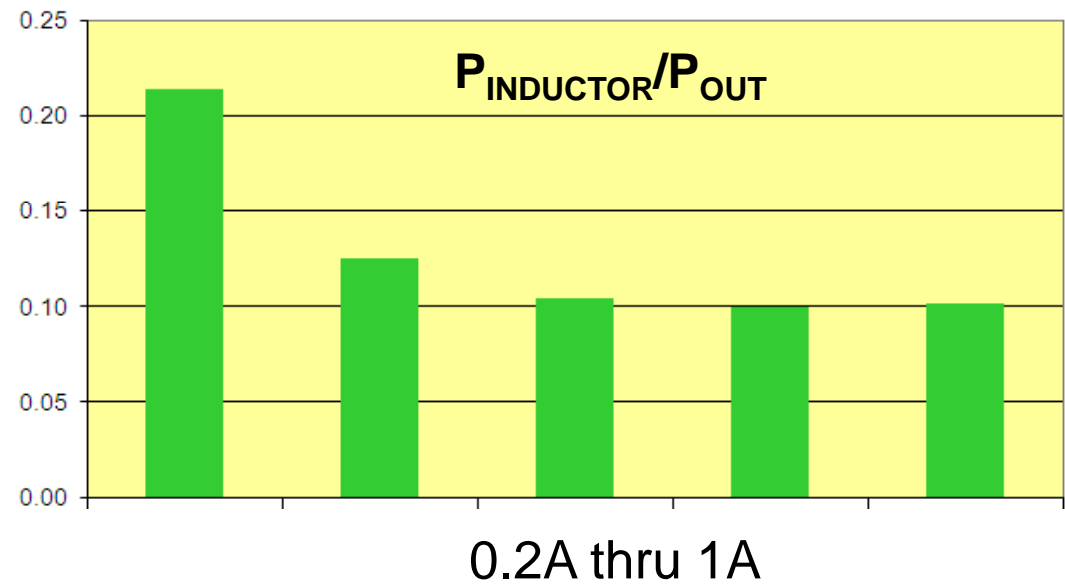
Inductor Level Performance

(Large Signal Characteristics)



Inductor Level Performance

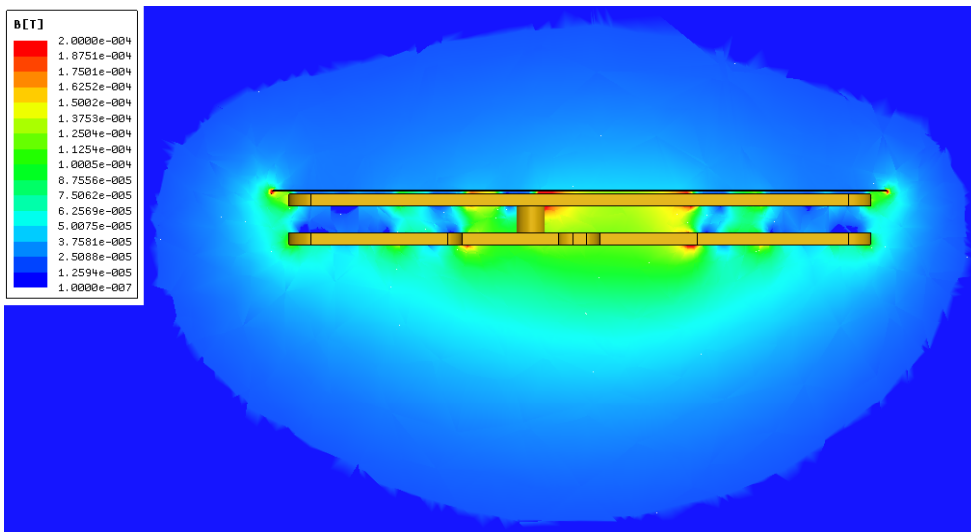
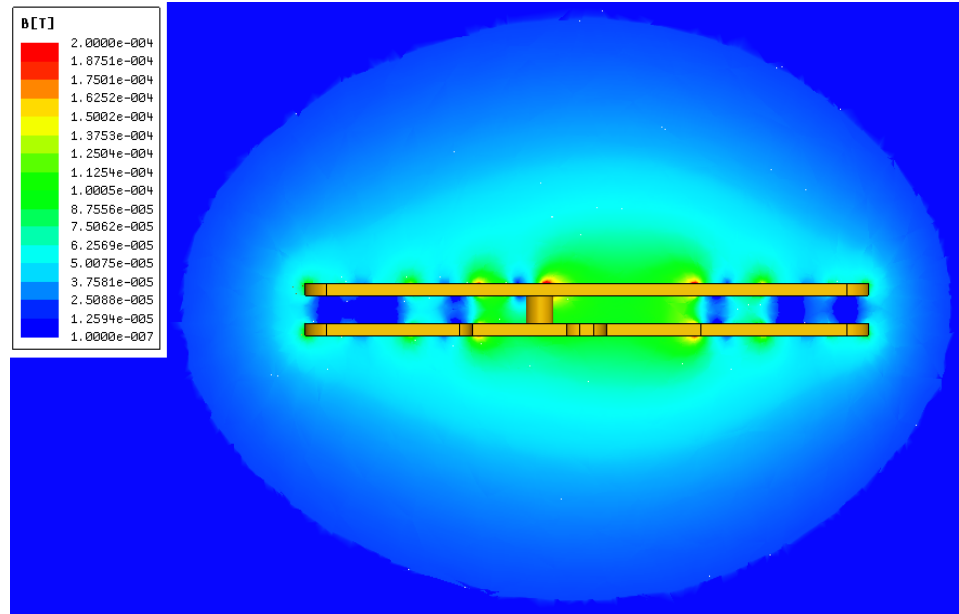
(Inductor Power Losses $V_{IN} = 3.3V_{DC}$ $V_{OUT} = 1.8V_{DC}$ $F_{SWITCH} = 20\text{ MHz}$)



Inductor Level Performance

(External Magnetic Fields: Same Scale)

Planar Coil Without
Magnetic Plate

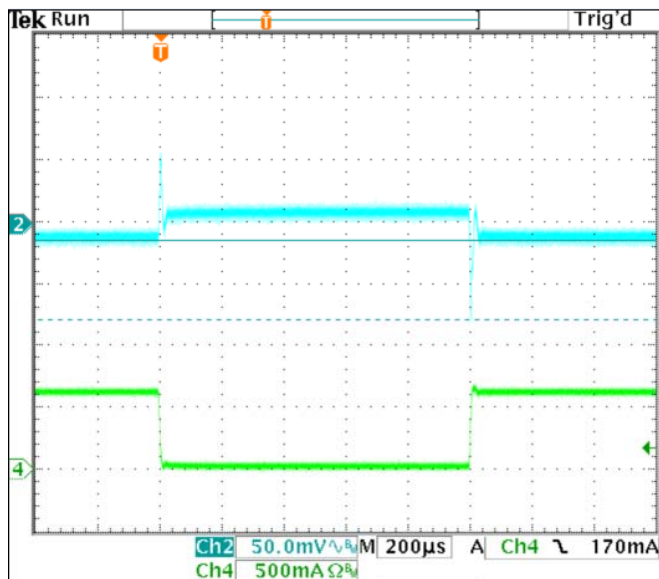
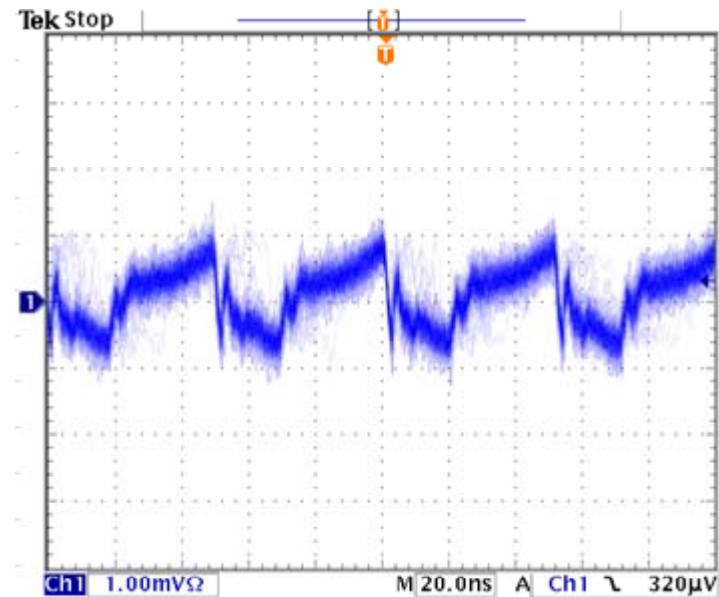


Planar Coil With
Magnetic Plate

Device Level Performance

(Output Ripple /Transient Response $V_{IN} = 3.3 V_{DC}$ $V_{OUT} = 1.8 V_{DC}$ $I_{LOAD} 0.6 A_{DC}$)

Output Ripple
2 mVp-p



Transient Response
65 mV deviation

Migration to Monolithic Device

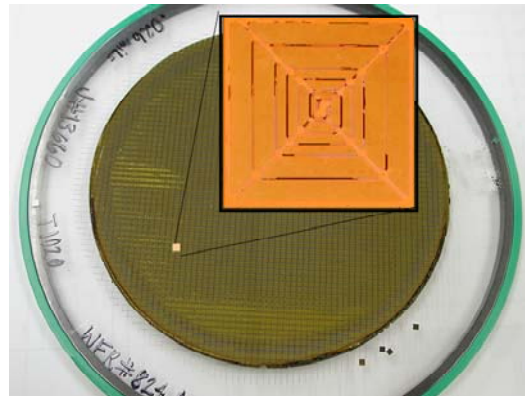
(CMOS Compatible Inductor Fabrication)

**Historical:
Concept
designs**



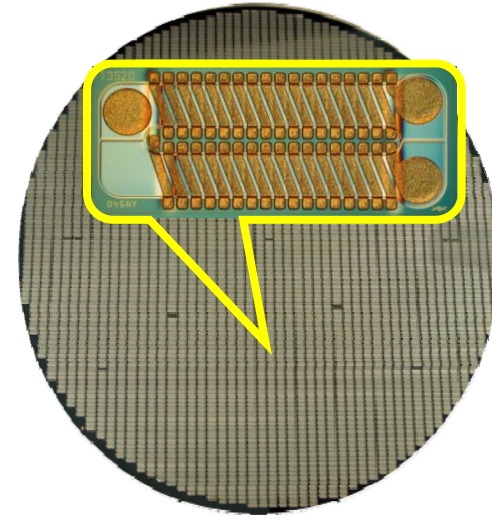
**Toroid
inductor**

**Today:
Ready for
Manufacturing**



**Magnetic Material
on Silicon**

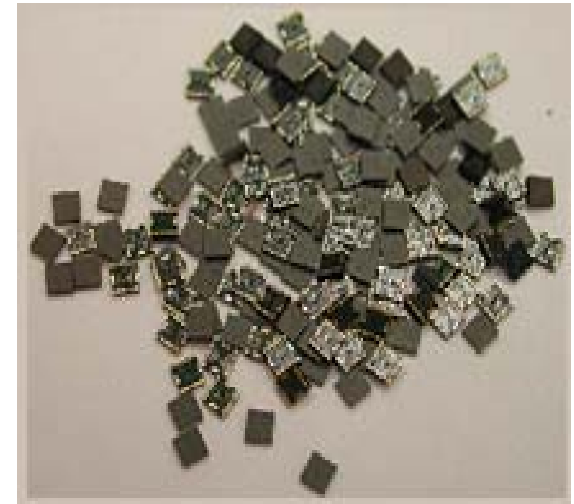
**Today's Prototypes
Tomorrow's Products**



**Conductors,
Insulators & Magnetic
Material on Silicon**

Summary and Next Steps

- ◆ Wafer level magnetics are being iterated thru the complete manufacturing process
- ◆ Finished devices pass qualification and reliability testing
- ◆ Achieved targeted inductor and device performance
- ◆ Low cost design construction techniques utilized
- ◆ Wafer level magnetic materials commercialization is underway



Wrap Up

Thank You For Your Attention

END