Adaptive Voltage Scaling (AVS)

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Agenda

- AVS Introduction, Technology and Architecture
- Design Implementation
- Hardware Performance Monitors Overview
- AVS Design & Test Flow
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Traditional Power Management Delivery

Digital Processor/ASIC \(\rightarrow\) Voltage Regulator

Fixed Voltage = Inefficient System!!!
- No temperature compensation
- No adjustment for lower voltages at lower frequencies
- No compensating for process variation
Adaptive Voltage Scaling = Maximum power savings
- Process and Temperature Compensation
- No need for frequency-voltage lookup tables
- Real-time continuous closed-up

\[ E = (\alpha \cdot C \cdot f_{CLK} \cdot V^2 + V \cdot I_{LEAK}) \cdot t_{TASK} \]

DYNAMIC LEAKAGE

PWI = PowerWise Interface

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Operating Vdd Range – Device Performance Distribution

Published (Fixed) V\textsubscript{DD}

- All silicon guaranteed to function
- Timing models for PTV corners at F

All units will work over full PTV range

Process Variation

Slow Typical Fast
Published (Fixed) $V_{DD}$

- All silicon guaranteed to function
- Timing models for PTV corners at F

Most units expected to work over extended $V$ range
Optimizing Power Efficiency

Published (Fixed) $V_{DD}$
- All silicon guaranteed to function
- Timing models for PTV corners at $F$

Process Variation
- Slow
- Typical
- Fast

Fast units expected to work over greatly extended $V$ range
AVS Optimizing Power / Full Range

Published (Fixed) $V_{DD}$
- All silicon guaranteed to function
- Timing models for PTV corners at F

AVS $V_{dd}$ for Lowest Power
- Power controller maintains $V_{dd}$ to lowest level possible based on on-chip PTV performance measurement
- Slow silicon possible lower $V_{dd}$ based on slack timing

Clamp Minimum $V_{DD}$
- Independent clamp level for minimum $V_{dd}$ set with power controller
- Overrides monitor request to go to a lower $V_{dd}$

- All silicon guaranteed to function
- Timing models for PTV corners at F

Slow silicon possible lower $V_{dd}$ based on slack timing

Independent clamp level for minimum $V_{dd}$ set with power controller

Overrides monitor request to go to a lower $V_{dd}$
### Process Variability Comparison

#### NMOS

<table>
<thead>
<tr>
<th>$I_{D_{ss}}$ [uA/μm]</th>
<th>$V_{dd} -10%$</th>
<th>$125^\circ C$</th>
<th>$25^\circ C$</th>
<th>$-45^\circ C$</th>
<th>$V_{dd} + 10%$</th>
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<tbody>
<tr>
<td>Corner</td>
<td>S:S</td>
<td>S:S</td>
<td>S:S</td>
<td>T:T</td>
<td>F:F</td>
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<tr>
<td>0.13μm</td>
<td>-39.60%</td>
<td>-24.91%</td>
<td>-14.46%</td>
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<td>14.19%</td>
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<tr>
<td>90nm G</td>
<td>-42.73%</td>
<td>-28.55%</td>
<td>-20.04%</td>
<td>0.00%</td>
<td>24.06%</td>
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<td>-26.95%</td>
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<td>23.32%</td>
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<td>40nm G</td>
<td>-45.43%</td>
<td>-28.29%</td>
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<tr>
<td>40nm LP</td>
<td>-47.87%</td>
<td>-29.36%</td>
<td>-25.30%</td>
<td>0.00%</td>
<td>28.69%</td>
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#### PMOS

<table>
<thead>
<tr>
<th>$I_{D_{ss}}$ [uA/μm]</th>
<th>$V_{dd} -10%$</th>
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<td>21.31%</td>
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AVS Results on 130nm

- ARM926EJ-S core
- Voltage and frequency scaling of CPU, Caches
- Four performance points:
  - 60, 120, 180, 240 MHz
  - 0.7V – 1.2V Adaptive Voltage Range

- Dual ARM7 CPU cores
- Voltage and frequency scaling of ARM7
- Performance points:
  - 96, 84, 72, 60, 12 MHz
  - 0.7V – 1.2V Adaptive Voltage Range
Measured AVS Power Savings

- Custom ASIC/SoC design
  - process 65nm, freq. greater than 750Mhz
- AVS reduced core power by 27 to 40% at maximum frequency

TA=25C
Power Saving and Thermal Performance, 65nm process

MTBF doubles with reduction of 10°C
TN2020 & NSC power solution
# Measurements – TN20xx

<table>
<thead>
<tr>
<th>Temp</th>
<th>AVS OFF</th>
<th></th>
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<th>AVS ON</th>
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<th>Power Savings</th>
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<td></td>
<td>deg C</td>
<td>mV</td>
<td>mV (c. sns.)</td>
<td>A</td>
<td>Power W</td>
<td>mV</td>
<td>mV (c. sns.)</td>
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AVS System Impact

• System Performance
  – Once enabled AVS runs in background
  – No processing overhead

• Energy Savings – Scaled Voltage Domain
  – Savings vary depending on process geometry, design implementation, and frequency scaling profile
  – Expected energy savings for typical silicon will be 20-50% based on process and temperature variations

• System Risk Mitigation
  – AVS is an additional function in the ASIC/Processor and the power conversion device
  – AVS compliant ASIC/Processor and power conversion devices can still operate at fixed voltage or DVS without any design changes
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HPM Overview

- HPM is Embedded in the voltage domain that is AVS controlled
- HPM translates the voltage level into silicon performance information
- HPM generated silicon performance information is a function of voltage level and HPM clock
- APC makes use of silicon performance information to determine the optimum voltage level for the required target performance
- Structurally coded synthesizable RTL to facilitate ease of layout P&R for optimizing silicon performance tracking accuracy
Critical path timing is correlated to HPM performance monitoring by setting the Reference Performance Code (RCC).

HPM

Performance Code

Passing Performance

Failure Point

RCC (selectable)

Control Margin
HPM Performance Code and APC Voltage Control

- **Reference Calibration Code**
  - Pre-delay
  - Main-delay

- **HPM delay line propagation**
  - PC > RCC
  - performance > requirement
  - adjust voltage level lower

- **RCC settings reside in APC**
- **PC is compared to RCC in APC**
- **Voltage adjustment initiated by APC**

- **PC < RCC**
  - performance < requirement
  - adjust voltage level higher
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APC2 IP SoC View

- Up to 4 AVS domains
- 1 - 4 per scalable clocks per AVS domain
- 1- 4 HPM per clock domain
- APC2
  - PWI2.0 interface master
  - Up to 4 AVS domains
  - Enhanced control-system
  - Adaptive Voltage Scaling closed-loop control based on performance measurement data sampled by HPM
  - Open-loop voltage scaling via voltage register table
  - 8 performance levels + retention level
  - Control registers programmed via AMBA-APB interface
  - Auto PL0 back-bias
  - Trace port for debug
AVS Design Flow

Power-aware ASIC Design Flow

Architecture Specification
- Functional specification
- Power management strategy
- Power domain partitioning
- IP selection

RTL Design
- RTL implementation
- Power domains

Functional Simulation
- Functional verification
- Power domains

Logic Synthesis and DFT
- Gate implementation
- Timing/power/area optimization
- SCAN chains
- Power domains

Physical Design
- Power domains
- Power gating
- Level shifters and isolation cells
- Timing/power/area optimization

Sign-off Verification
- Equivalency
- Timing
- Power

Adding the AVS

- No. of independent AVS power domains
- Frequency scaling → no. of performance levels
- No. of clock domains in each AVS power domain
- No. of HPM for performance tracking
- PowerWise Interface pins
- IP selection → low voltage std cells and memories

- Clock management with performance level interface
- Integrate APC and HPMs
- Synchronizers at power domain boundary

- APC/HPM connectivity
- APC programming
- AVS modeling

- HPM synthesis
- HPM SCAN chain stitching

- HPM layout
- HPM placement in ASIC

- AVS timing verification
- HPM timing verification

November 2009

PowerWise

National Semiconductor
AVS Production Flow

Typical ASIC Production Flow

- DC/AC Characterization
  - One time effort
  - Over process and temperature corners

- SCAN and Functional Test
  - Manufacturing test

AVS ASIC Production Flow

- DC/AC + AVS Characterization

- SCAN and Functional Test

- Low voltage SCAN and Functional Test

- HPM and Emulated AVS Test
  - Determine AVS minimum VDD
  - Correlate ASIC performance/voltage requirements to HPM

- Include APC and HPM in the testing

- Repeat regular testing at low voltage and low speed
  - Check HPM performance code

and / or

- Check HPM performance code vs. voltage scaling trend
  - Identify AVS voltage level and test functional at speed