Low Parasitic Packaging of Power Modules for High Frequency Operation

Paul McCloskey[a], Ray Foley[b], Virginia Morris[a], Nicolás Cordero[a], Alan Mathewson[a], Cian Ó Mathúna[a]

[a]Tyndall National Institute,Lee Maltings, Prospect Row, Cork.
[b]Department of Electrical Engineering, University College Cork, College Road, Cork..

Motivation

Next generation power supplies must be

- Smaller
- More efficient
- Cheaper
- Manufacturable as “system in a package”

SMPS switching at higher frequencies

- Reduces size of passive components required
- Helps miniaturisation
- Parasitic inductance has much greater impact on performance
- **Hence packaging needs to be better**

Integrated Power Trains - State of the Art

	NXP	*Renesas*	*Fairchild*	*ON Semi*
Model	PIP212-12M	R2J20601NP	FDMF8704V	NIS3001A
Vout	0.8V to 6V	1.0V to 5V	0.8 to 3.2V	0.7V to 5.1V
Vin	3.3V to 16V	Up to 16V	7 to 20V	7V to 14V
Iout max	35A	35A	32A	31A
Operating Frequency	Up to 1MHz	>1MHz possible	Up to 1MHz	Up to 1MHz
Package size (Power Train)	8mm x 8mm x 0.85mm	8.1mm x 8.1mm x 0.8mm	8mm x 8mm x 0.8mm	10.5 mm x 10.5mm x 2.0mm
Included	2 Mosfetts,1 Schottky, 1 driver	2 Mosfetts,1 Schottky, 1 driver	2 Mosfetts,1 Schottky, 1 driver	2 Mosfetts,1 Schottky, 1 driver
Required	L, C, Controller	L, C, Controller	L, C, Controller	L, C, Controller

Renesas SiP

NXP PIP212-12M

CASE 500 PinPAK
On Semi

Wafer Level Module Packaging

Cu interconnect
Thick photo-resist
Embedded die

Fabrication Steps

- Deposit release layer
- Create pads and bottom side interconnect
- Mount die required for module
- Embed die in thick photoresist
- Fabricate top side interconnect
- Fabricate top cover
- Release from temporary substrate

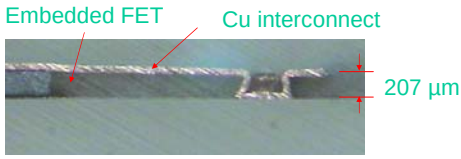
Advantages

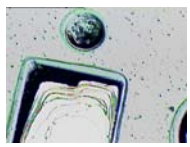
- Batch processing
- Thick plated copper interconnect
- Good feature size capability
- Repeatable release process

Novel thick photoresist developed

- Uses modified commercial materials
- Patterning of thick layers achievable
- Reduced shrinkage
- Repeatable release process

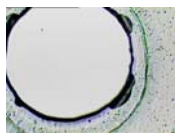
Vertical Vias			Horizontal Interconnect	
Max Via Length	Min Via Ø	Min Via Spacing	Min Width	Min Spacing
500 µm	200 µm	200 µm	50 µm	50 µm





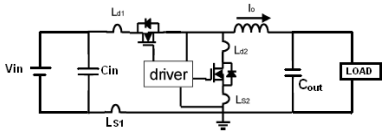
Closed 300 micron via and partly closed large structure

Process optimisation



Close up of 300 micron via

Electrical Modelling



Buck Converter with parasitic inductance; L_{d1}, L_{d2}, L_{s1}, L_{s2}

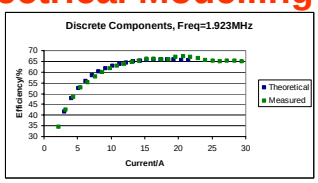
Analytic Model developed to predict converter efficiency
Calculates losses at each part of the converter waveform

Inputs

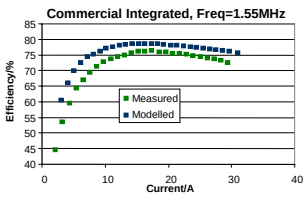
- FET performance parameters
- R_{ds} ➔ MOS Conduction loss
- Q_{rr}, C_{oss} ➔ Reverse recovery & ringing turn-on loss
- C_{gd}, C_{ds} ➔ Ringing turn-off loss
- V_f, $t_{deadtime}$ ➔ Body diode Conduction losses
- $Q_{g\text{-}q}$, $V_{drv\text{-}q}$ ➔ Gate drive losses

Packaging

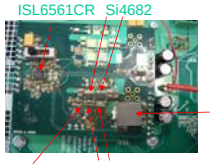
- Parasitic L ➔ P_{on} and P_{off} loss

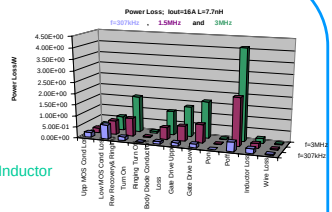


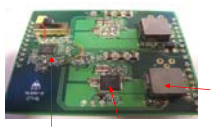
Discrete Components
Parasitic L = 7.7 nH

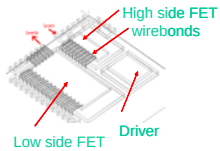


Commercial Power Train
Loop inductance = 1.4 nH

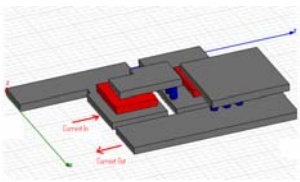








Optimised Design



Build Up Power Train
(Optimised layout)
Loop Inductance = **0.6 nH**
2% HF efficiency improvement vs. commercial
50% reduction in size