

Voltage Scalable Switched Capacitor DC-DC Converters for Ultra-Low-Power On-Chip Applications

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Ultra-Low-Voltage Operation?

Motivation

Weak Inversion:
Slower, power savings

Strong Inversion:
Fast, power-hungry

Sub-threshold:
Intermittent computation, minimum energy

Applications

Environmental Sensors

Medical Devices

Ambient Intelligence

Minimum Energy Operation

90nm CMOS 32-bit adder

- Operate at lowest voltage to just meet performance constraints
- If performance is not a constraint, operate at the minimum energy point

$$E_{\text{total}} = C_{\text{eff}} V_{\text{DD}}^2 + W_{\text{eff}} L_{\text{eff}} K_C V_{\text{DD}}^2 \sigma_{\text{eff}}^2$$

Switched Capacitor DC-DC Converters

Efficiency Loss Mechanisms

Sub- V_T MSP430 Microcontroller

Conduction Loss

Energy from battery = $Q \cdot V_{\text{BAT}}$
Energy to load = $Q \cdot V_L$
 $\eta_{\text{con}} = \frac{V_L}{V_{\text{BAT}}}$

Energy from battery = $Q \cdot V_{\text{BAT}}$
Energy to load = $2Q \cdot V_L$
 $\eta_{\text{con}} = \frac{V_L}{V_{\text{BAT}}/2} = \frac{2V_L}{V_{\text{BAT}}}$

Multiple Gain Settings

Bottom-Plate Parasitic Loss

$E_B = 24C_B V_{\text{BAT}} \Delta V$
 $E_{BP} = 12\alpha C_B \frac{V_{\text{BAT}}^2}{4}$
 $K_p \frac{V_{\text{BAT}}}{\Delta V} = \frac{E_{BP}}{E_B} = 0.125\alpha \frac{V_{\text{BAT}}}{\Delta V}$

Switching and Control Loss

$E_{\text{SW}} = nC_{\text{ov}} W L V_{\text{BAT}}^2$
 $E_{\text{SW}} = n\beta C_f V_{\text{BAT}}^2 W \sim C, f_s$
 $K_s f_s \frac{V_{\text{BAT}}}{\Delta V} = \frac{E_{\text{SW}}}{E_B} = n\beta f_s \frac{V_{\text{BAT}}}{\Delta V}$

Topology Dependent Technology Dependent

- Pre-factor is due to linear efficiency loss
- Contribution of other losses decrease as ΔV goes up
- There is an optimum ΔV for any given topology
- Larger C improves efficiency

$$\eta_{\text{av}} = \frac{E_L}{E_B + E_{BP} + E_{\text{SW}} + E_{\text{CONT}}} = \left(1 - \frac{\Delta V}{V_{\text{BAT}}}\right) \frac{1}{1 + K_p \frac{V_{\text{BAT}}}{\Delta V} + K_s f_s \frac{V_{\text{BAT}}}{\Delta V} + K_c \frac{V_{\text{BAT}}}{\text{CAV}} + \frac{I_{\text{leak}}}{\text{CAV} f_s}}$$

Core logic (2 power domains) DC-DC converter

128Kb SRAM array

1.8mm x 2.29mm

Process	65nm CMOS
Area	
DC-DC Converter	0.12mm ²
SRAM	1.36mm ²
Logic	0.14mm ²
Performance	
Minimum Energy Point	$V_{\text{DD}} = 500\text{mV}$
Minimum Functional V_{DD}	$V_{\text{DD}} = 300\text{mV}$

$V_L = 0.5\text{V}$

- 65nm SoC functional down to 300mV
- Embedded DC-DC converter
- Extremely small area
- Scalable output voltage

0.18µm 1mA SCDCC Converter

Architecture

NON-OV CLK GENERATOR
AUTOMATIC FREQUENCY SCALER
SWITCH MATRIX

Gain Settings

Automatic Frequency Scaler

Overload comparator is used to increase switching frequency at higher loads

At low load, switching frequency is halved using a counter mechanism

enW2 and enW4 determine switching frequency out of divided versions of clk4X

Die Photo

0.57 mm²

Transient Response

Efficiency

Conclusions

- On-chip Switched Capacitor DC-DC converters can provide up to 10 - 20mA load current
- Multiple Voltage Domains possible
- Achieves above 80% efficiency
- Technology Scaling helps to reduce area and switching losses