Synchronization Scheme for a High Frequency Hysteretic Controlled DC-DC Buck converter

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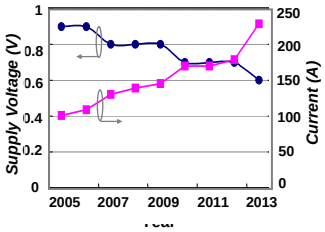
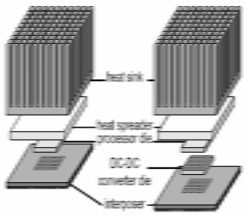
High-Frequency Near-Load DC-DC converters

In order to cope with the fast current demands and stringent voltage tolerance requirements in performance products, near-load power delivery solutions based on high-frequency low voltage dc-dc converters have been proposed. Integrating the voltage regulator module near or within the processing die for localized power delivery has several advantages.

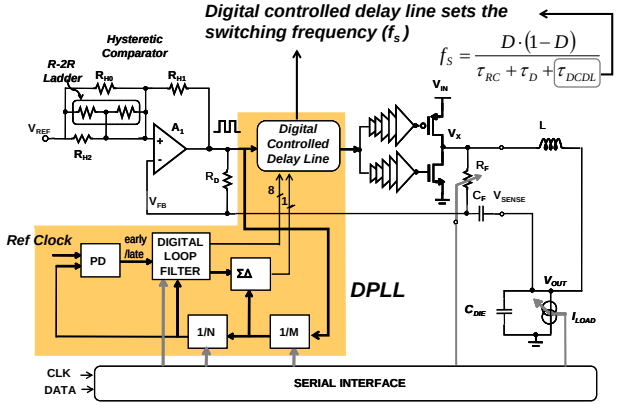
- High voltage conversion ratios near the load trades voltage for current efficiency to reduce external peak currents and relax stringent impedance requirements of packages and board level traces.
- High frequency converters lead to a reduction in capacitor and inductor sizes by several orders of magnitude.
- Faster load response to cope with fast localized transients.
- Localized and efficient power delivery systems naturally lend themselves to multiple voltage domains for multi-core processing architectures.



Processor's voltage and current
(Source: ITRS Roadmap, 2006)

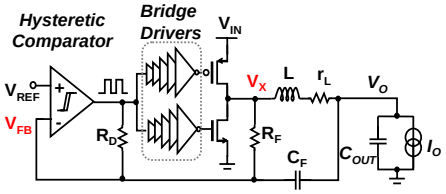


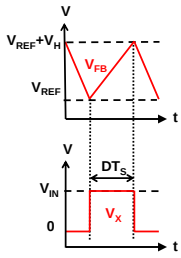
Digital PLL Synchronized Converter



Hysteretic Controlled Buck Converter

Hysteretic control techniques for dc-dc switched buck converters based on a simple feedback loop achieves a near immediate load response without stability issues.



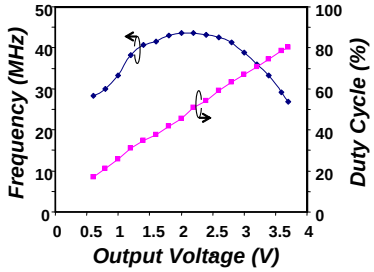


The switching frequency of the hysteretic controlled buck converter exhibits a strong dependence on voltage conversion ratio:

$$f_S = \frac{D\cdot(1-D)}{\tau_{RC}+\tau_D}$$

If kept unchecked, the free-running oscillations may fall in undesired power supply resonance bands created by parasitic package inductance interconnects and on-die decoupling capacitances.

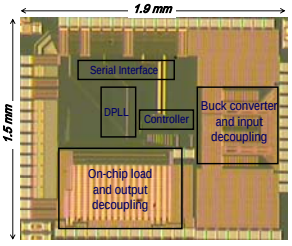
[P. Li, R. Bashirullah, P. Hazucha, T. Karnik, VLSI Circuits Symp. 2007]

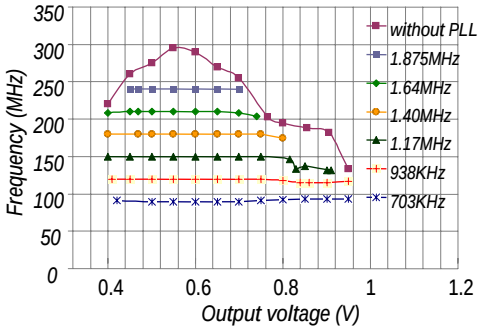


This can potentially generate large voltage excursions in the supply network due to high impedance peaks formed by the multi-resonant networks, compromising overall system operation and device reliability. Therefore, ideally it is desirable to synchronize the converter to an on-chip clock generated from within the processor to mitigate noise injection in undesirable frequency bands.

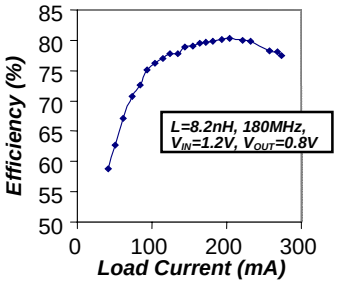
Frequency Locked Converter

130nm 1P-8M Digital CMOS

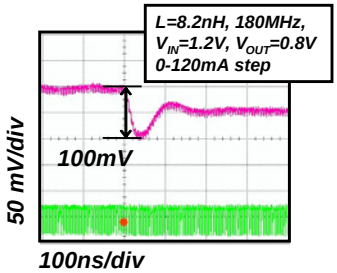




Efficiency



Load Response



Performance Summary

Technology	**130nm CMOS 8M1P**
Chip area	**2.85mm²**
DC-DC converter area	**0.42mm²**
Bridge area, A_{BRDG}	**0.03mm²**
Decoupling Capacitance	**20nF**
Inductance, L	**8.2nH**
Input voltage, V_{IN}	**1.2V**
Output voltage, V_{OUT}	**0.4V~0.96V**
Switching frequency, f	**90M~240M**
Maximum current, I_{MAX}	**0.28A**
Current density, I_{MAX}/ A_{BRDG}	**9.33A/mm²**
V_{IN}=1.2V, V_{OUT}=0.8V, f=180MHz	
Droop $V_{OUT,P-P}$ @ 0.12A load step	**100mV**
Efficiency (peak)	**80%**
Efficiency @ I_{MAX}	**77.5%**

Acknowledgment

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