



***Inductors In Silicon Based on SU-8  
Enhanced Silicon Molding Technique for  
Portable Electronics***

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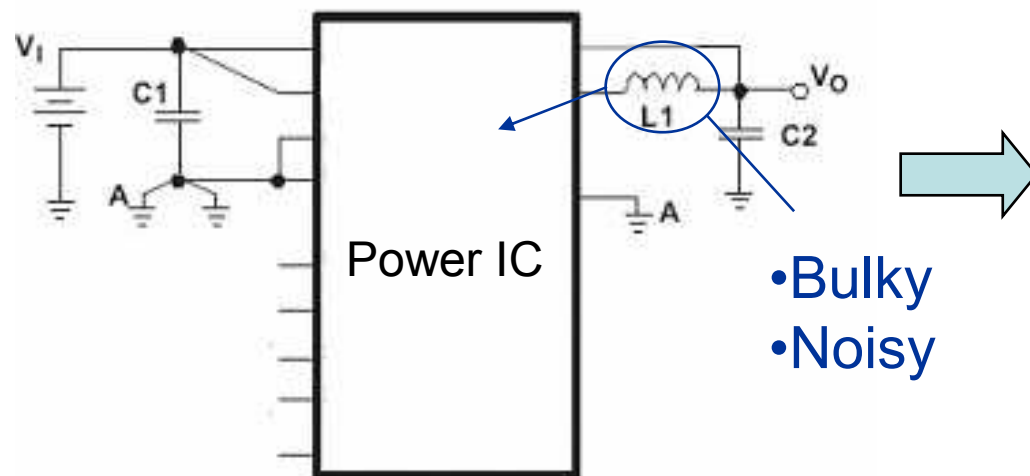
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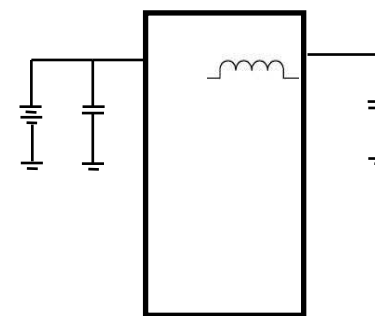
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- Introduction
- Concept of MEMS Inductors Based on Silicon Molding Technique
- Direct Silicon Molding Technique
- SU-8 Enhanced Silicon Molding Technique
- Testing and Results
- Summary

- Typical specifications of DC-DC converters in portable electronics
  - Input voltage: 2.5~5.5V,
  - Output Current: 0.5~2 A, output voltage: 1.2~1.8



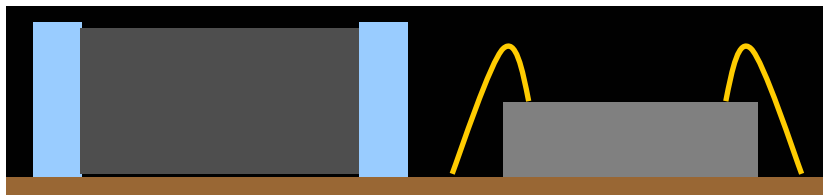
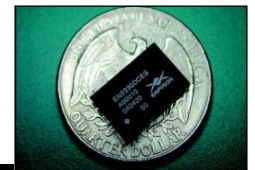
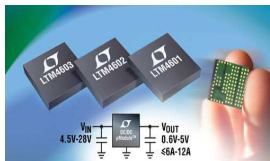
- Bulky
- Noisy



***Monolithic integration  
of miniaturized inductor  
and power ICs***

# Products with Embedded Inductors

	f (MHz)	L (uH)	Vin (V)	Vout (V)	Iout (A)	Footprint (mm <sup>3</sup> )
LTM4608	1.5	-	2.375~5.5	0.6~5	8	15×9×2.8
EN5396Q	5	0.09	2.375~5.5	0.75~5	9	10×12×1.8
EN5368QI	5	0.5	2.4~5.5	0.6~5	0.6	3×3×1.1
LM3218	2	2.6	2.7~5.5	0.8~3.6	0.65	3×2.5×1.2
MIC3385	8	0.47	2.7~5.5	0.6~5	0.6	3×3.5×0.9
FB6831J	2.5	-	2.7~5.5	0.8~4.8	0.5	2.9×2.4×1



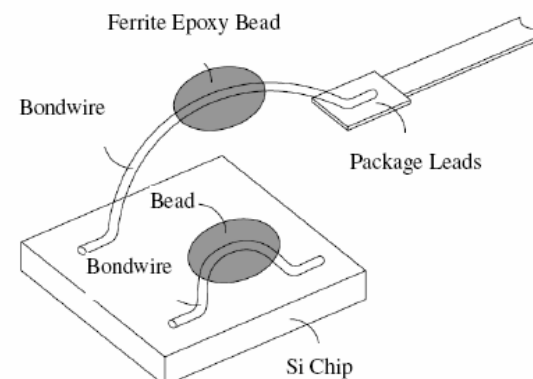
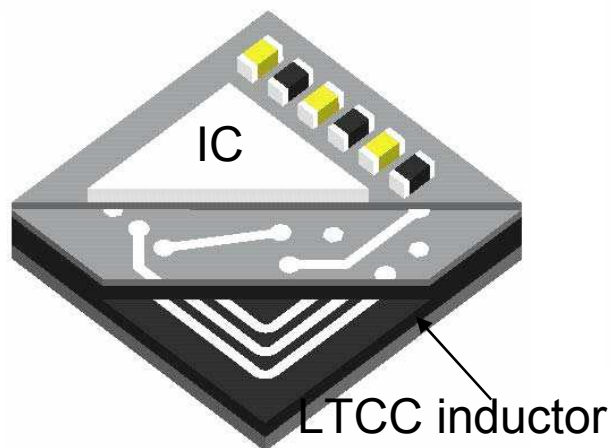
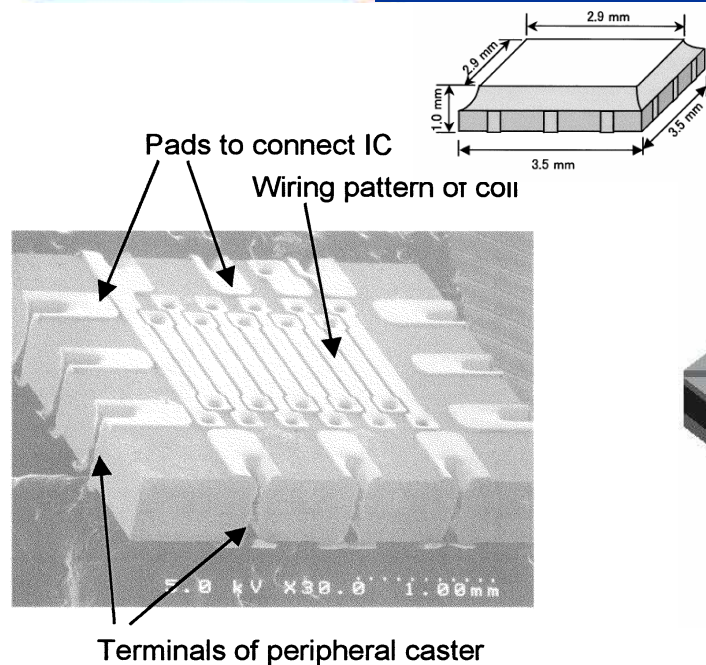
Mounted side by side on lead frame



Stacking together

Power IC  
SMT inductors

# Inductors by Packaging Technologies



- *Inductor on Magnetic substrate*
- Inductance: 1.65  $\mu\text{H}$
- DC resistance: 0.18  $\Omega$
- Output current: 500 mA
- Size: 3.5\*3.5\*0.6mm<sup>3</sup>

- *LTCC inductor as substrate*
- Inductance: 1.5  $\mu\text{H}$
- DC resistance: 0.46  $\Omega$
- Output current: 700 mA
- Size: 5\*5\*0.6mm<sup>3</sup>

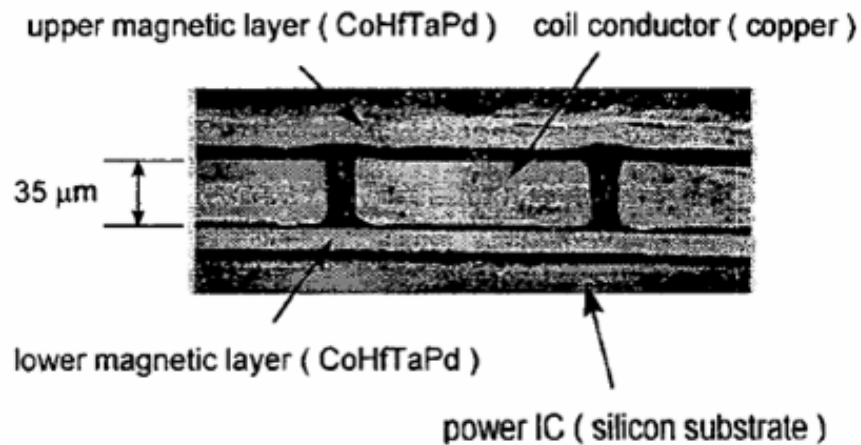
- *Magnetic coated bond wires*
- Inductance: 38 nH
- DC resistance: 7.1 m $\Omega$

**Hayashi, Fuji Cop.,2003**

**Mikura, Kyocera Inc.,2006**

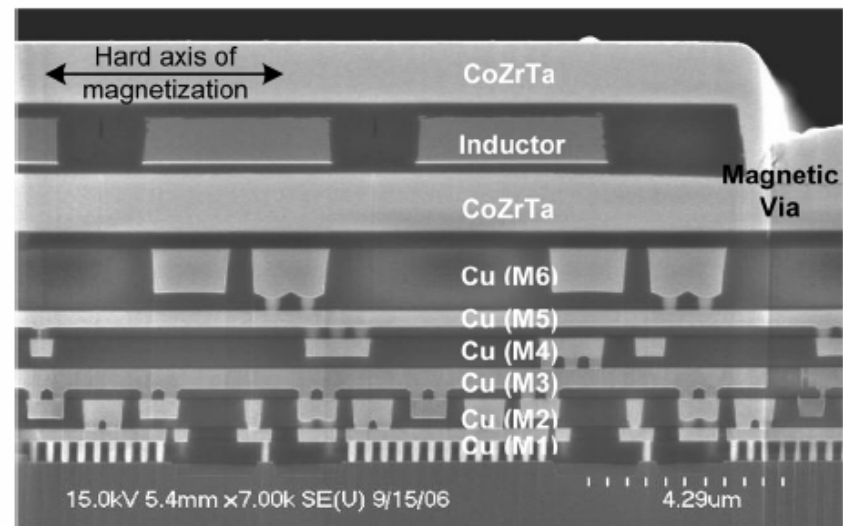
**Shen, UCF,2007**

# Inductors on Silicon



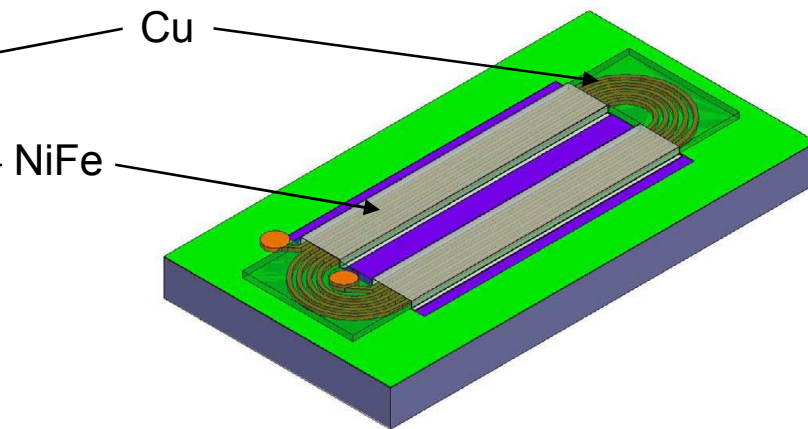
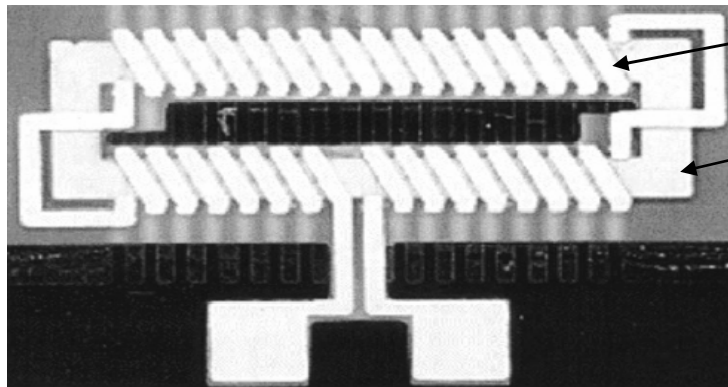
- 35 $\mu\text{m}$  Cu, 9 $\mu\text{m}$  CoHfTaPd (Magnetic)
- Inductance: 0.96  $\mu\text{H}$
- DC resistance: 0.9  $\Omega$
- Output current: 300 mA

***Katayama, Fuji, 2000***



- 1.5~2 $\mu\text{m}$  CoZrTa (Magnetic)
- Inductance: **9**  $\times$  air core spiral inductor
- Output current: < 400mA

***Gardner, Intel, 2007***



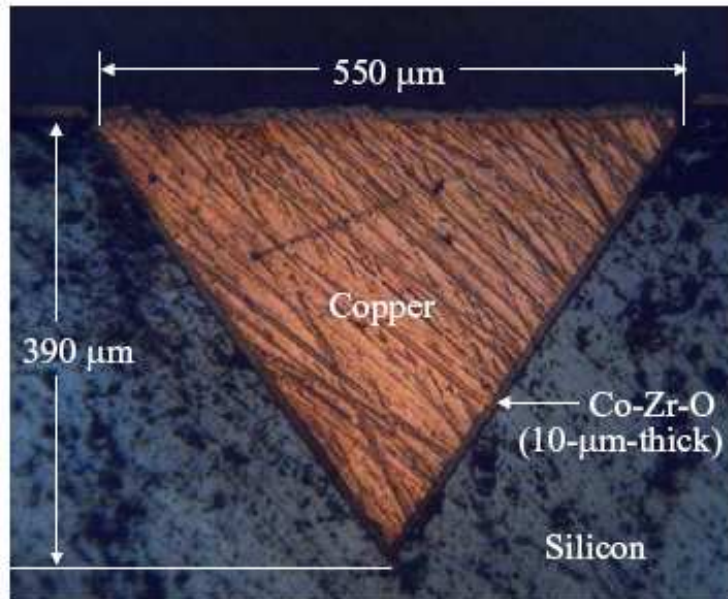
- 30 $\mu\text{m}$  Cu, 72 layers of 1 $\mu\text{m}$  NiFe
- Inductance: 2.3  $\mu\text{H}$
- DC resistance: 0.15  $\Omega$
- Area: 4 $\times$ 3 mm<sup>2</sup>
- Output current: 200 mA

***Park, GaTech, 2003***

- 50 $\mu\text{m}$  Cu, 10 $\mu\text{m}$  NiFe
- Inductance: 100 nH
- DC resistance: 0.13  $\Omega$
- Area: 6.4 mm<sup>2</sup>
- Output current: 500 mA

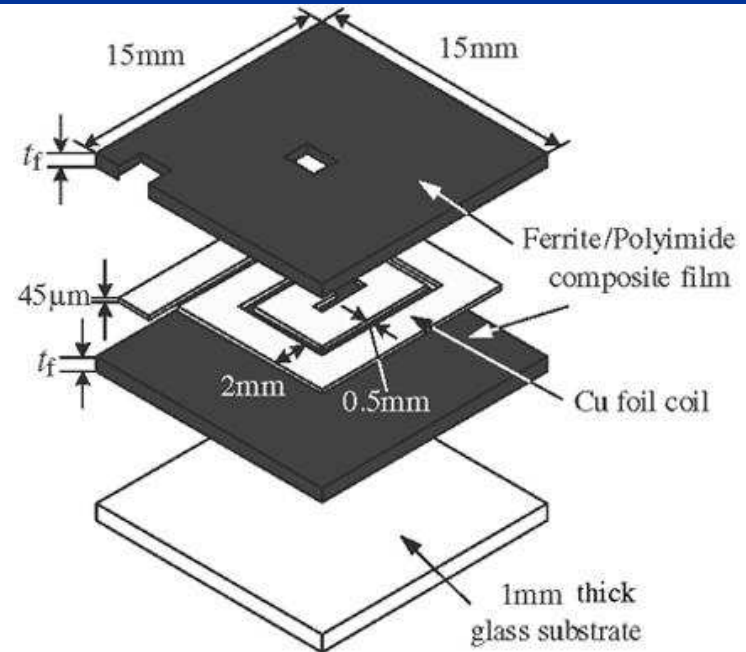
***Donnell, Tyndall, 2008***

## Inductors on Silicon



- Inductance: 11 nH
- DC resistance: 3 mΩ
- Size: 11mm straight line
- Output current: 5A

***Prabhakaran, Dartmouth, 2005***



- 45μm Cu, 200μm NiFe ferrite powder
- Inductance: 50 nH
- DC resistance: 15 mΩ
- Size: 15×15 mm<sup>2</sup>
- Output current: 10 A

***Kowase, Shinshu U., 2008***

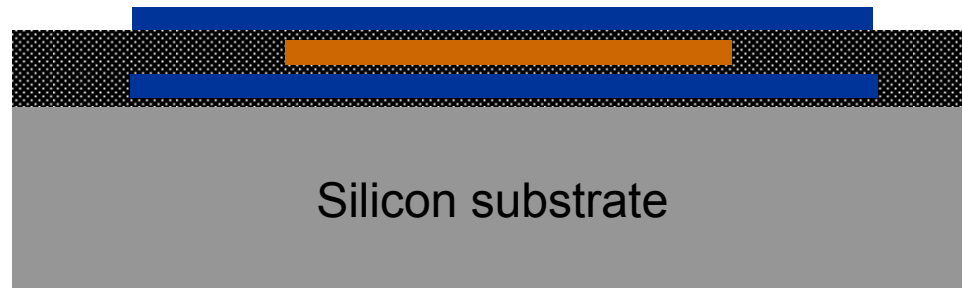


## *In Package VS On Silicon*

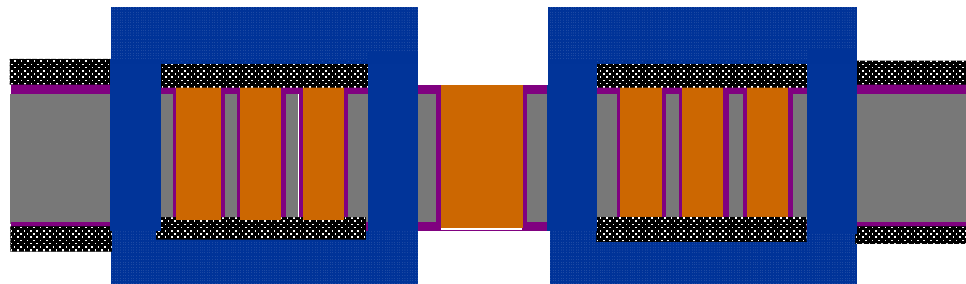
	Inductor in package	Inductor on silicon
Inductance	<b>High</b>	<b>Low</b>
DC resistance	<b>Low</b>	<b>High</b>
Saturation Current	<b>High</b>	<b>Low</b>
Magnetic material	<b>More options</b>	<b>Limited</b>
Size	<b>Large</b>	<b>Small</b>
Cost	<b>High</b>	<b>Low*</b>

- \*Two reasons:
1. wafer level process
  2. "in house" fabrication for semiconductor companies, not components from magnetic manufactures

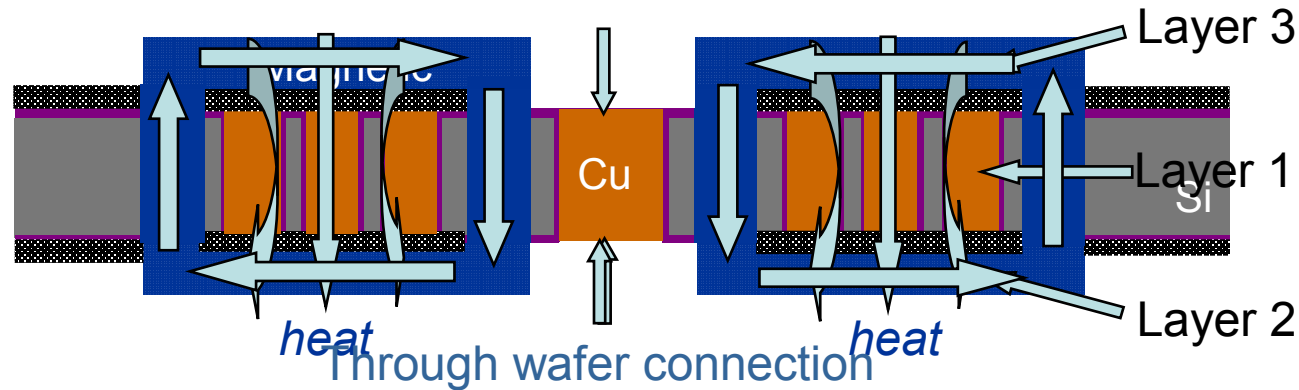
# On Silicon VS In Silicon



**State of Art Technologies:** *Stacked **On** the top of silicon substrate*



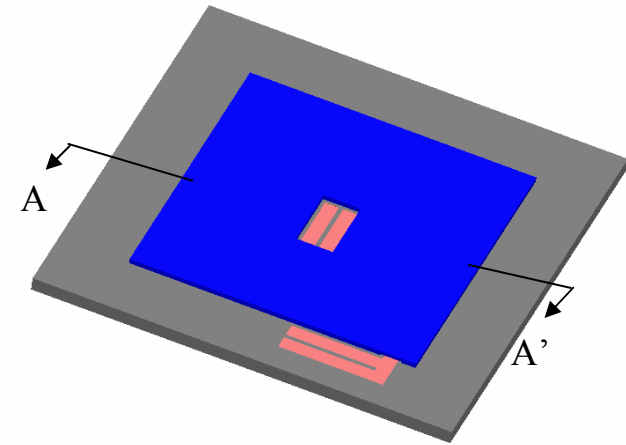
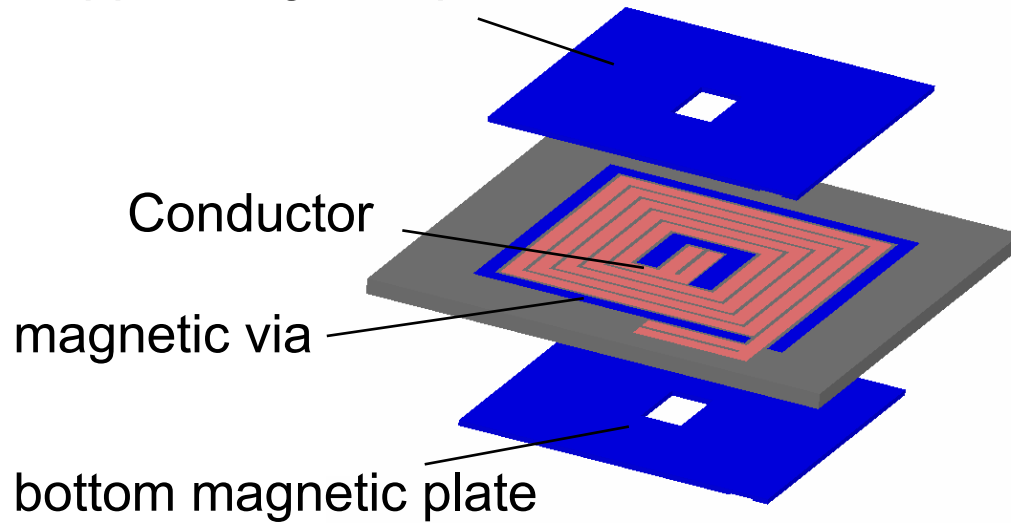
**Our Approach:** *Fabricated **INTO** (through wafer) silicon substrate*



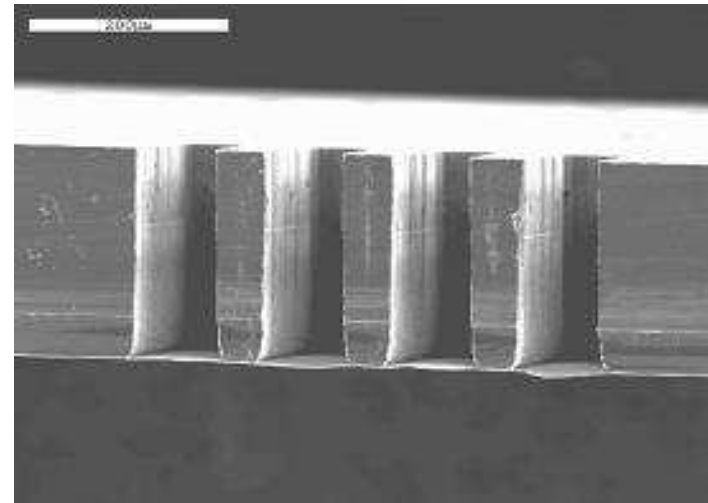
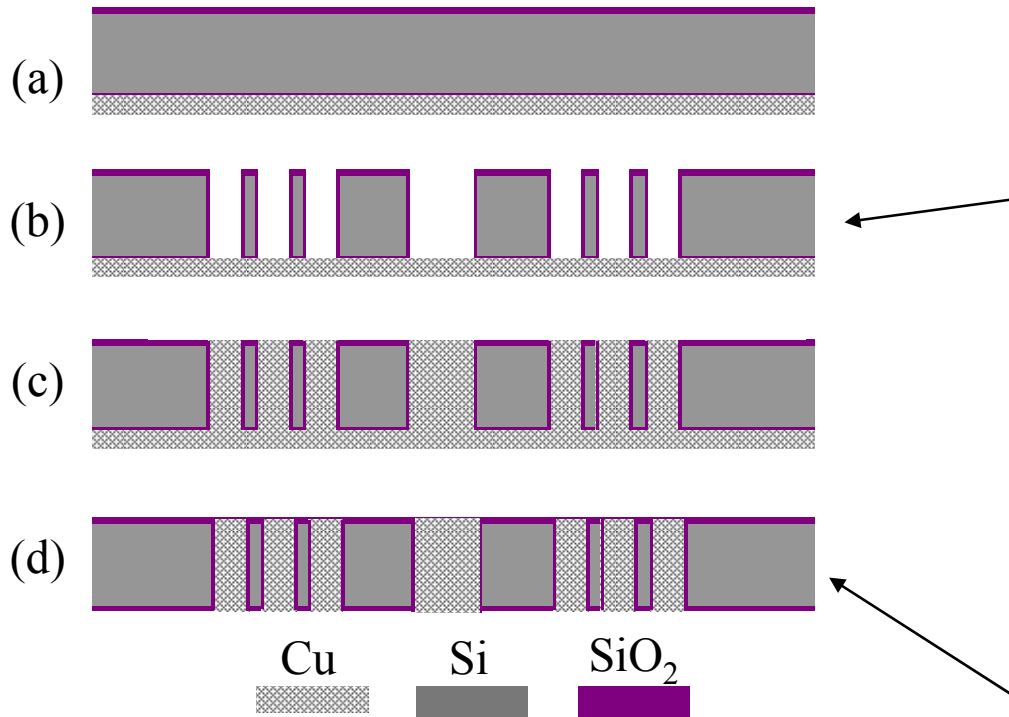
- ❖ Copper as thick as silicon substrate (200  $\mu\text{m}$ ~500  $\mu\text{m}$ )
- ❖ Three metal layers distribute at frontside, backside and inside of substrate
- ❖ Closed Magnetic path
- ❖ Excellent thermal dissipation
- ❖ Through-wafer metal can be used as interconnections for three-dimension packaging, and also ready for packaging

# Inductors In Silicon

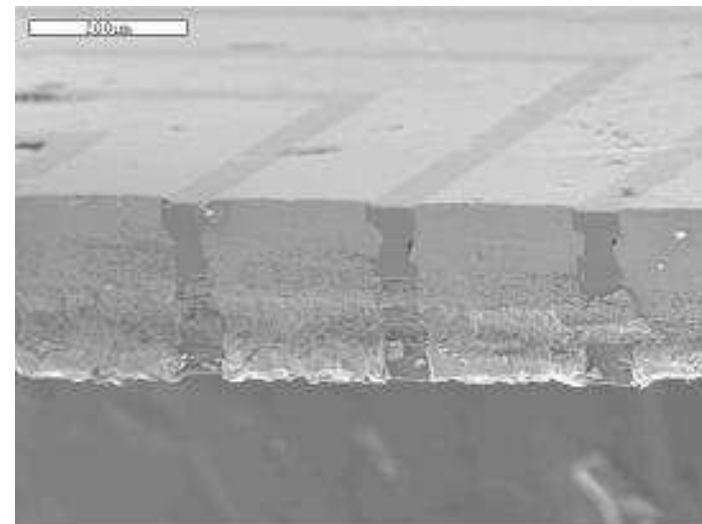
Upper magnetic plate



Cross-section view along A-A'



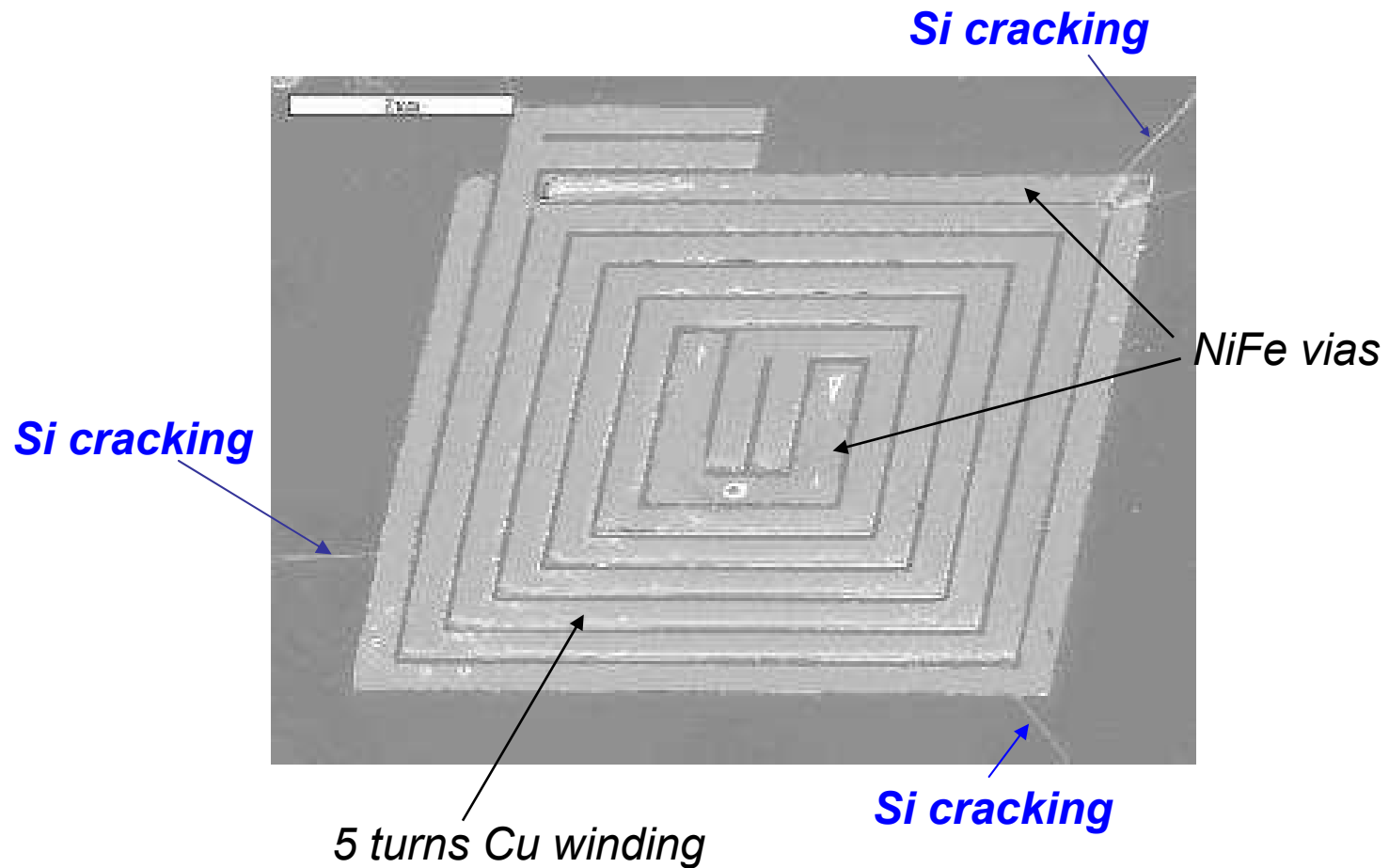
SEM of (b)



SEM of (c)

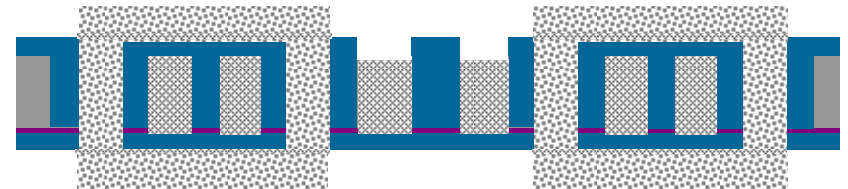
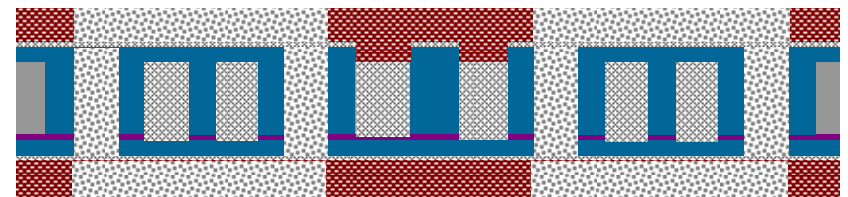
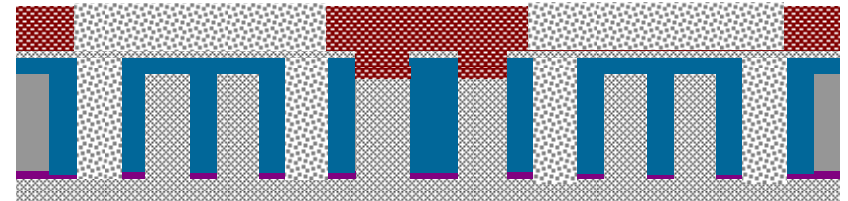
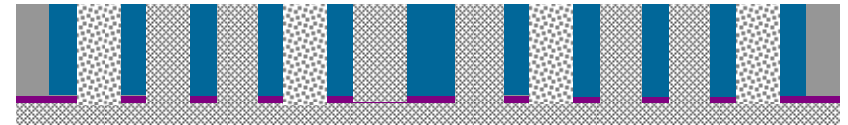
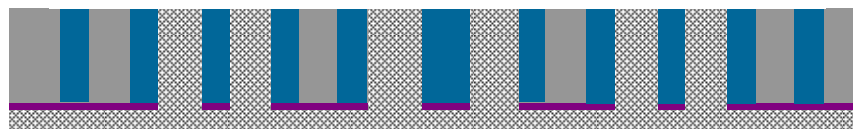
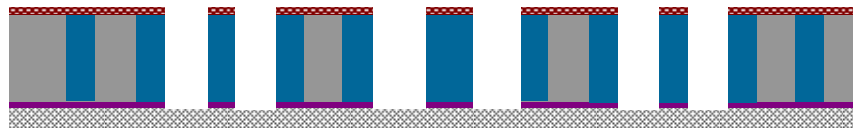
- (a) 10 μm Cu deposition on the backside
- (b) Through-wafer Si trenches by DRIE
- (c) Metal electroplating and surface polishing
- (d) removal of the 10 μm-thick Cu on the backside.

# Reported Problem



Thermal stress due to the difference of thermal expansion coefficient

# SU-8 Enhanced Process



# Fabricated Device

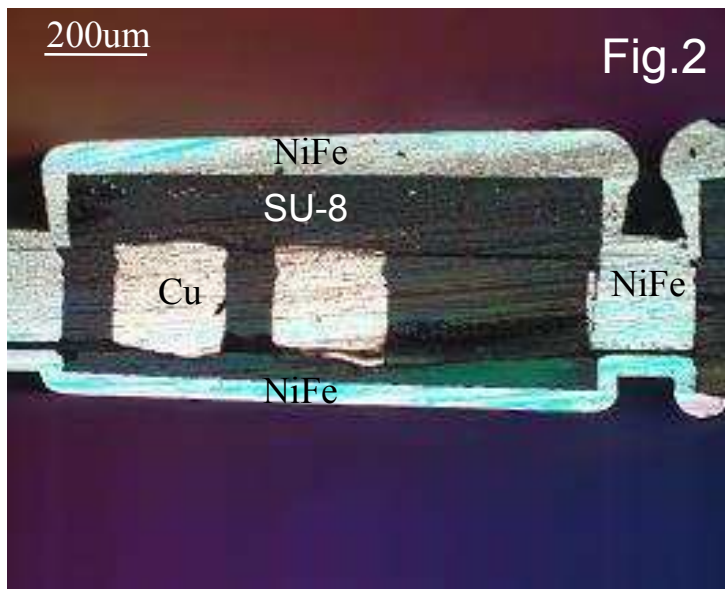
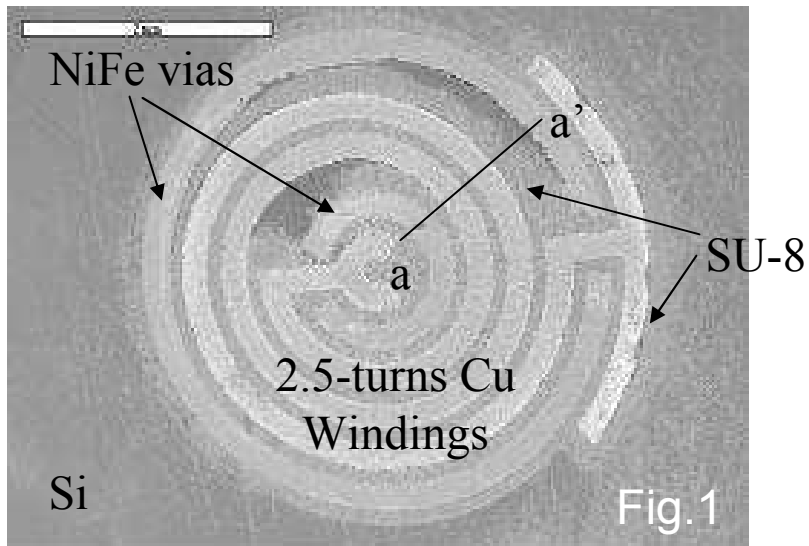
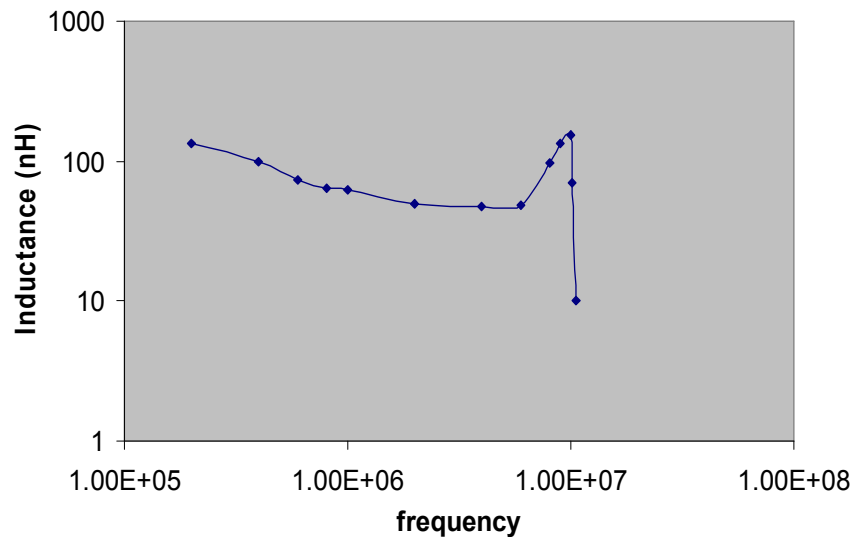


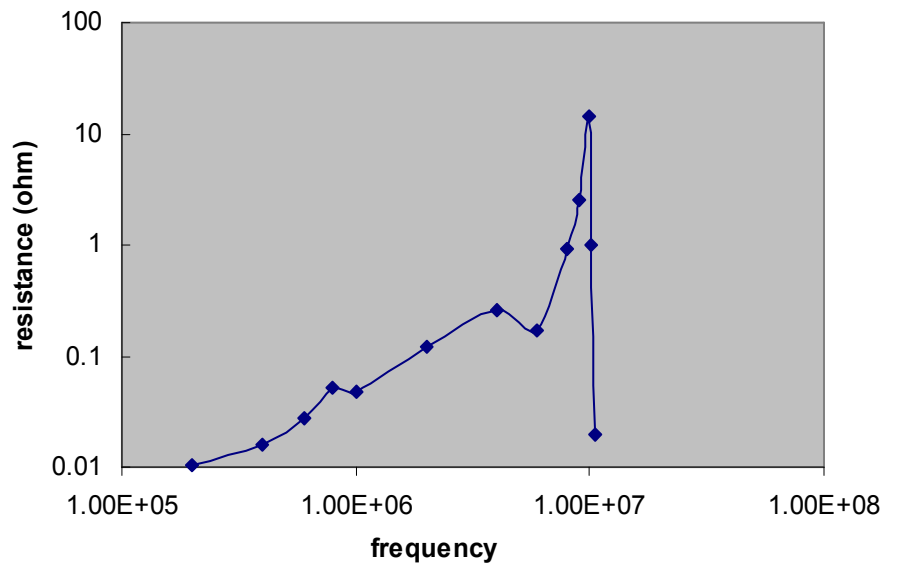
Fig.1 Metals inside the silicon wafer  
 Fig.2 Cross-section view along A-A'  
 Fig.3 Top view of fabricated device



(1) DC resistance: **10.1 mΩ**



(2) Inductance versus frequency



(3) AC resistance versus frequency

- State-of-art technologies were reviewed
- Concept of Silicon Molding Technique was demonstrated
- SU-8 Enhanced Process was developed to solve the thermal crack problems
- An inductor with 134 nH and 10 m $\Omega$ DCR was fabricated
- Magnetic material should be replaced by high frequency material to reduce the loss

Questions?