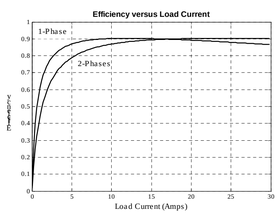

Intelligent Power Management Group, University of Limerick: Activities 2008

Dr. Tony Scanlan, Dr. Mark Halton
Department of Electronic & Computer Engineering, University of Limerick.
Email: mark.halton@ul.ie

Abstract:

The Intelligent Power Management Group (IPMAC) at the University of Limerick Ireland is involved in the design of key technologies for digital integrated power supply controllers. This poster details active projects within the group for the current year 2008, and outlines a roadmap for future technology development. Current funded projects include the development of improved efficiency power converters for nonisolated POL voltage regulators, particularly at light load. This will be achieved through circuit and advanced control techniques. Coupled with this research strand is the development of event-driven digital control laws for improved VRM transient performance. Complementary to the above activities is the development of integrated circuit and power supply technologies for demonstration and commercialisation purposes.

1. Digital Power SoC incoporating Time/Event Driven Control (EdCON):

The objectives of this research work is to develop, implement and characterise new *event-driven* control algorithms for VRMs. This will be achieved through the development of analogue "event estimation" circuitry and a DSP core architecture which is designed to compute multiple parallel control laws necessary for VRMs. This event detection approach coupled with new digital control laws offers superior transient performance over conventional control schemes.

The proposed concept will implement a fundamentally new type of VRM control. This concept provides a framework for implementing novel control algorithms with greater flexibility to significantly improve the performance of VRMs since it is based on varying sampling time. In our proposed system (Figure 1.1), it is the occurrence of a VRM system event e.g. a change in the average output current, which can be used to take a sample.

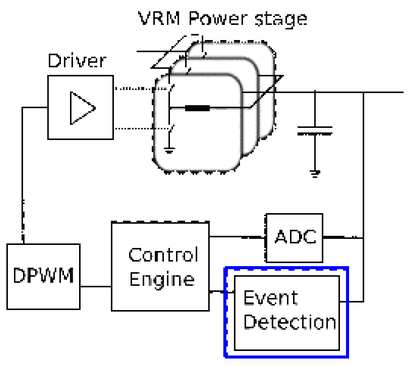

Figure 1.1 Proposed EdCON Concept

This estimation method will be coupled with optimised digital control laws to achieve improved performance. Digital control algorithms and implementations are necessary in future designs as power conversion applications trend towards multiple phases and multiple power rails.

Preliminary research results have been presented at PESC 2008 and PCIM 2008 [1,2]. Simulation results indicate improved transient performance when compared to a typical step response. To illustrate, Figure 1.2 shows the output voltage response, using this new approach (blue) for a 50A load step compared to a conventional digital design (green). Full details included in [1,2].

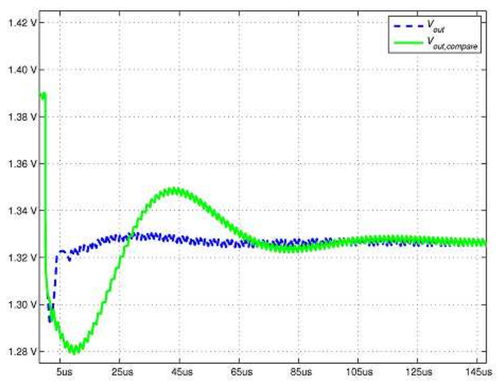

Figure 1.2 Output Voltage Transient Response

[1] Effler S., Halton M., Kelly A. and Krüger T. (2008). "Digital control law design using a novel load current estimator principle for improved transient response". Proceedings of the 39th IEEE Power Electronics Specialists Conference PESC '08, 2008.

[2] Effler S., Kelly A., and Halton M. (2008). "Optimization of Generalized Model Predictive Control for DC/DC converters". Proceedings of PCIM 2008, 2008.

2. Digital Controller for High-efficiency DC-DC Conversion (HiECON):

The objective of this research is to allow digital power converters to fulfil the promise of improved power conversion efficiency compared to today's solutions. Focusing on non-isolated point-of-load (POL) voltage regulators, it is proposed to develop circuits, and advanced control techniques which improve converter efficiency, particularly at light-load.

The total loss in switch-mode power converters (SMPCs) does not scale with load current. With SMPC efficiency defined as the ratio of the output load power to the converter input power,

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{Load}}{P_{Loss} + P_{Load}}$$

It is clear that when the load operates with a low current draw (for example during standby), then the efficiency is severely impacted by the fixed losses of the SMP (Figure 2.1).

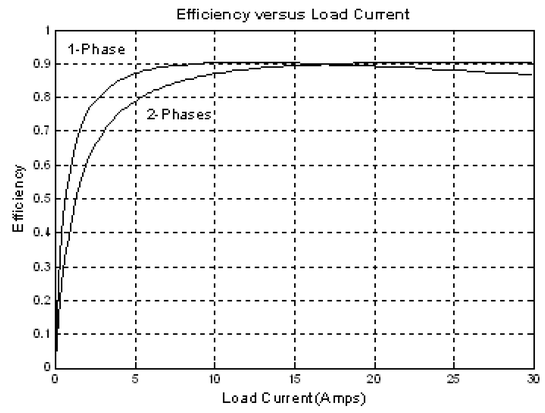

Figure 2.1 SMPC Efficiency versus Load Current

The fixed losses are largely due to switching of the power stage, therefore state-of-the-art control strategies are mainly focused on techniques which allow the switching losses to scale with frequency. Traditionally, these techniques are applicable to analogue SPMC ICs. Broadly with proposed approach, switching losses can be made to scale with load current using current mode control in discontinuous conduction mode (DCM) operation of the SMPC. In this way, the controller varies the switching frequency of the SMPC to control the current supplied to the load. Therefore, switching frequency varies with load current, and hence the switching losses scale with load current. This allows low losses to be achieved at low load current, maintaining high efficiency.

Dead-time optimisation is an important function in an efficient SMPC to minimise the power loss associated with cross-conduction. It may be included in the driver or integrated driver/FET or integrated power-converter/driver/FET. It is proposed to develop IP to optimise the SMPC dead-time using signals which exist in the digital power controller. This technique will use adaptive estimation techniques to implement dead-time optimisation based upon the duty-cycle, producing a more robust convergence than previous methods.

As power conversion applications trend towards multiple phases and multiple power rails, the limited ability of a single computation unit to process control loops in parallel limits the flexibility to implement multiple phases/rails operating simultaneously in the DSP core. It is also proposed to develop a DSP core architecture which is designed to compute multiple parallel control laws, offering the required computing power in the most power and area efficient manner. This DSP core will be implemented on a technology demonstrator involving an FPGA and switch mode power converter, allowing potential commercial partners to evaluate the IP.

3. (Future Work) Low power A/D Conversion for Digital SMPC:

The power consumption P_C of an ADC is dependent on the number of bits N_{BITS} resolved, the sample rate F_S required, and the energy consumption E_C per quantization step (joules per conversion). This final quantity is a function of the ADC architecture and process technology.

$$P_C = E_C f_S 2^{N_{BITS}}$$

Standard full range ADCs such as that detailed in [1] have an energy consumption of the order of ~5pJ for each step resolved. Therefore at a sample rate of 10MHz and with 10bit resolution (1024 steps), the overall power consumption will be ~50mW. This large power consumption coupled with large silicon area may make using a standard ADC unattractive for power converter applications. In order to reduce power consumption to the µW level required for highly efficient, high speed power converters, many designers of digital power converters have chosen approaches that greatly reduced the number of quantization levels resolved by the ADC. The resulting ADCs referred to as window ADCs only operate over a small input voltage range ~100mV. Table 3.1 compares various approaches to A/D conversion in Digital SMPC.

	ADC Type	Conversion Steps	Sample Rate (MS/s)	Power Consumption (µW)	Efficiency: Energy per Conversion Step (pJ)
1	Flash ADC [2]	2	3	30	5
2	Delay Line ADC [3]	10	1	50	5
3	VCO [4]	6	0.5	37	12
4	Pipeline [1]	1024	40	55e3	1.3

Table 3.1 Comparison of ADC for Digital SMPC

Recent developments in state of the art design of ADCs have focused on improving the energy efficiency of ADCs. Values of EC in the ~fJ range have been reported [5,11]. By improving converter efficiency to the fJ level, µW power consumption is achievable with wide input voltage ranges and high resolution at high sample rates. Table 3.2 summarises recent highly efficient ADC architectures. Compared to the designs in 3.1 it is noted that E_C performance is much improved and a wider conversion range could be achieved for the same power consumption. In particular [6] achieves best E_C to date in a CMOS process.

	ADC Type	Conversion Steps	Sample Rate (MS/s)	Power Consumption (mW)	Energy per Conversion Step (pJ)
1	Pipe[5]	1024	7.9	28	0.35
2	SAR [6]	512	10	0.290	0.056
3	Pipe [7]	1024	120	90	1.25
4	Pipe [8]	1024	12	3.3	0.76
5	Pipe [9]	1024	125	40	0.79
6	Pipe [10]	1024	100	35	0.6
7	Pipe [11]	1024	100	33	0.69

Table 3.2 Comparison of Recent Low E_C ADCs

Figure 3.1 compares the power consumption required for two converters of differing E_C. Clearly a converter with low E_C allows a greater number of quantization levels to be achieved for a given power consumption. The proposed project involves development of a high efficiency A/D converter in a low geometry CMOS process for digital power conversion applications.

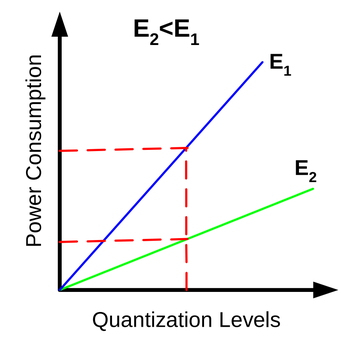

Figure 3.1 Comparison of Two Converters with differing E_C