Abstract:

The Intelligent Power Management Group (IPMAG) at the University of Limerick, Ireland is involved in the design of key technologies for digital integrated power supply controllers. This poster details active projects within the group for the current year and outlines a roadmap for future technology development. Current funded projects include the development of improved efficiency power converters for non-isolated POL voltage regulators, particularly at light load. This will be achieved through circuit and advanced control techniques. Coupled with this research strand is the development of event-driven digital control laws for improved VRM transient performance. Complementary to the above activities is the development of integrated circuit and power supply technologies for demonstration and commercialisation purposes.

1. Digital Power SoC incorporating Time/Event Driven Control (EdCON):

The objectives of this research work is to develop, implement and characterise new event-driven control algorithms for VRMs. This will be achieved through the development of analogue event estimation circuitry and a DSP core architecture which is designed to compute multiple parallel control laws necessary for VRMs. This event detection approach coupled with new digital control laws offers superior transient performance over conventional control schemes.

The proposed concept will implement a fundamentally new type of VRM control. This concept provides a framework for implementing novel control algorithms with greater flexibility to significantly improve the performance of VRMs since it is based on varying sampling time. In our proposed system (Figure 1.1), it is the occurrence of a VRM system event e.g. a change in the average output current, which can be used to take a sample.

![Figure 1.1 Proposed EdCON Concept](image)

This estimation method will be coupled with optimised digital control laws to achieve improved performance. Digital control algorithms and implementations are necessary in future designs as power conversion applications trend towards multiple phases and multiple power rails.

Preliminary research results have been presented at PESC 2008 and PCIM 2008 [1,2]. Simulation results indicate improved transient performance when compared to a typical step response. To illustrate, Figure 1.2 shows the output voltage response, using this new approach (blue) for a 50A load step compared to a conventional digital design (green). Full details included in [1,2].

![Figure 1.2 Output Voltage Transient Response](image)

2. Digital Controller for High-efficiency DC-DC Conversion (HiECON):

The objective of this research is to develop an efficient digital power converter to fully realise the potential of improved power conversion efficiency compared to today’s solutions. Focusing on non-isolated point-of-load (POL) voltage regulators, it is proposed to develop circuits, and advanced control techniques which improve converter efficiency, particularly at light-load.

The total loss in switch-mode power converters (SMPCs) does not scale with load current. With SMPC efficiency defined as the ratio of the output power to the converter input power, it is clear that when the load operates with a low current load (for example during standby), the efficiency is severely impacted by the fixed losses of the SMPC (Figure 2.1).

![Figure 2.1 SMPC Efficiency versus Load Current](image)

The fixed losses are largely due to switching of the power stage, therefore state-of-the-art control strategies are mainly focused on techniques which allow the switching losses to scale with frequency. Traditionally, these techniques are applicable to analogue SPIMC ICs. Broadly with proposed approach, switching losses can be made to scale with load current using current mode control in discontinuous conduction mode (DCM) operation of the SMPC. In this way, the controller varies the switching frequency of the SMPC to control the current supplied to the load. Therefore, switching frequency varies with load current, and hence the switching losses scale with load current. This allows low losses to be achieved at low load current, maintaining high efficiency.

Dead-time optimisation is an important function in an efficient SMPC to minimise the power loss associated with cross-conduction. It may be included in the driver or integrated driver/FET or integrated power controller/driver/FET. It is proposed to develop IP to optimise the SMPC dead-time using signals which assist in the digital power controller. This technique will use adaptive estimation techniques to implement dead-time optimisation based upon the duty-cycle, producing a more robust convergence than previous methods.

As power conversion applications trend towards multiple phases and multiple power rails, the limited ability of a single computation unit to process control loops in parallel limits the feasibility to implement multiple phases/rails operating simultaneously in the DSP core. It is also proposed to develop a DSP core architecture which is designed to compute multiple parallel control laws, offering the required computing power in the most power and area efficient manner. This DSP core will be implemented on a technology demonstrator involving an FPGA and switched/mode power converter, allowing potential commercial partners to evaluate the IP.

3. Low Power A/D Conversion for Digital SMPC:

The power consumption $P_p$ of an ADC is dependent on the number of bits $N_{p}$, the sample rate $f_s$, and the energy consumption $E_p$ per quantization step (pJ/pers conversion). This final quantity is a function of the ADC architecture and process technology.

$$P_p = E_p \cdot f_s$$

Standard full range ADCs such as that detailed in [1] have an energy consumption of the order of ~5pJ for each step resolved. Therefore at a sample rate of 10MHz and with 10bit resolution (1024 steps), the overall power consumption will be ~50mW. This large power consumption coupled with large silicon area may make using a standard ADC intractable for power converter applications. In order to reduce power consumption to the uW level required for highly efficient, high speed power converters, many designers of digital power converters have chosen approaches that greatly reduce the number of quantization levels resolved by the ADC. The resulting ADCs referred to as window ADCs only operate over a small input voltage range ~100mV. Table 1.1 compares various approaches to A/D conversion in Digital SMPC.

![Figure 3.1 Comparison of ADC for Digital SMPC](image)

Recent developments in state of the art design of ADCs have focused on improving the energy efficiency of ADCs. Values of EC in the ~fJ range have been reported [5,11]. By improving converter efficiency to the uJ level, uW power consumption is achievable with wide input voltage ranges and high resolution at high sample rates. Table 3.2 summarises recent highly efficient ADC architectures. Compared to the designs in 3.1 it is noted that $E_p$ performance is much improved and a wider conversion range could be achieved for the same power consumption. In particular [6] achieves best $E_p$ to date in a CMOS process.

![Figure 3.2 Comparison of Recent Low $E_p$ ADCs](image)

Table 1.1 Comparison of ADC for Digital SMPC

<table>
<thead>
<tr>
<th>ADC Type</th>
<th>Quantization Levels</th>
<th>Power Consumption</th>
<th>Efficiency: $E_p$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard</td>
<td>10 bits</td>
<td>5pJ/pers conversion</td>
<td>~50mW</td>
</tr>
<tr>
<td>Low Power</td>
<td>6 bits</td>
<td>0.6pJ/pers conversion</td>
<td>~10μW</td>
</tr>
<tr>
<td>Window</td>
<td>4 bits</td>
<td>0.1pJ/pers conversion</td>
<td>~1μW</td>
</tr>
</tbody>
</table>

Table 3.2 Comparison of Recent Low $E_p$ ADCs

<table>
<thead>
<tr>
<th>ADC Type</th>
<th>Quantization Levels</th>
<th>Power Consumption</th>
<th>Efficiency: $E_p$</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA</td>
<td>10 bits</td>
<td>50mW</td>
<td>~5pJ/pers conversion</td>
</tr>
<tr>
<td>DSP</td>
<td>6 bits</td>
<td>10μW</td>
<td>~0.6pJ/pers conversion</td>
</tr>
<tr>
<td>Window</td>
<td>4 bits</td>
<td>1μW</td>
<td>~0.1pJ/pers conversion</td>
</tr>
</tbody>
</table>

Figure 3.1 compares the power consumption required for two converters of differing $E_p$. Clearly a converter with low $E_p$ allows a greater number of quantisation levels to be achieved for a given power consumption. The proposed project involves development of a high efficiency A/D converter in a low geometry CMOS process for digital power conversion applications.