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Topology comparison for a system-in-package integrated DC-DC converter for portable electronic applications

F. Haizoune*, H.J. Bergveld†, J. Popović-Gerber#, J.A. Ferreira*

*Delft University of Technology, Delft, The Netherlands

†NXP Semiconductors, Eindhoven, The Netherlands

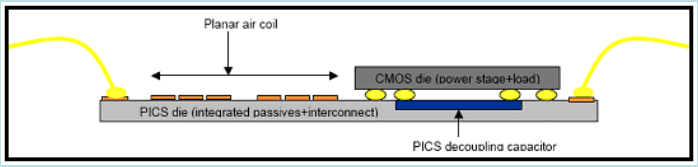
#European Centre for Power Electronics (ECPE), Nurnberg, Germany

DC/DC converters for portable applications

- Interface between battery and load
- Application requirements:
  - High conversion efficiency for longer battery life → topology and technology considerations
  - Small size for portability → high switching frequency
  - Low cost for consumer applications → die size and integration level optimisation
- Monolithic integration of passives in silicon challenging → System-in-Package (SiP)
- Specs: V_{in} = 3 ~ 4.2V (Li-ion battery), I_{out} = few mA ~ several 100 mA, V_{out} = 0.6 V ~ 1.2 V

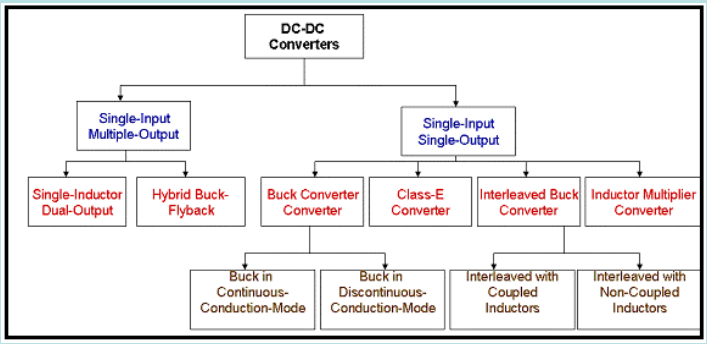
Technology platform

- NXP technology platform
- 65nm CMOS technology - for future possibility of load integration
- Passive-Integration Connective Substrate (PICS)
  - High density integrated capacitors – 80nF/mm² and beyond
  - Planar inductor – spiral air core or electroplated magnetic core (Tyndall)

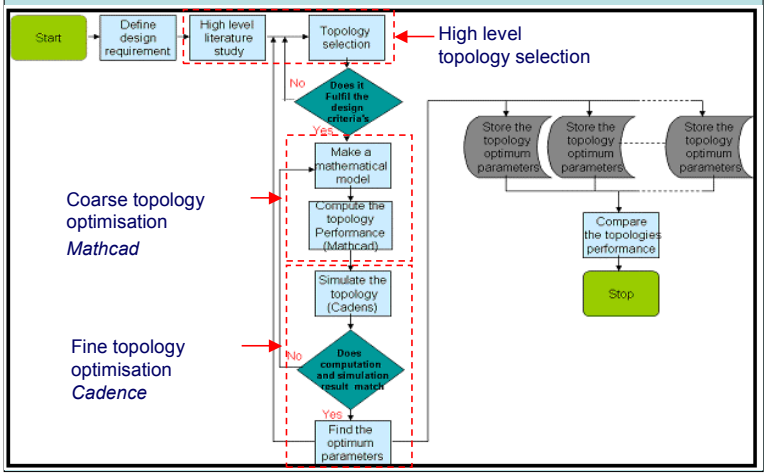


Topology tree

- Single and dual output topologies analysed



Flowchart



High level topology decision making

- Weighing factors for the evaluation criteria: efficiency, size, cost, transient response, technology feasibility
- Each topology evaluated on the basis of the criteria

Criteria	FoI	Buck	Interleaved Buck	Class- E	Inductor Multiplier	Single Inductor Dual-Output
Efficiency	3	2/3 (integr. inductor)	3/3	2/3 (circulating currents in res. tank)	1/3 (losses almost 2X that of off-chip inductor)	2/3 (additional switches)
Size	3	3/3	2/3 (multiple stages)	1/3 (multiple conversion stages)	3/3	3/3
Cost	3	3/3	2/3 (add. control circuitry)	1/3 (large silicon area)	3/3	3/3
Transient Response	2	3/3	3/3	2/3 (size of RF input inductor)	1/3 (ripple cancellation)	2/3 (regulation of different outputs)
Feasibility	3	3/3	3/3	3/3	3/3	3/3
Total		**39/42**	**36/42**	**25/42**	**32/42**	**37/42**

Topology optimisation and comparison

- Coarse optimisation – finding optimum frequency for highest η
- Fine optimisation – including parasitics such as R_{dson} and ESR_l

	Single-Input Single-Output Converter			Single-Input Dual-Output Converter (SIDO)	
I_{out}= 100mA V_{out} = 1V V_{in} = 3.6V	**Buck CCM Air-Core Inductor**	**Buck DCM Air-Core Inductor**	**Buck Magnetic core Inductor (CCM)**	**SIDO (DCM, Air-core inductor)**	**Two buck (DCM, Air-core inductor)**
L [nH]	18.92	18.88	199	18.96	18.88(x2)
ESR_L [Ω]	1.40	1.25	1.05	1.03	1.25(x2)
R_{ON_PMOS} [Ω]	2.01	1.82	0.48	0.86	1.82
$f_{s,opt}$ [MHz]	140	120	10	160	140
R_{ON_NMOS} [Ω]	0.97	0.88	0.23	0.42	0.88
η [%]	59.35	66.05	72.29	56.753	66.05