From Dual Die PwrSoC
To Monolithic PwrSoC

September 24, 2008
Overview

- Markets & Applications
- Strategy: From Dual Die to Single Die (Monolithic) For PwrSoC
- Milestones of Dual Die PwrSoC
- Inductor Design Issues
- Progression Towards Monolithic
Industry wide system demands are challenging power designs to deliver **Higher Efficiency, Smaller Size and Lower Noise**

**Energy Utilization**
- Reduction of OpEx
- Extension of battery life
- Improved thermals in constrained designs

**New Services and Applications**
- Driving additional functions
  - Adding more power rails
- In a constrained or shrinking board size

**Broadband Technology**
- Wireless and networking data rates increasing
- Reduction of jitter, ripple, EMI critical to achieve higher speeds
Innovating Power Designs

Engineered from the start to enable the industry’s first power system-on-chip solution

- High frequency design in proprietary CMOS
- Proprietary integrated inductor technology
- Package architecture enabling leading edge performance
- System level RF & EMI design for high performance

**LDO Replacement:** Address space constraint challenges while tripling power efficiency in ultra low noise environments

**Noisy DC-DC Replacement:** Replace offending noisy DC-DC with an ultra quiet, high-efficiency DC-DC converter

**Alleviating the Space Crunch:** Miniaturize traditional discrete DC-DC
PwrSoC’s Deliver Value

**Highest Power Density from Milli-Amps to Tens of Amps**
- Tiny Package/Low Profile
- Low Part Count and Small Solution Footprint

- Reduces board area
- Enabling smaller designs with more features

**Ultra-Low Ripple & Noise**
- Up to 95% less Ripple
- Low Conducted and Radiated Noise

- Superior RF performance
- Higher data rate capability

**High Performance**
- Excellent Transient Response
- Load Matched to Technology
- Very High Efficiency: up to 95%

- Glitch-free error performance
- Excellent match to <90nm technology
- Enables superior battery savings

**Ease-of-use**
- Simple Design
- Fully-tested Gerber files provided

- Fast Time-to-Market and rapid reuse
- Design in Hours not Weeks or Months
## Markets Served by PwrSoC’s

<table>
<thead>
<tr>
<th>Markets</th>
<th>Applications</th>
<th>Value to Customer</th>
</tr>
</thead>
</table>
| **Personal Mobile**| • PC Cellular Data Cards  
                     • Navigation (GPS)  
                     • Media Players | • Smallest Footprint  
                     • Low noise  
                     • Energy Efficiency |
| **Home Entertainment**| • Audio Amplifiers  
                       • DVR  
                       • Blu-ray Disc Players  
                       • Digital TV | • Low noise  
                       • Energy Efficiency  
                       • Ease of use |
| **Enterprise**     | • Servers  
                     • Storage Controllers  
                     • Solid State Drives  
                     • Office Automation | • Smallest Footprint  
                     • Energy Efficiency |
| **Telecom Access** | • DSL/GPON  
                      • Cellular Base Stations | • Smallest Footprint  
                      • Energy Efficiency  
                      • Solution cost |
Strategy For Commercial Realization of PwrSoC
(Dual Die Transition to Single Die)

♦ Establish market viability and reliability track record for PwrSoC today
♦ Define technical operating conditions required to achieve single die solution
♦ Take advantage of current advanced assembly and components consistent with these technical operating conditions
♦ Use existing inductor technology to initially achieve the competitive cost thresholds
♦ Continue to work the manufacturability and cost of the single die solutions
  • Focus on applications for which the monolithic approach can provide a compelling technical advantage
Dual Die PwrSoC Approach

(change)

Output Current Range
- 0.3A thru 9A

Manufacturability
- Yield

Quality & Reliability
- System level performance with IC reliability
  - JEDEC, JESD
- MSL 3 260°C peak solder reflow temperature profile
- FIT rate = 6.1 (MTBF ≈ 18700 years)

Technical Performance
- Transient response
- Noise performance
- Ripple performance
- Efficiency
Dual Die PwrSoC Approach
(Design for Manufacturability Challenges)

♦ Discrete Inductor Size Compatibility With Semiconductor Packaging
  • Molding compound
    – Stress effects on magnetic characteristics
      o inductance & ac power loss
    – Overhead coverage/clearance
    – Sufficient volume to constrain internal reflow of solder joints
  • MSL issues
    – Balance
    – Solder reflow
  • MTBF
    – Combine inductor reliability with silicon reliability

♦ Die to Substrate Connections
  • Inductance effects on switching losses

♦ Layout
  • Trade-off between efficiency & noise

♦ Thermal Dissipation
  • Distribution of power losses

Minimize inductance of conduction path to reduce rise time
Typical Inductor Design Criteria
(Physical Parameters of Commercially Available Inductors)

♦ Physical Size
  • Profile dictated by application and market
  • Footprint dictated by cost and application

♦ Terminations
  • Location
    – Effect on layout
      o Trade-off become flow of power current and clearance from wire bonds
  • Metalization
    – Choice of manufacturing i.e wire bond, smt, etc
      o Au => wire bonding if flatness and hardness is met
      o Sn, SnAg or SnAgCu => smt
  • Size
    – Solder volume
Dual Die to Single Die Solution
*(Transition Strategy)*

♦ Address physical size of inductor consistent with wafer manufacturing process

♦ Revisit inductor design rules
  - Inductance value required to meet ripple voltage
  - Effect of power loss on distribution overall power loss budget

♦ Cost effective interconnect technology
Inductor Sizing

(Design Hierarchy)

- High $L_S$
  - Low DCR & $R_S$
  - Low C, Shielding

- Low $L_S$
  - Manufacturability
  - Yield
  - Reliability
Inductor Size Progressions
(Commercial Discrete Inductors Vs Monolithic Solution)

Multi layers inductors provide cost competitive solutions for applications that allow overall device height > 0.8 mm

Monolithic approach provide cost competitive solution for footprints < 2 mm² and a technical advantage for applications that require a device height < 0.6 mm
Traditional Inductor Design Criteria

(普通话 Parameters)

L VS \( I_{\text{OUT}} \) Based on \( \Delta V / V_{\text{full load}} = \text{Constant} \)

Increasing Frequency for \( \Delta V / I_{\text{OUT}} = 0.2 \)

DCR VS \( I_{\text{OUT}} \) for \( V_{\text{OUT}} = 1.2V_{\text{DC}} \)

DCR < 0.12 \( \Omega \) corresponds to \( P_{\text{IN}} / P_{\text{OUT}} < 5\% \) for 0.5A

INDUCTANCE SATURATION CHARACTERISTIC

Impedance Magnitude

| 14 |
Inductor Design Criteria
(Power Loss)

\[ P_{AC} = P_{DC} \]

\[ P_{DC} = I_{DC}^2 \times R_{DC} \]
Inductor Design Criteria
(Surveying Small Signal Parameters to Fit Power Loss Budget)

5 MHz (Baseline)

- \( L_S = 400 \, \text{nH} \)
- \( DCR = 0.1 \, \Omega \)
- \( R_S = 0.38 \, \Omega \)

10 MHz (options for same loss as 5 MHz)

- \( L_S = 200 \, \text{nH} \)
- \( DCR = 0.1 \, \Omega \)
- \( R_S = 0.38 \, \Omega \)
  or
- \( L_S = 400 \, \text{nH} \)
- \( DCR = 0.1 \, \Omega \)
- \( R_S = 1.52 \, \Omega \)
Power Loss Distribution
(Pareto - 5V/1V Vs 5V/3.3V - 33% Load Vs Full Load)

\[ V_{IN} = 5V_{DC} \quad V_{OUT} = 1.0V_{DC} \]

\[ V_{IN} = 5V_{DC} \quad V_{OUT} = 3.3V_{DC} \]
Progression From Dual Die to Single Die Solution
(Advantage of Physical Profile)

Discrete Inductor: Alone

Monolithic Solution: Active Inductor (~150 μm)
CMOS circuitry
Progression From Dual Die to Single Die Solution
(Combination of Two Wafer Processing Technologies)

CMOS wafer

Micromachined wafer

Micro Machining Technology
Progression From Dual Die to Single Die Solution
(Overview)

♦ Obstacles
  • Costs
    – Wafer size (150 mm -> 200 mm)
      o Increase die per wafer by increasing wafer size
      o Trade-off inductor function versus silicon function
  • Wafer manufacturing yields
    – Stress effects of copper & magnetic material
      o Wafer warp
        » Less material for less warp Vs more material for better performance
      o Technical performance
        » Effects on physical stress on magnetic properties
  • Package assembly
    – Assembly process effects on magnetic performance
    – Interconnects between inductor and silicon functions

♦ Benefits
  • Overall footprint approaches silicon die size for given profile
  • Reduce cost, yield and reliability issues associated with mixed mode manufacturing (smt + wire bond)
  • Lower inductance and resistances associated with interconnects
Summary
(PwrSoC)

♦ Dual Die Solutions Are Here Today And Serve To
  • Set the pace towards higher switching frequencies
  • Demonstrate market acceptance of PwrSoC
  • Demonstrate manufacturability
  • Establish a reliability track record for PwrSoC
  • Address issues for inductor sizes to be compatible with wafer process
    – adapt distribution of silicon, inductor and packaging losses
    – adapt to established forward package assembly processes
  • Establish capability limits of more conventional inductors

♦ Single Die (Monolithic) Solutions
  • Will be required to meet the challenges of low profile
    – <0.60 mm package height)
  • Address current applications that require
    – LDO sizing and cost with switcher type efficiencies
Wrap Up

Thank You for Your Attention
(Any Questions?)