Design Considerations for Integrated Powertrains

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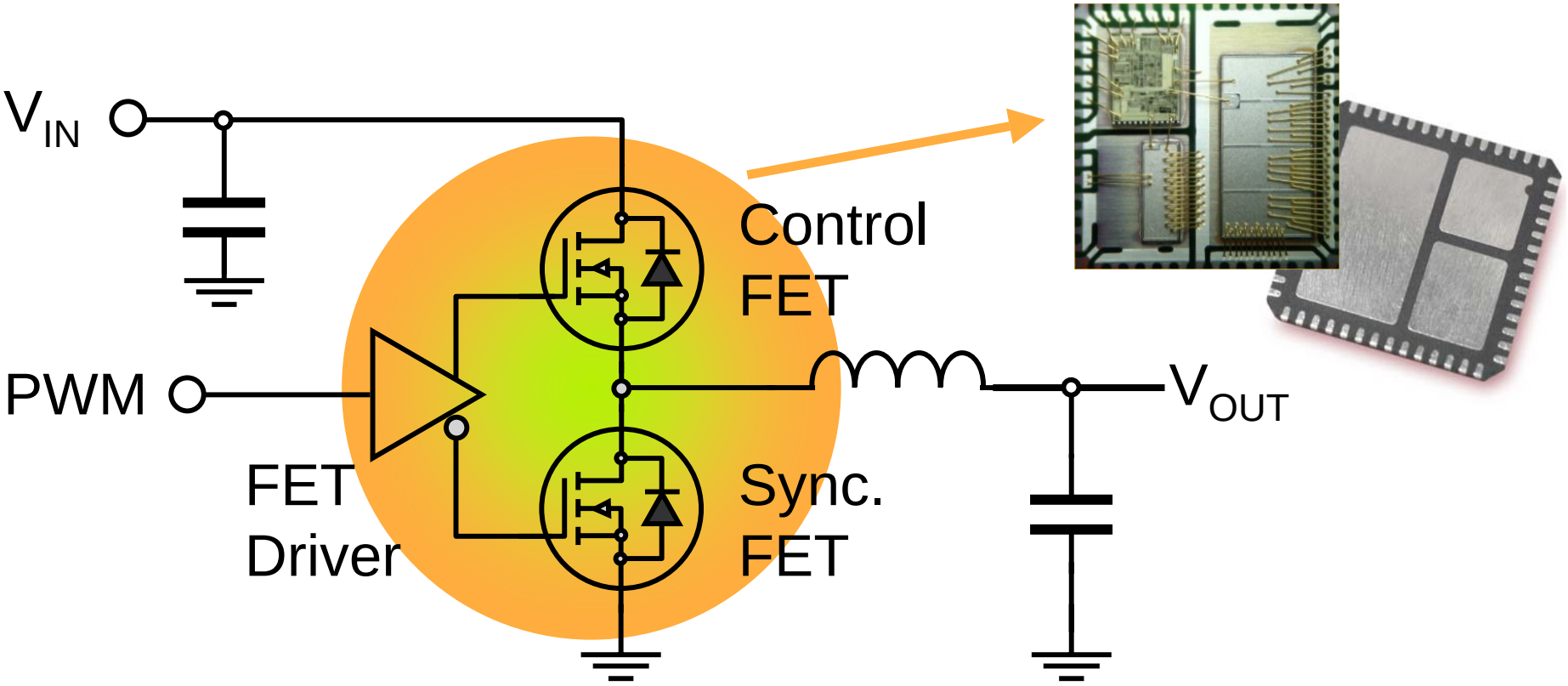
Contents

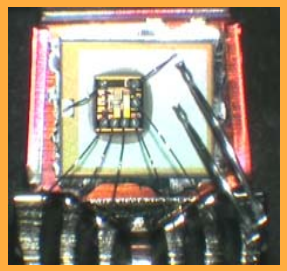
- Introduction to Integrated Powertrains
- MOSFET & Technology Evolution
- Technology Choices
- Power Loss Analysis
- Design Choices
- Future Improvements
- Conclusion

What Is an Integrated Powertrain (DrMOS)?



Focus: 12V Conversion, 20-40A/phase

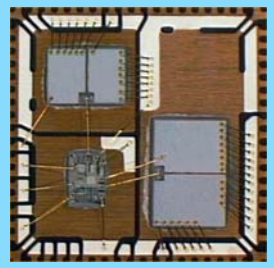
Evolution of Integrated Powertrains



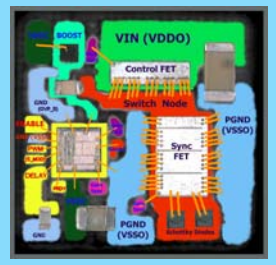
NXP
SAPFET1
1999

NXP
SAPFET2[1]
2000

Std Power Packages



NXP
PIP201
2001
10 x 10 HVQFN



I.R.
IP2001
2001
BGA

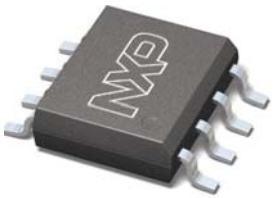
NXP
PIP212
2004[2]
10 x 10 MLF

- Commercial Products emerged in ≈2001
  - Discrete MCM vs. BGA vs. Single chip (e.g. Volterra VT1101)
  - Different approaches by NXP, Int. Rectifier, On Semi, Intersil
- MCM Approach adopted by Intel for DrMOS spec ≈2002-2004[3]
  - Approach adopted by many manufacturers (NXP, Renesas, Fairchild, etc)

[1] SAPFET-2: A Power Module For Power Converters , L.A. de Groot, PCIM 2000
[2] Challenges of Integrated Power Trains, P. Rutter, Intel Technology Symposium 2004
[3] DrMOS Rev 1.0 Nov 2004, http://www.intel.com/design/pentium4/papers/DrMOS.htm

A Decade of Power MOSFET Improvement

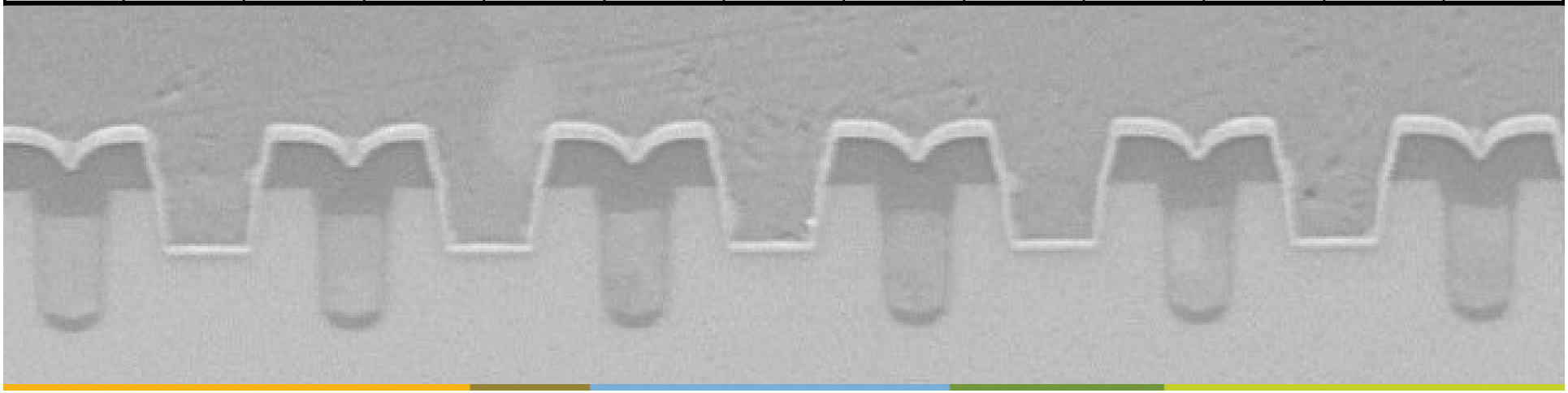
In SO8 footprint ≈90% Reduction in Rds(on) & Rds(on)*Qgd



PHN1013 (30V Vds)
Qgd =10nC, Qgtot =29nC
$Rds(on)_{typ}$ =10mΩ (Vgs=10V)

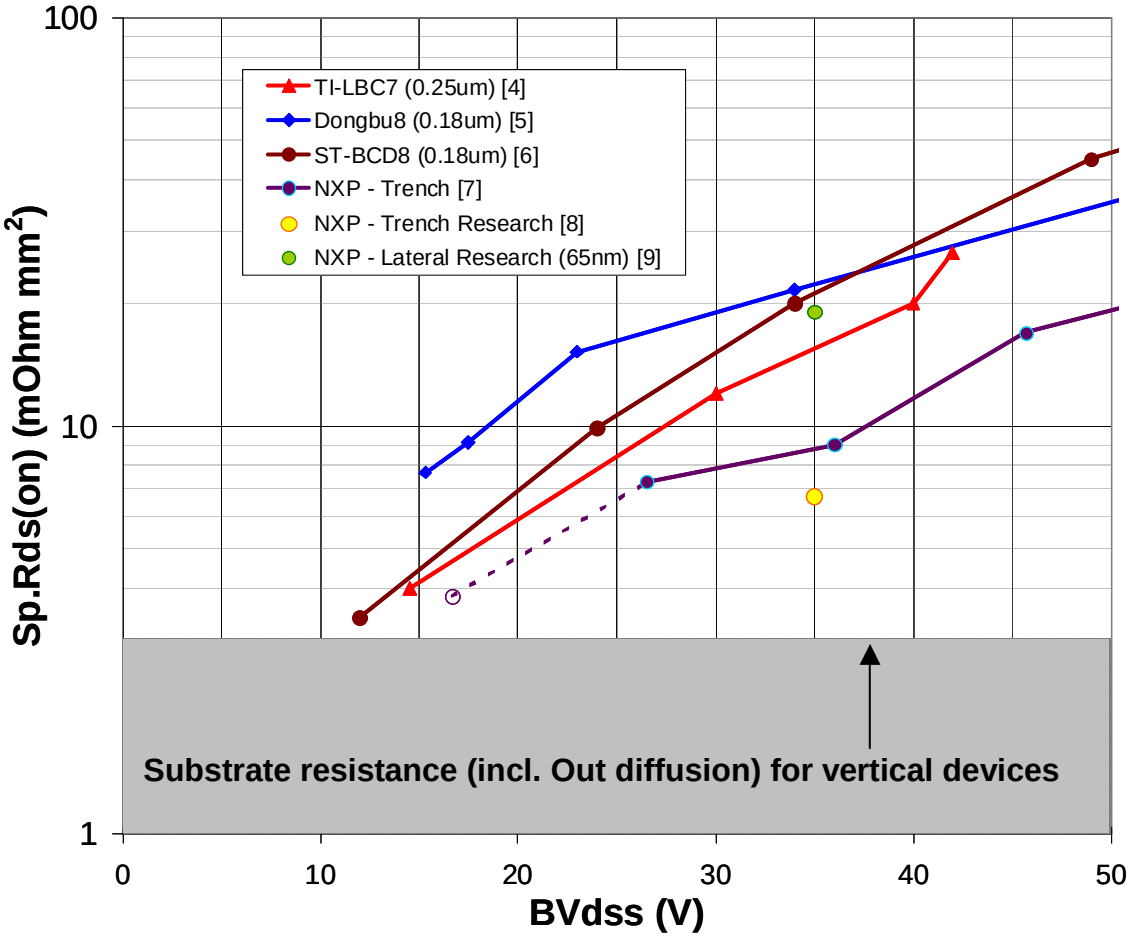
PHSMN1R7-30YL (30V Vds)
Qgd =8.7nC, Qgtot =36nC
$Rds(on)_{typ}$ =1.2mΩ (Vgs=10V)

	1998		2000		2002		2004		2006		**2008**	



Technology Choice: Lateral vs. Vertical

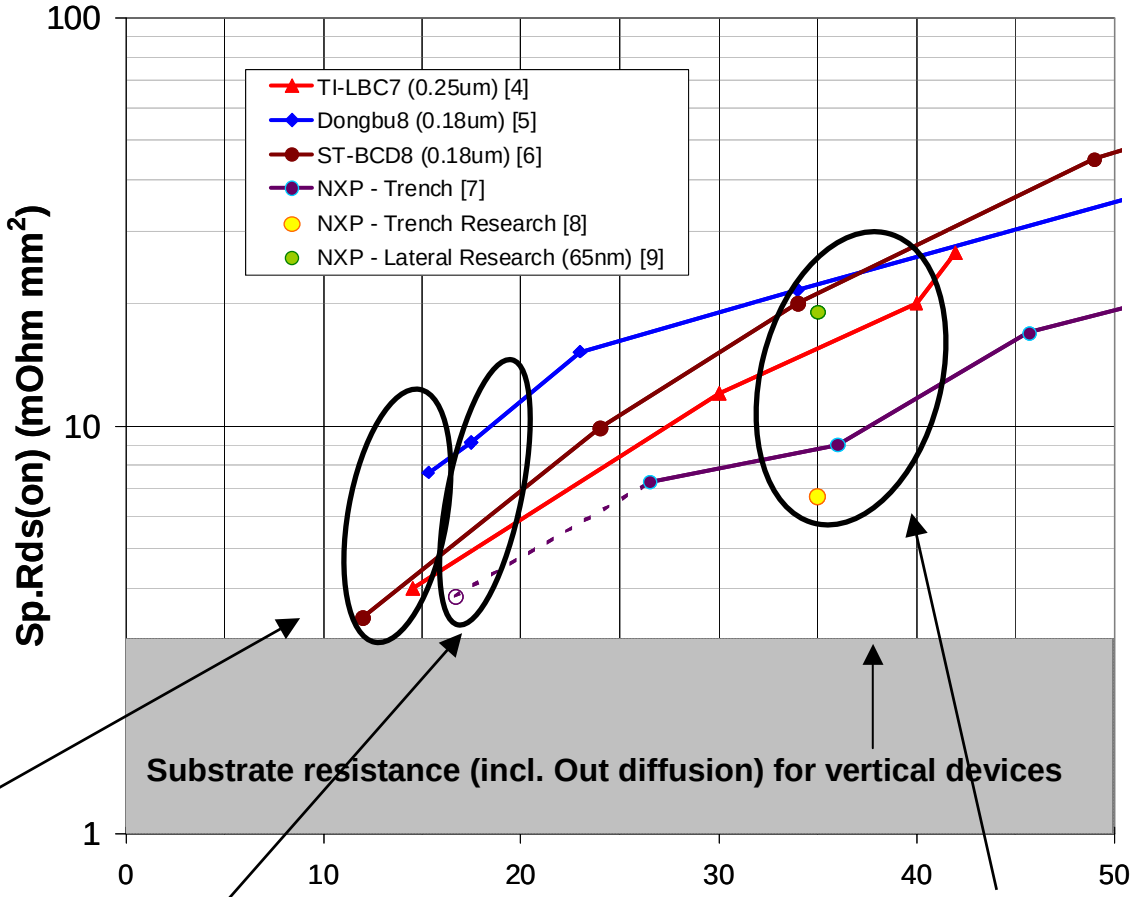
- Monolithic laterals use 3x mask count for discrete MOSFET
  - Only if Power<Logic is it cost effective
  - Laterals tend to need higher BV margin due to SOA
  - Reverse Recovery of Laterals is poor
- Rds(on) of laterals is close theoretical limit (BV requires ≈20V/μm drift length), changes in technology node down to 65nm do not give significant improvement
  - Vertical devices still offer promise of significant improvement (≈factor 2) in Rds(on) and switching FOMs



[4] Pendhakor, ISPSD04
[5] Park, ISPSD08
[6] Riccardi,ISPSD07
[7] Peake,ISPSD08
[8] Goarin,ISPSD07
[9] Heringa, ISPSD08

Technology Choice: Lateral vs. Vertical

- If conversion voltage is reduced to facilitate higher voltage switching then cross-over of lateral vs. vertical is around 5V
- For 3V conversion lateral is best choice due to ease of integration of driver & PWM in single die



7V Rated suitable for 3V Conversion

12V Rated suitable for 5V Conversion

30V Rated suitable for 12V Conversion

[4] Pendhakor, ISPSD04
[5] Park, ISPSD08
[6] Riccardi,ISPSD07
[7] Peake,ISPSD08
[8] Goarin,ISPSD07
[9] Heringa, ISPSD08

Lateral vs. Vertical: Product Comparison

- Latest Vertical trench devices are catching up with Lateral devices FOM
  - No verified data for latest Ciclon technology but looks like 25V 4.5mΩ device has Rds(on)*Qgd of 11.25mΩnC and Rds(on)*Qgtot of 40.5mΩnC at Vds of 12V. Expected performance of next generation trench at 30V.
- For same die area Rds(on) of vertical is <½ of lateral
  - Significant cost advantage for vertical (even discounting higher mask count)

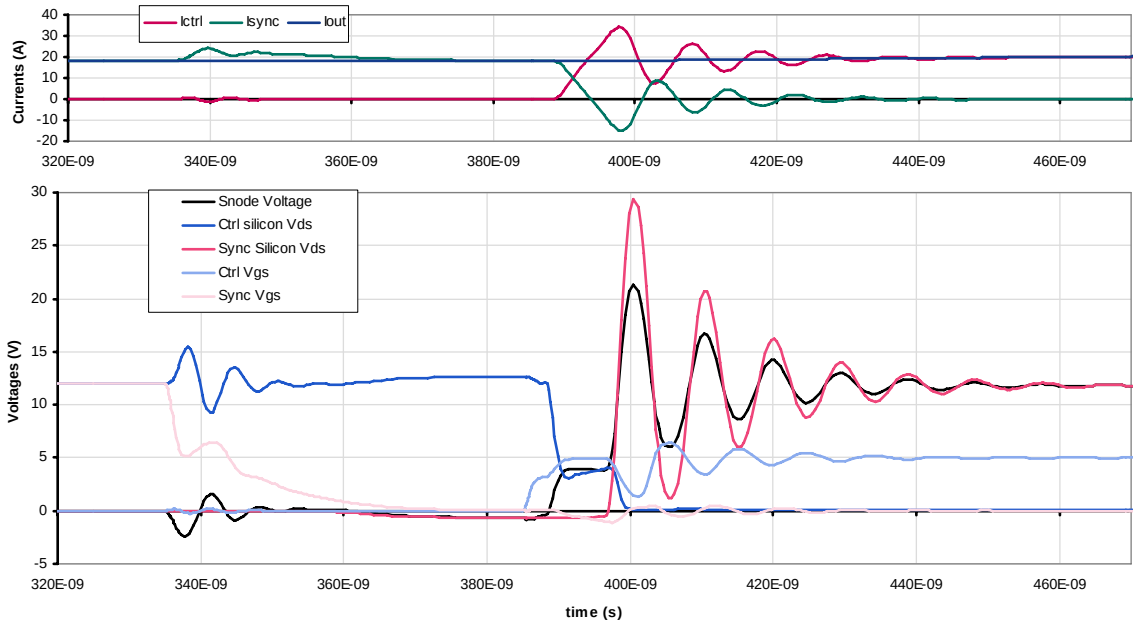
	Lateral	Vertical Trench	
		Same Rds(on)	Same Die Size
	GWS12N30[10]	PSMN5R0-30YL[10]	PSMN2R0-30YL[10]
BVdss	30V	30V	30V
Typ. Rdson @4.5V	5mΩ	5mΩ	2.15mΩ
Qgd (@Vds=15V)	4nC[11]	4.4nC[12]	8.7nC[12]
Qgtot (@Vgs=4.5V)	14nC	14.1nC	30nC
Product Rds(on)* Qgd	20mΩnC	22mΩnC	18.7mΩnC
Product Rds(on)*Qgtot	70mΩnC	70.5mΩnC	64.5mΩnC

Note: Difference in FOMs for Vertical devices due to slightly different package resistance

[10] Values taken from product datasheets, except Qgd
[11] Value taken from: Comparative Study of Lateral and Trench Power MOSFETs in Multi-MHz Buck Converter Applications,Yali Xiong et. al, PESC07
[12] Lab measurements with conditions as in [11]

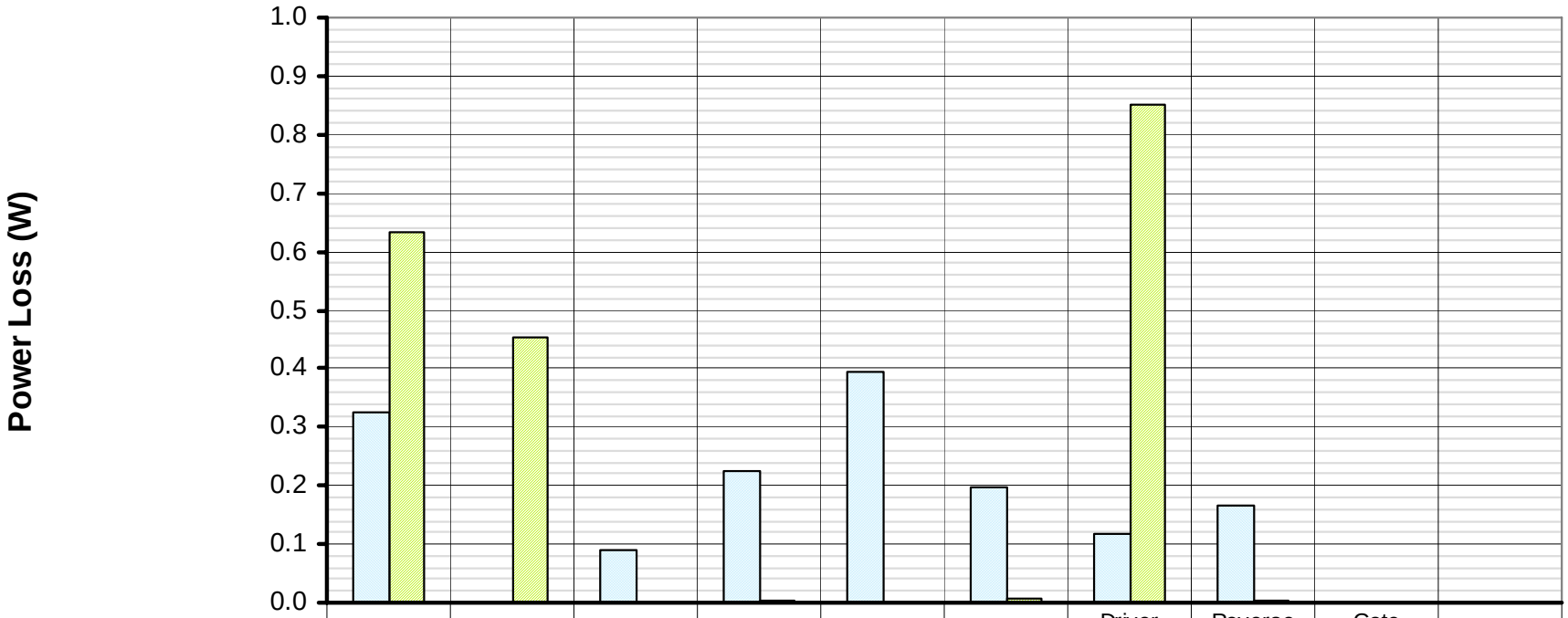
Power Loss Analysis (LFPak (Power SO8) not Int. Powertrain)

- PSpice unsuitable for loss analysis due to poor silicon models
- FEA unsuitable due to lack of PCB parasitics & accurate drive circuit (& very very slow)
- SOLUTION: Build accurate PSpice model!
  - Complex behavioural model ensures accuracy of MOSFET capacitance & reverse recovery



[13] Accurate behavioural modelling of power MOSFETs based on device measurements and FE-simulations, Elferich, R.; Lopez, T.; Koper, N., EPE 2005

Power Loss Breakdown (500KHz, 20A)



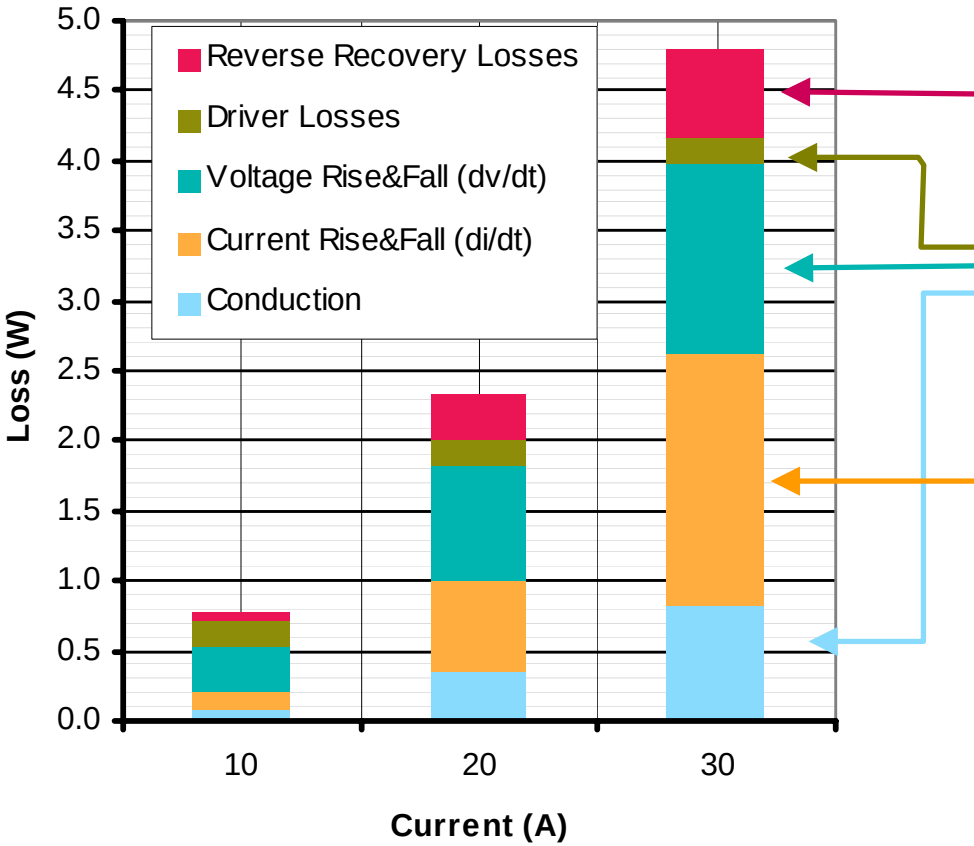
	On State	Dead Time	dI/dt on	dV/dt on	dV/dt off	dI/dt off	Driver losses	Reverse Recovery	Gate bounce	Avalanche
Control FET: Total Loss:1.52W	0.33	0.00	0.09	0.22	0.40	0.20	0.12	0.17	0.00	0.00
Sync FET: Total Loss:1.95W	0.63	0.45	0.00	0.00	0.00	0.01	0.85	0.00	0.00	0.00

- Mathcad used to analyse PSpice waveforms & produce loss breakdown

[14] Quantification of Power MOSFET Losses in a Synchronous Buck Converter, Toni López and Reinhold Elferich, APEC 2008

Control FET Power Loss (1MHz)

- At high currents almost half of the Control FET power loss is independent of the actual Control FET silicon !



Caused by the Reverse Recovery of Sync FET

Related to the Control FET silicon (Qgd, Rds(on), Qgtot)

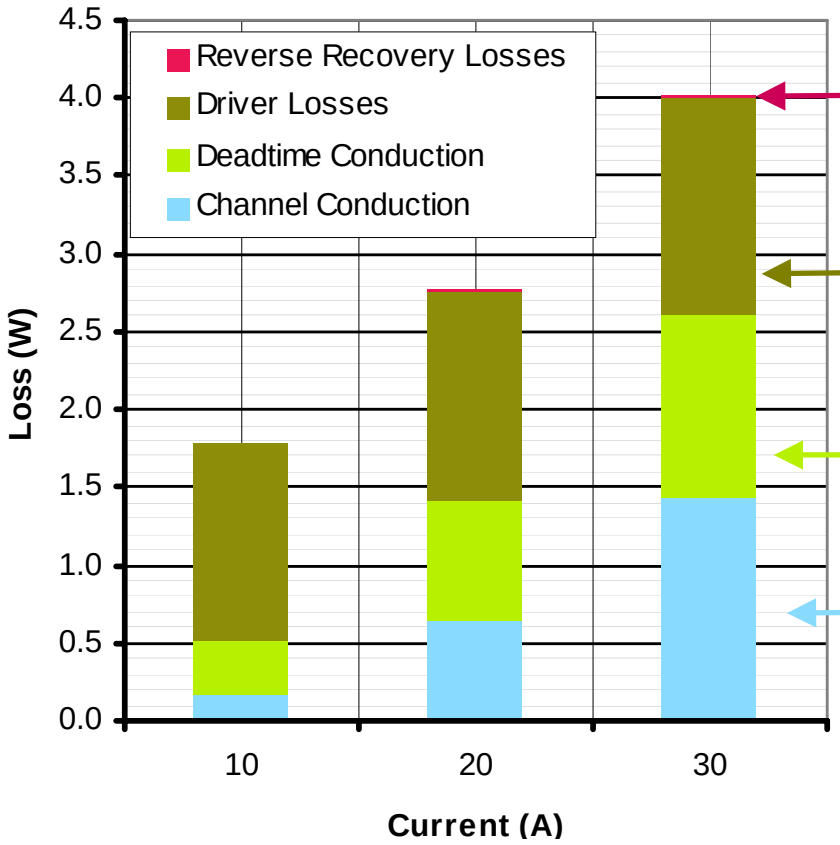
Determined by parasitic inductance: PCB & Package

No.1. Cause of Power Loss

freq=1MHz, Vin=12V, Vout=1.3V

Sync FET Power Loss (1MHz)

- Sync FET Rds(on) is now so low (e.g. 1.2mΩ for PHSMN1R7-30YL) that other loss mechanisms are just as important



Reverse Recovery Losses in Sync FET are negligible
- they occur in Control FET

Related to the Sync FET silicon (Qgtot) and on gate drive voltage

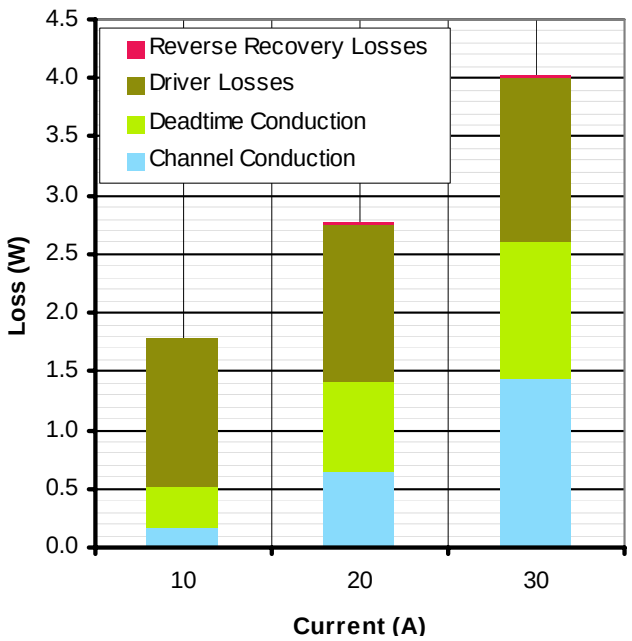
Determined largely by deadtime control of driver IC

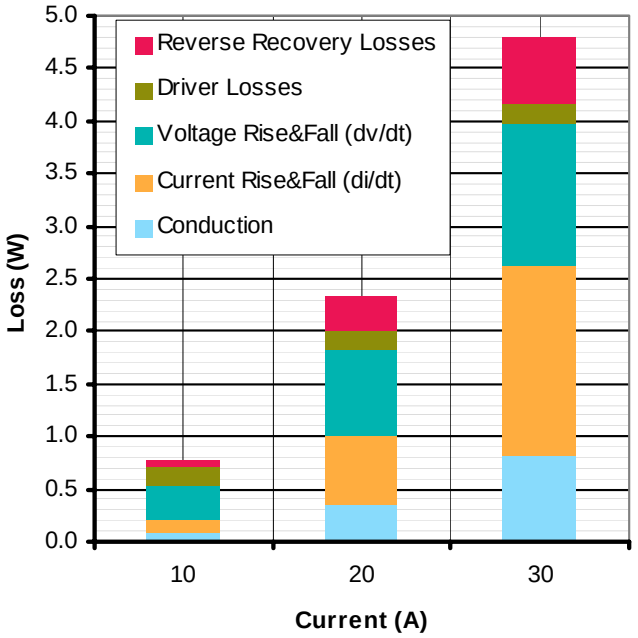
Related to the Sync FET silicon (Rds(on))

freq=1MHz, Vin=12V, Vout=1.3V

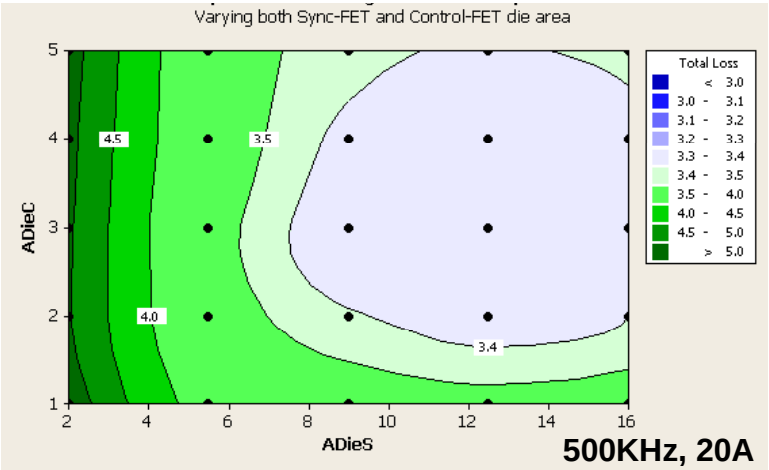
Power Loss Analysis Conclusions

- Improvements in Power MOSFET technology over the last ten years mean that:
  - Qgd is no longer the dominant cause of power loss for Control FET
  - Rds(on) no longer dominates power loss in the Sync FET
- Improvements in efficiency require all sources of power loss are improved
  - This is the driving force behind the development of integrated powertrains.

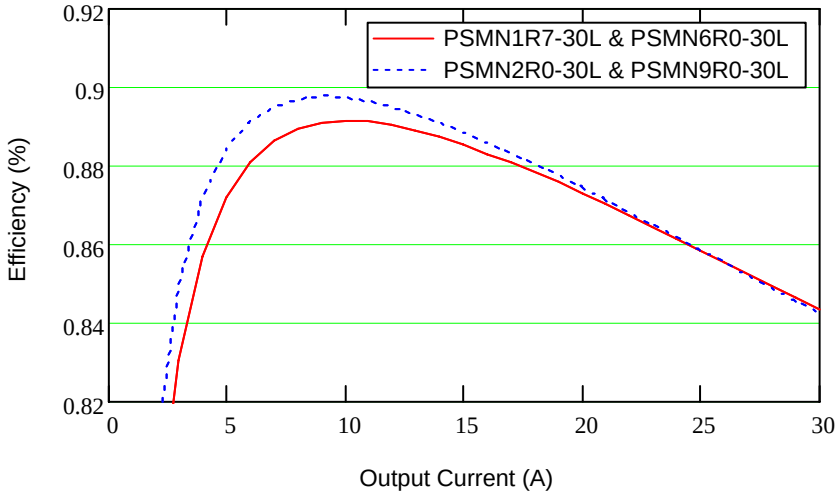




Design Choices: Die Size



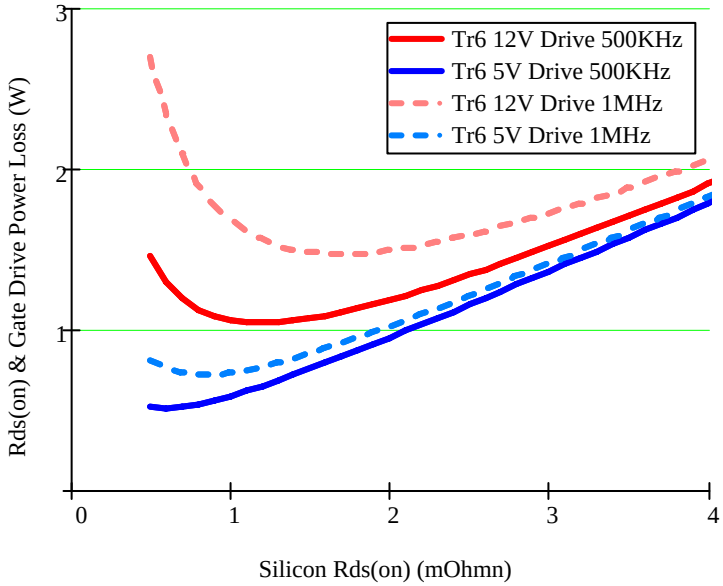
- Die Size Choice is a compromise
  - Cost / Performance
  - Low Load vs. High Load efficiency
  - Varying Customer Requirements
    - Iout, Freq, etc.



- High Load vs. Low Load
  - LFPak (using online SIMport[14])
  - FETs chosen for lowest loss at 30A & 20A, 500KHz are compared
- Optimising FETs at full load is expensive and wasteful
  - Only if thermals are limiting factor

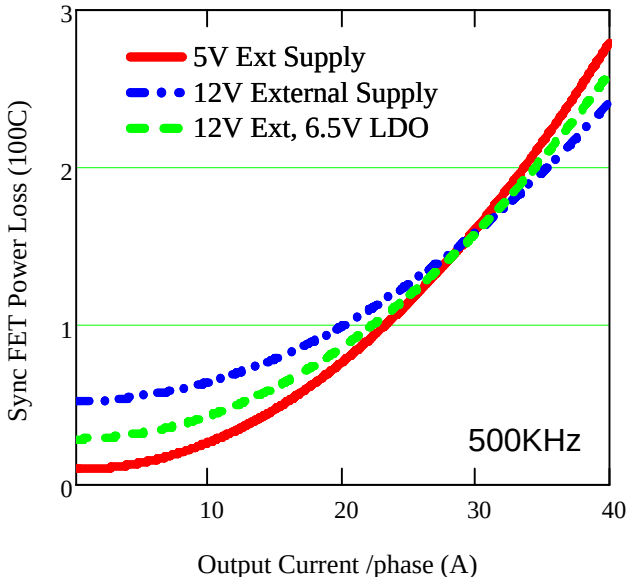
[15] SIMport is a complex formula MOSFET selection tool, that also allows efficiency comparisons over the whole current range to be performed. Typically optimising FETs at 2/3 maximum current tends to give good low and high load optimisation, http://www.nxp.com/models

Design Choices: Gate Drive Voltage



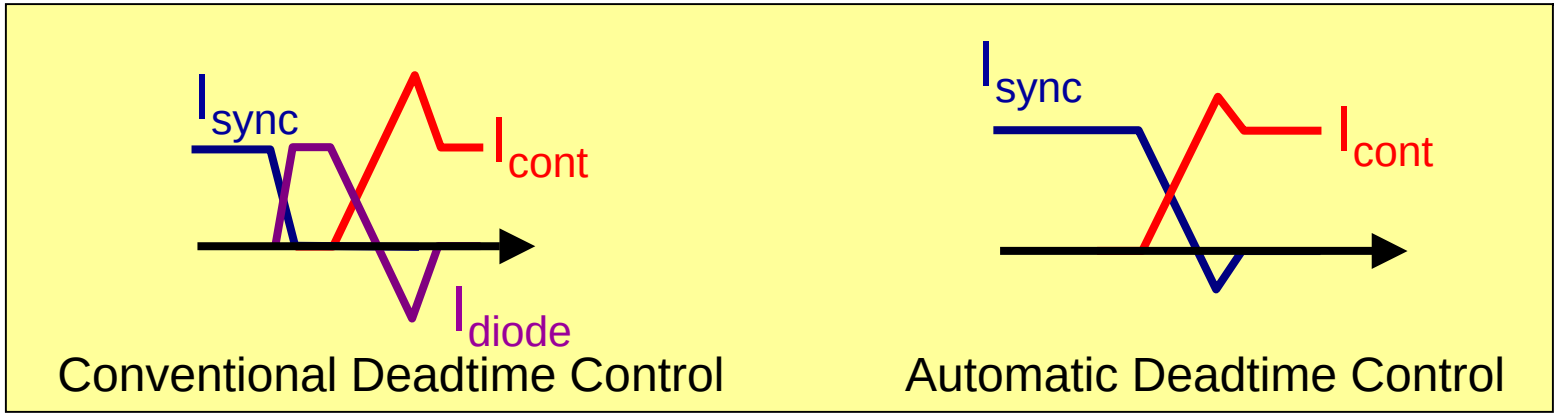
- 5V drive for Sync FET is optimum
  - Especially @ 1MHz
  - Not always available e.g. modules

- Include LDO to reduce gate drive losses where 5V not available
  - Optimum gate drive is load and frequency dependent
  - In PIP212 6.5V chosen

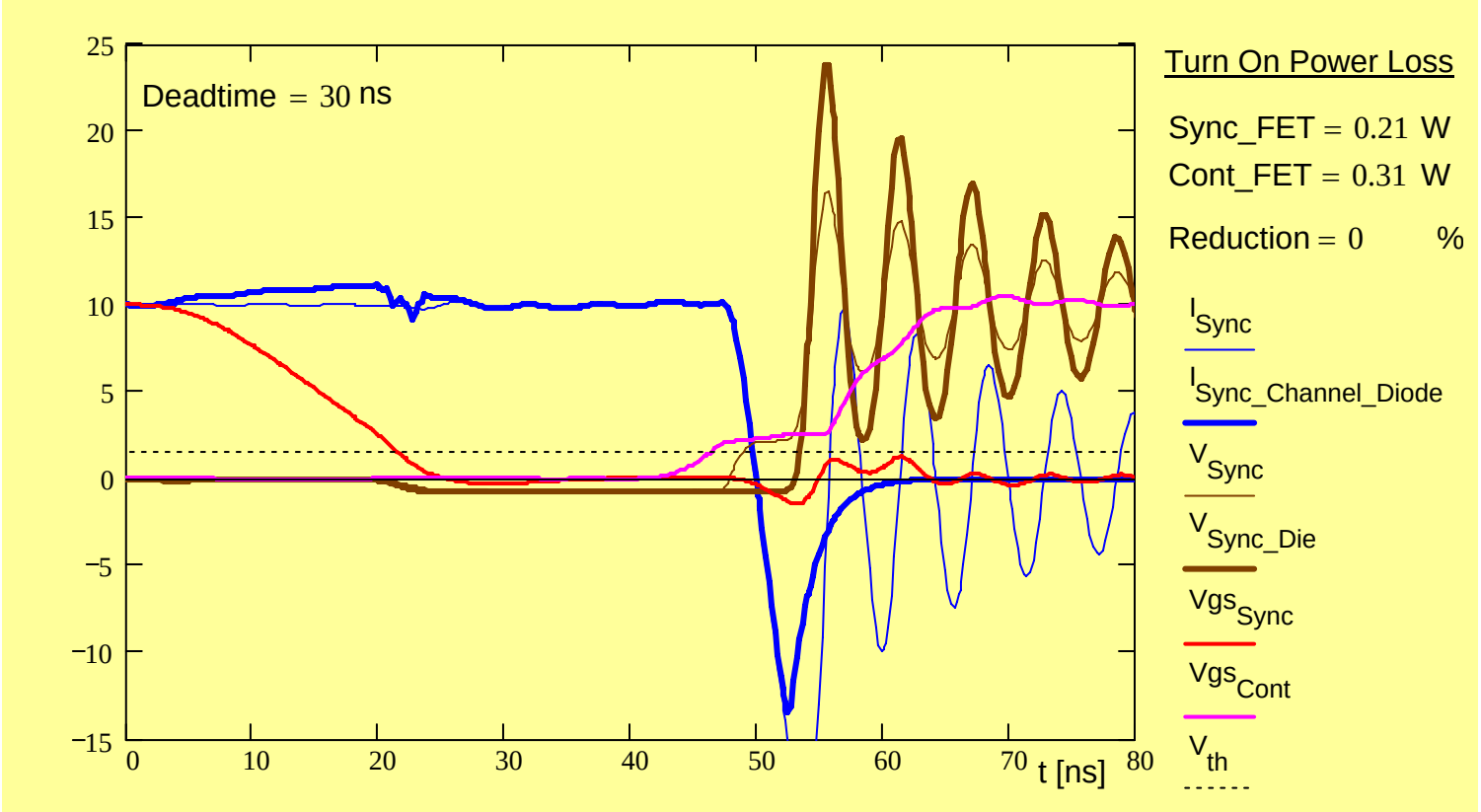


Further Efficiency Improvements

- Physical closeness of MOSFET & Driver allows for additional efficiency and system enhancing features
  - Adding intelligence in the way power switches are used is key benefit of integration (often neglected as di/dt increase is usual focus)
- Example: Automatic Deadtime Reduction
  - Driver can directly sense the Sync FET die and reduce internal timing on cycle by cycle basis until no diode conduction occurs
    - Clean sense signal as source inductance spikes not measured

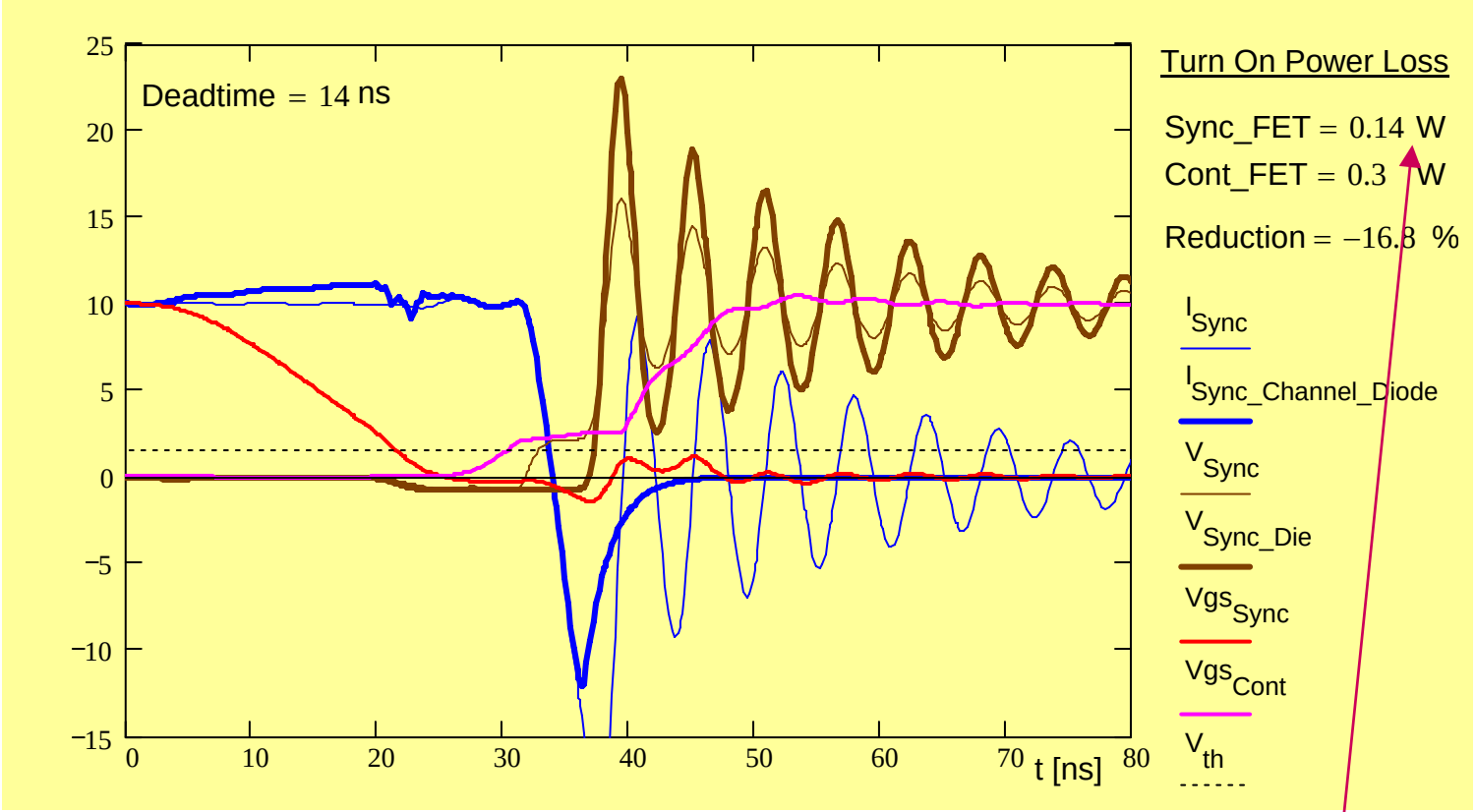


Automatic Deadtime Reduction - Concept



Traditional solution with 30ns deadtime (diode conduction)

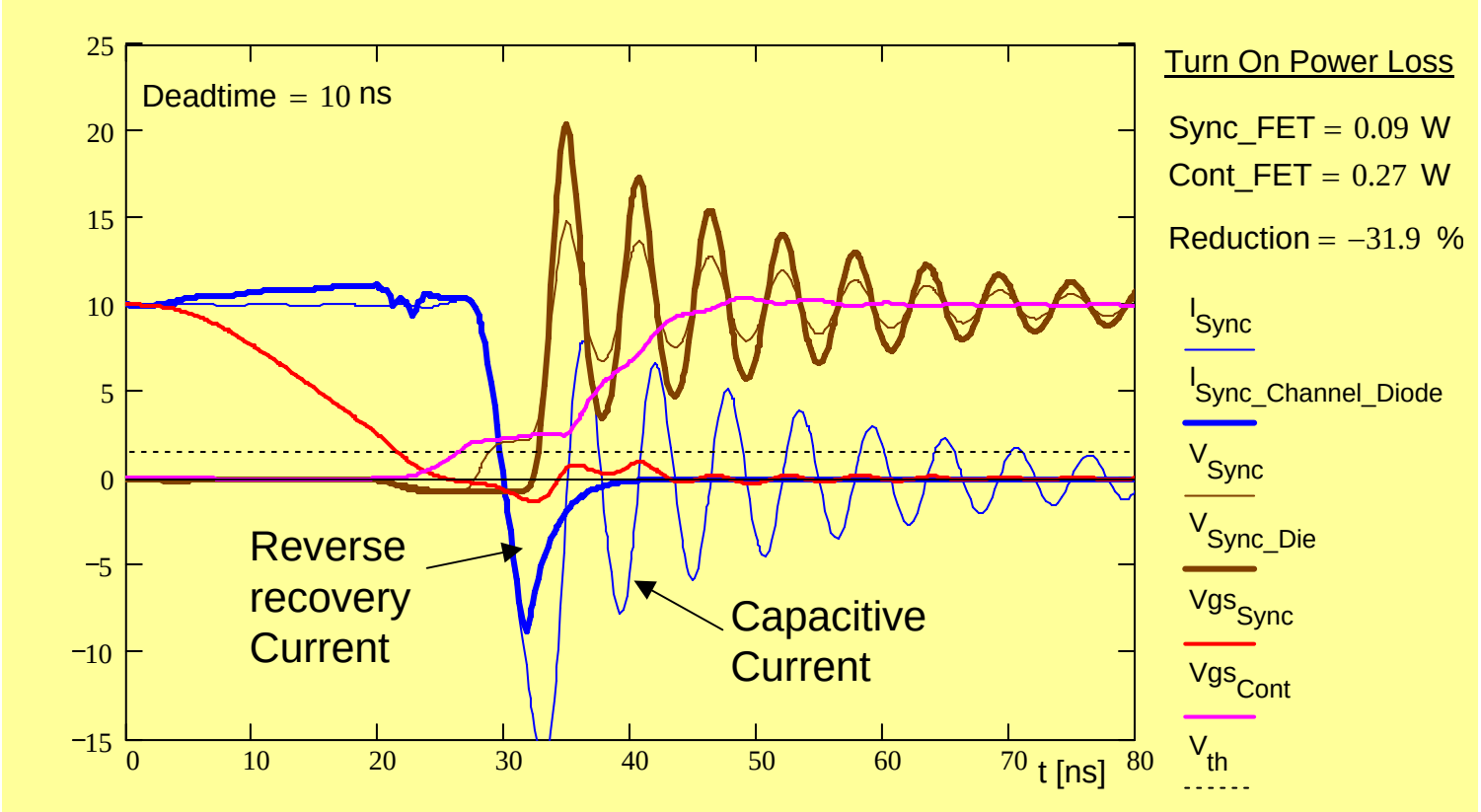
Automatic Deadtime Reduction - Concept



Sync FET losses slowly reduce as deadtime narrows

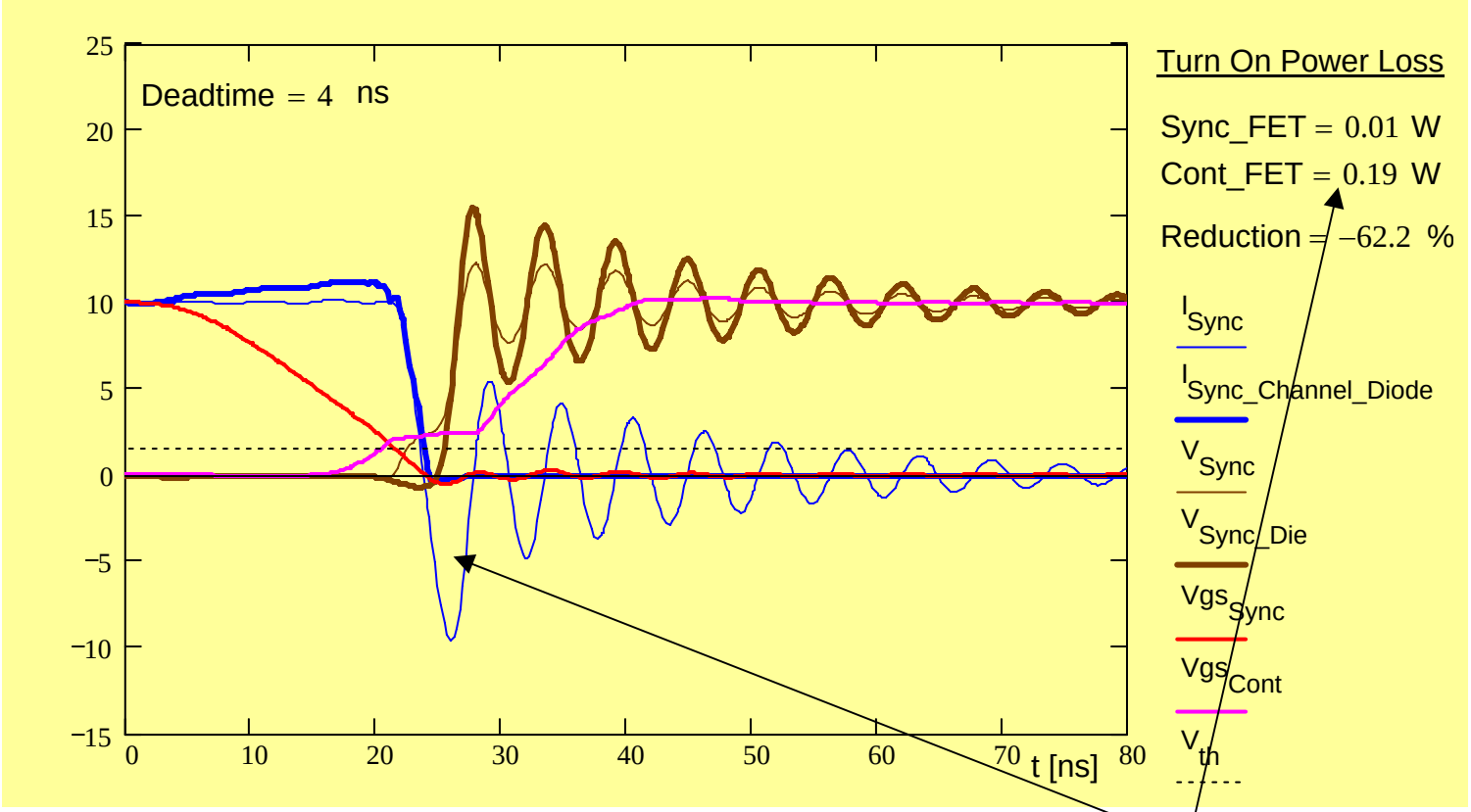
Note: Deadtime scheme can (is) be done discretely but package source inductances prevents optimum deadtime being achieved

Automatic Deadtime Reduction - Concept



Positive Sync FET Vgs during deadtime reduces reverse recovery current and voltage overshoot

Automatic Deadtime Reduction - Concept

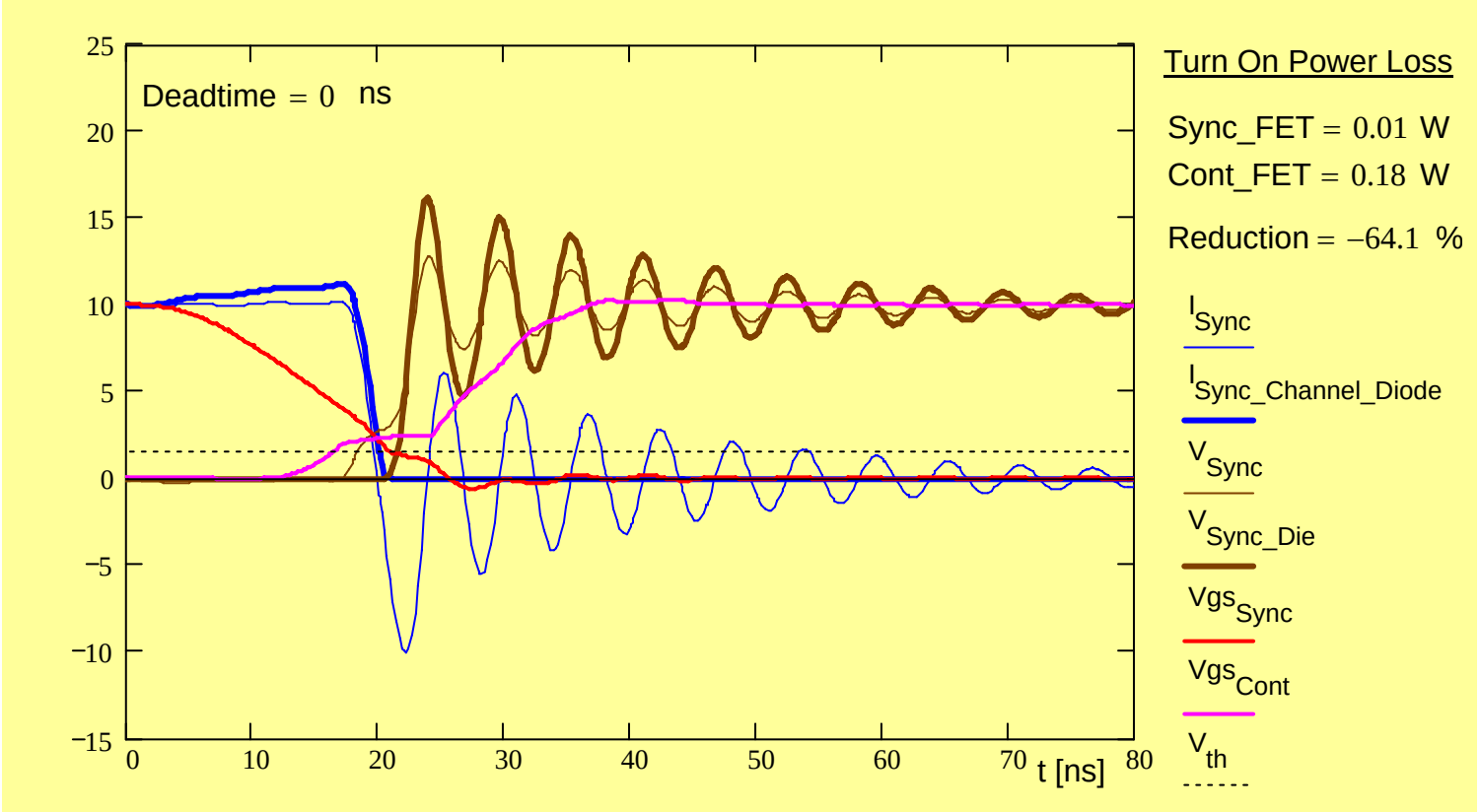


At 4ns deadtime reverse recovery eliminated

⇒ Subthreshold current effect in ultra high density TrenchMOS

[16] Reverse Recovery in High Density Trench MOSFETs with Regard to the Body-Effect, Toni López, Reinhold Elferich & Nick Koper

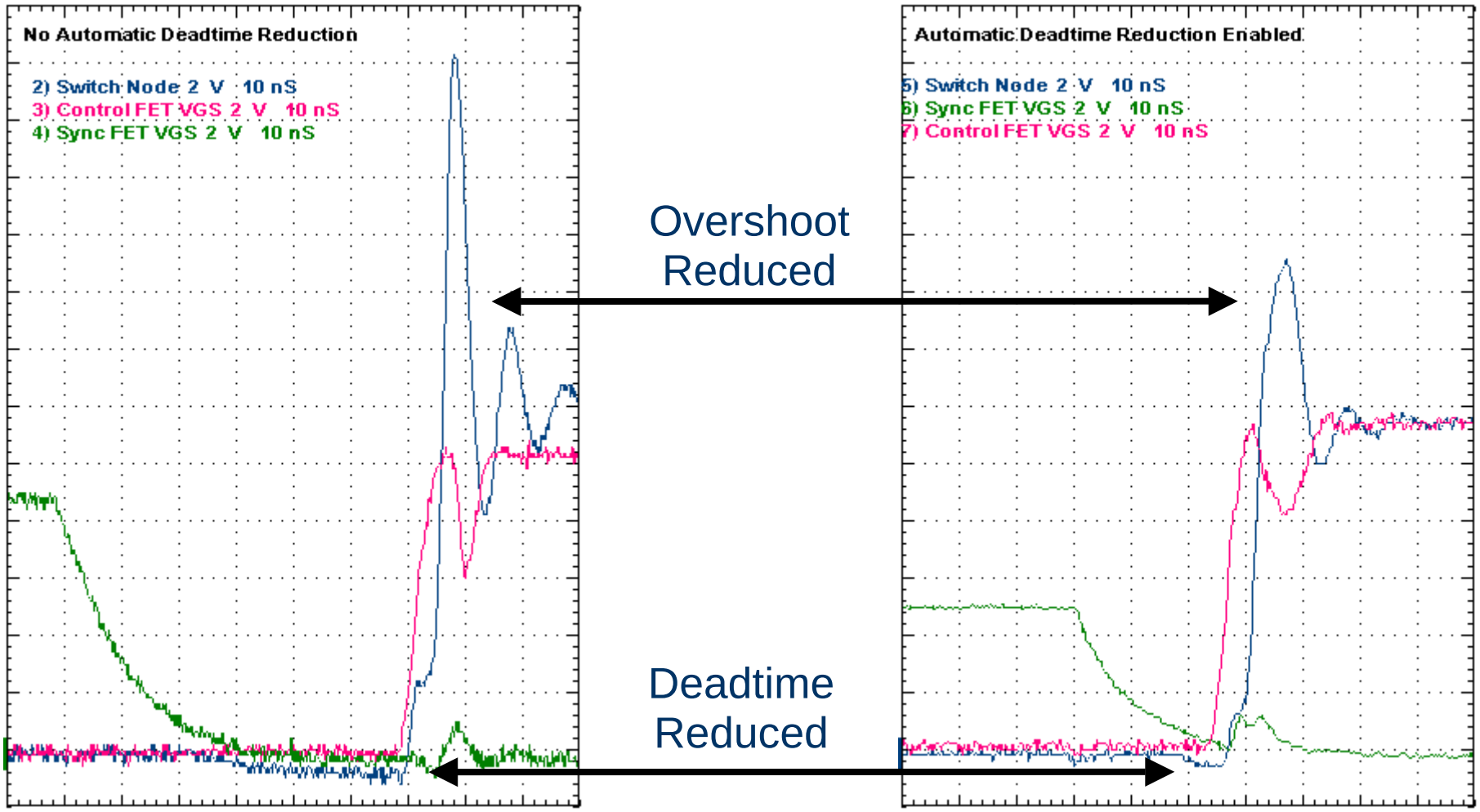
Automatic Deadtime Reduction - Concept



Ideal situation, no diode current

⇒ but just 10mW improvement over 4nS deadtime

Deadtime Reduction - Implemented

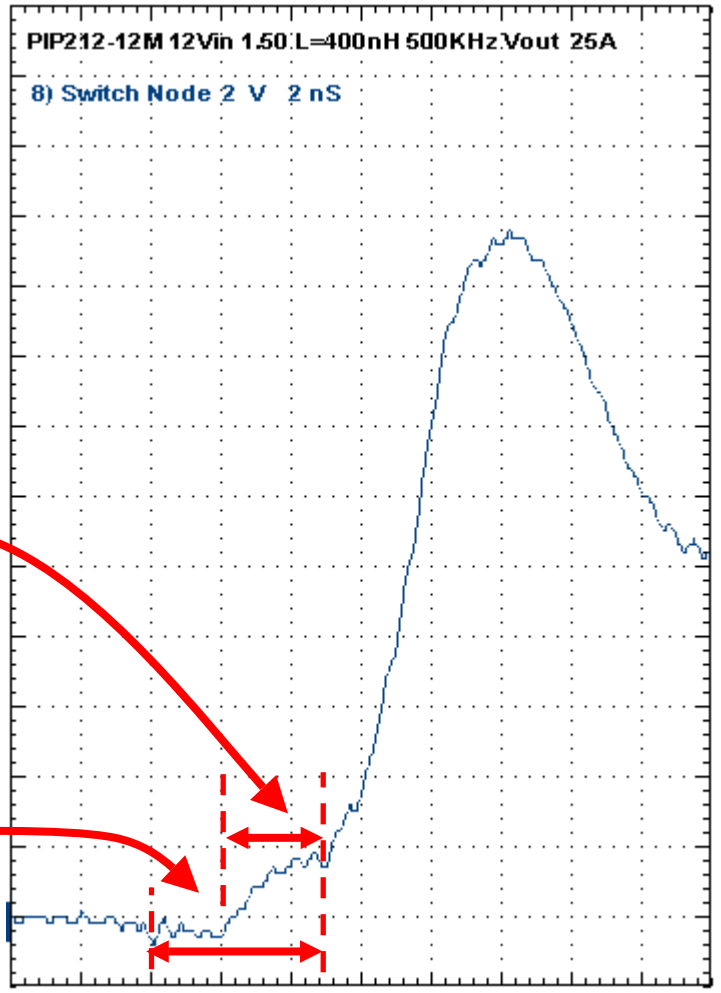


Performance Improvement

- Benefits of Integrated Powertrain approach is to produce approximately a doubling of switching frequency for same silicon technology
  - Or approx ≈3% efficiency increase

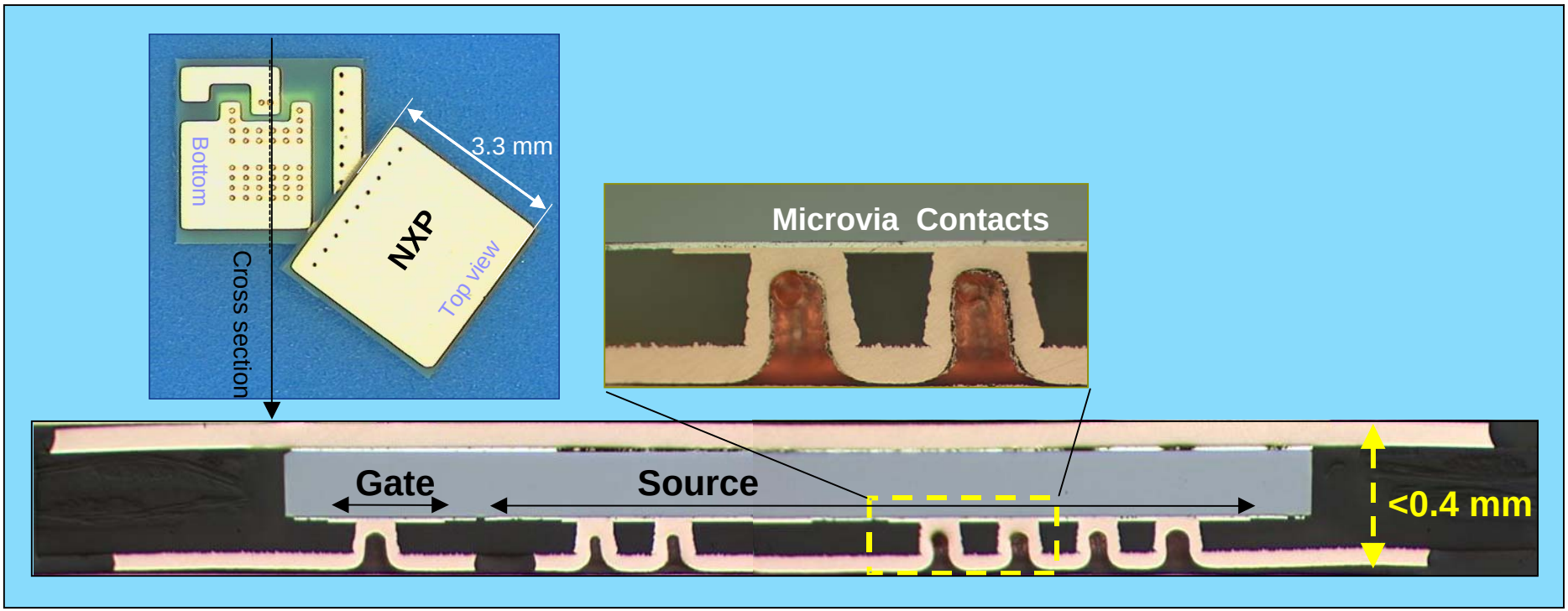
- di/dt
  - di/dt = 7A/ns
  - 7x faster di/dt than DPak
  - 2x faster than di/dt LFPak (Power SO8)

- Deadtime
  - Steady State deadtime only 5ns
  - Diode Losses (deadtime & reverse recovery significantly reduced)



Advanced Powertrain Packaging

- As die sizes shrink HVQFN is poor choice
  - Die:Footprint ratio becomes inefficient
    - Isolation gaps, space for pins etc
  - Embedded technology has potential for creating very low inductance integrated powertrains



[17] Development of Flex-based Embedded Actives Packages, Ronnie Chin, Tien Siang Chia, Kebao Wan, Thai Houng Tiong & Wil Peels, ECWC11
[18] Embedded Die Technology, Next Generation Packaging for Discrete Semiconductors, Wil Peels, David Heyes, Martien Kengen, Semicon Europa 2008

Conclusion

- Over the last 10 years Power MOSFET technology has improved tremendously (≈90% in Rds(on) and Rds(on)*Qgd)

- For 12V Conversion Vertical MOSFETs are optimum technology choice
  - If conversion voltage <5V then Lateral structures become viable, especially for output currents <10A

- Placing Driver and MOSFETs physically close in a single package offers significant performance advantages
  - Faster switching of the current (di/dt increased by a factor of 2)
  - Small overall footprint (half footprint of discrete alternative)
  - Ability to introduce power saving functionality (e.g. automatic deadtime reduction)

- Future Powertrain development aims at reducing total loop inductance
  - Additional efficiency enhancing and ease of use features

Thank-you

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