What About Switched Capacitor Converters?

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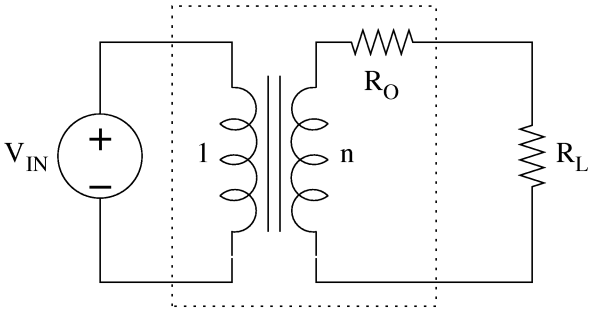
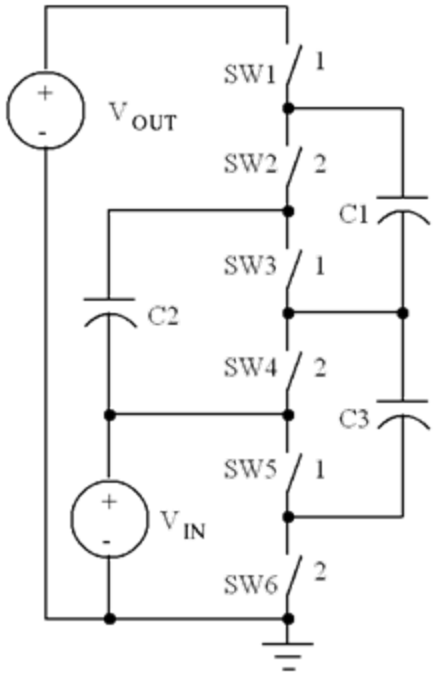
Switched Capacitor Power Converters

- Only switches and capacitors
- Simple low freq model as an ideal transformer with Thevenin impedance
  - neglects freq dependent loss and leakage
  - Would model leakage, dynamic losses with shunt imped.
- Using no inductors has advantages:
  - Simplified full integration potential
  - Works well over a wide power range
    - Single mode, can adjust clock rate
    - No minimum load
  - No inductive switching losses
- Open-loop loadline regulation:
  - Output impedance has R-C characteristic, with R naturally designed to meet efficiency spec

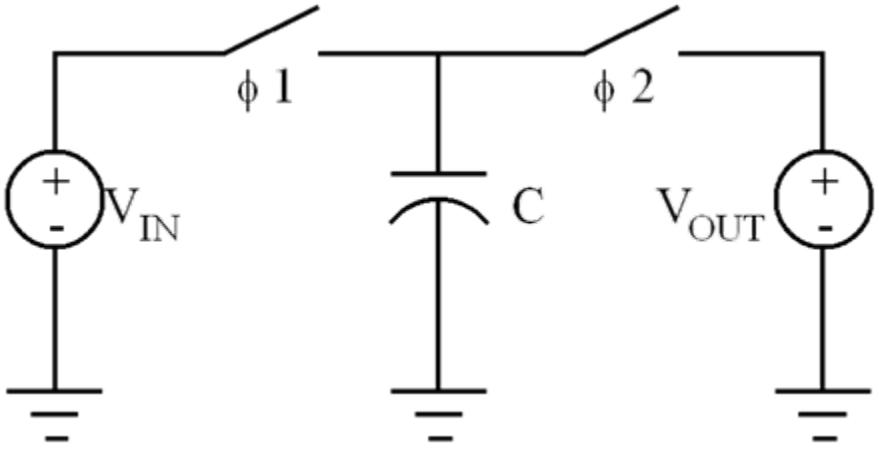


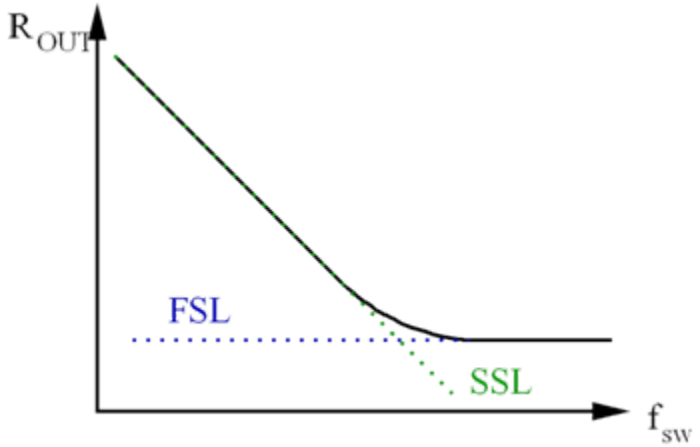


Why Not S-C ?

- Difficult regulation?
- Not suited for high current/power?
- Lots of difficult gate drive details?
- Interconnect difficulty for many caps?
- Voltage rating of CMOS processes?
- Magnetic-based ckts = higher performance?

SC Analysis: Simplest Example





- Slow Switching Limit (SSL):
  - Impulsive currents (charge transfers)
  - Resistance negligible (assume R = 0)
  - This (SSL) impedance is the switching loss!
- Fast Switching Limit (FSL):
  - Constant current through switches
  - Model capacitors as voltage sources (C → ∞)

$$i = f_{sw}\Delta q = f_{sw}C\Delta v$$

$$i = \frac{1}{4}\frac{1}{R}\Delta v$$

$$(\Delta v = V_{IN} - V_{OUT})$$

Comparing Converters

Need a metric to compare converters of different types!

Example: How much power can we get out of a converter with 10% voltage drop?

$$P_{OUT} = I_{OUT} V_{OUT} = (0.1 G_{OUT} V_{OUT}) V_{OUT} = 0.1 \cdot G_{OUT} V_{OUT}^2$$

Power performance related to GV^2

We can make a unitless performance metric by comparing converter GV^2 to component GV^2

SSL Metric:

$$\frac{G_{OUT} V_{OUT}^2}{f \sum_{caps} C_i v_{c,i(rated)}^2}$$

FSL Metric:

$$\frac{G_{OUT} V_{OUT}^2}{\sum_{switches} G_i v_{r,i(rated)}^2}$$

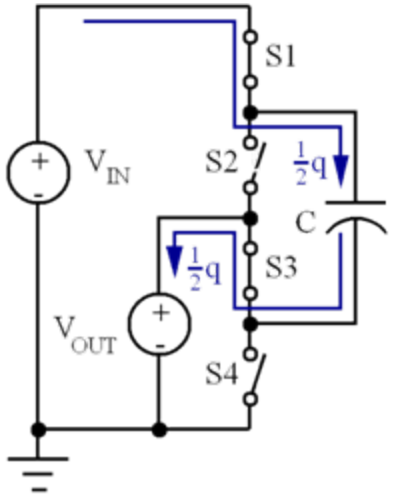
Analysis via Charge Multipliers

Capacitor Charge Multiplier:

$$a_{c,i}^{j} = \frac{\text{charge flow in cap } i\text{, phase } j}{\text{output charge flow, both phases}}$$

Switch Charge Multiplier:

$$a_{r,i} = \frac{\text{charge flow in switch } i\text{, when on}}{\text{output charge flow, both phases}}$$

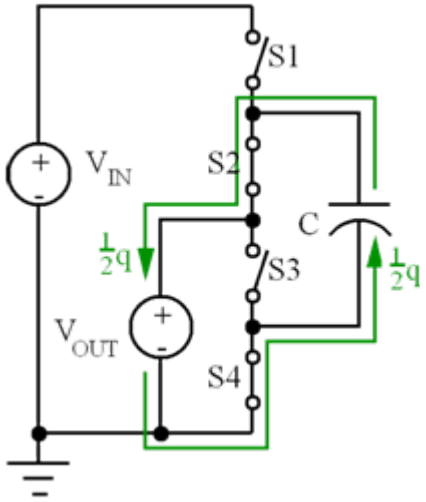


Phase 1:

$a_c^1 = \frac{1}{2}$

$a_{r,1} = \frac{1}{2}$

$a_{r,3} = -\frac{1}{2}$



Phase 2:

$a_c^2 = -\frac{1}{2}$

$a_{r,2} = \frac{1}{2}$

$a_{r,4} = -\frac{1}{2}$

Output Impedance ~ Power Loss

M. Seeman, S. Sanders, IEEE T-PELS, March 2008

- An SC converter's power loss is the sum of component energy (power) losses:

$$P_{SSL} = f_{sw} \sum_{capacitors} \Delta q_i \Delta v_i = R_{SSL} i_{OUT}^2 \qquad P_{FSL} = \frac{1}{2} \sum_{switches} R_i \left(2 q_i f_{sw}\right)^2$$

- The converter's output impedance can be determined in terms of just the charge multiplier components:

$$R_{SSL} = \sum_{capacitors} \frac{(a_{c,i})^2}{C_i f_{sw}} \qquad R_{FSL} = 2 \sum_{switches} R_i (a_{r,i})^2$$

Output Impedance and Optimization

Tellegen's theorem and energy conservation used to find R_{OUT}:

SSL: $$R_{OUT} = \frac{1}{f_{sw}} \sum_{i \in capacitors} \frac{(a_{c,i}^1)^2}{C_i}$$

FSL: $$R_{OUT} = 2 \sum_{i \in switches} R_i (a_{r,i})^2$$

Minimize output impedance while keeping component cost constant:

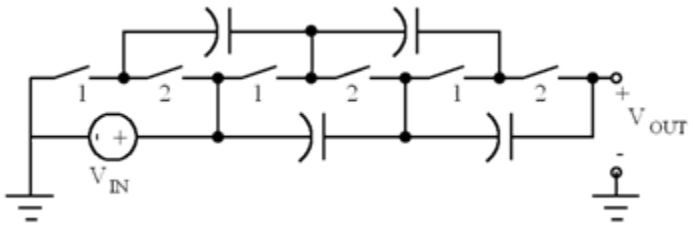
Cost constraint	**Optimized components**	**Optimized output impedance**
$E_{TOT} = \frac{1}{2} \sum_{capacitors} C_i v_{c,i(rated)}^2$	$\Longrightarrow \quad C_i^* \propto \left\| \frac{a_{c,i}}{v_{c,i(rated)}} \right\|$	$R_{SSL}^* = \frac{1}{2E_{TOT} f_{sw}} \left(\sum_{capacitors} \left| a_{c,i} v_{c,i(rated)} \right| \right)^2$
$A_{TOT} = \sum_{switches} G_i v_{r,i(rated)}^2$	$\Longrightarrow \quad G_i^* \propto \left\| \frac{a_{r,i}}{v_{r,i(rated)}} \right\|$	$R_{FSL}^* = \frac{2}{A_{TOT}} \left(\sum_{switches} \left| a_{r,i} v_{r,i(rated)} \right| \right)^2$

In the optimal case:

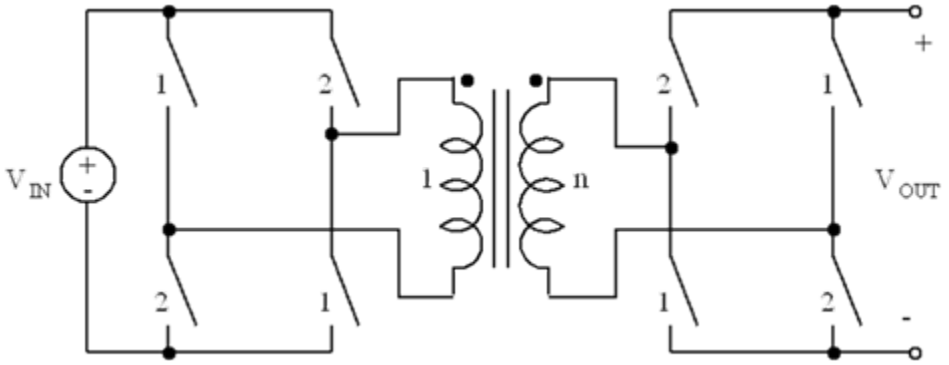
- Capacitor voltage ripple and switch voltage drop are proportional to rated voltage
- Output impedance proportional to the square of the *sum of the component V-A products*

Comparison with Magnetic Designs

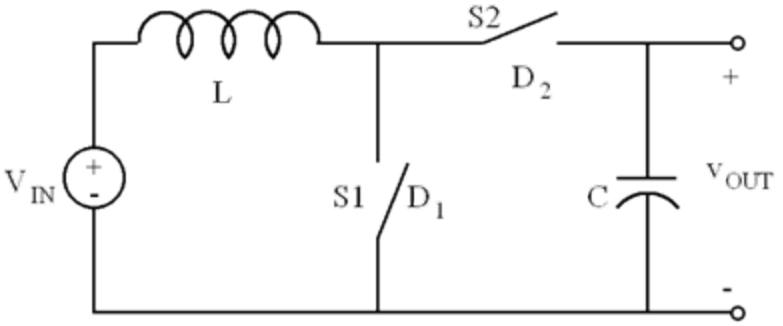
Ladder-type switched-cap converter



Transformer-bridge converter



Boost or Buck converter



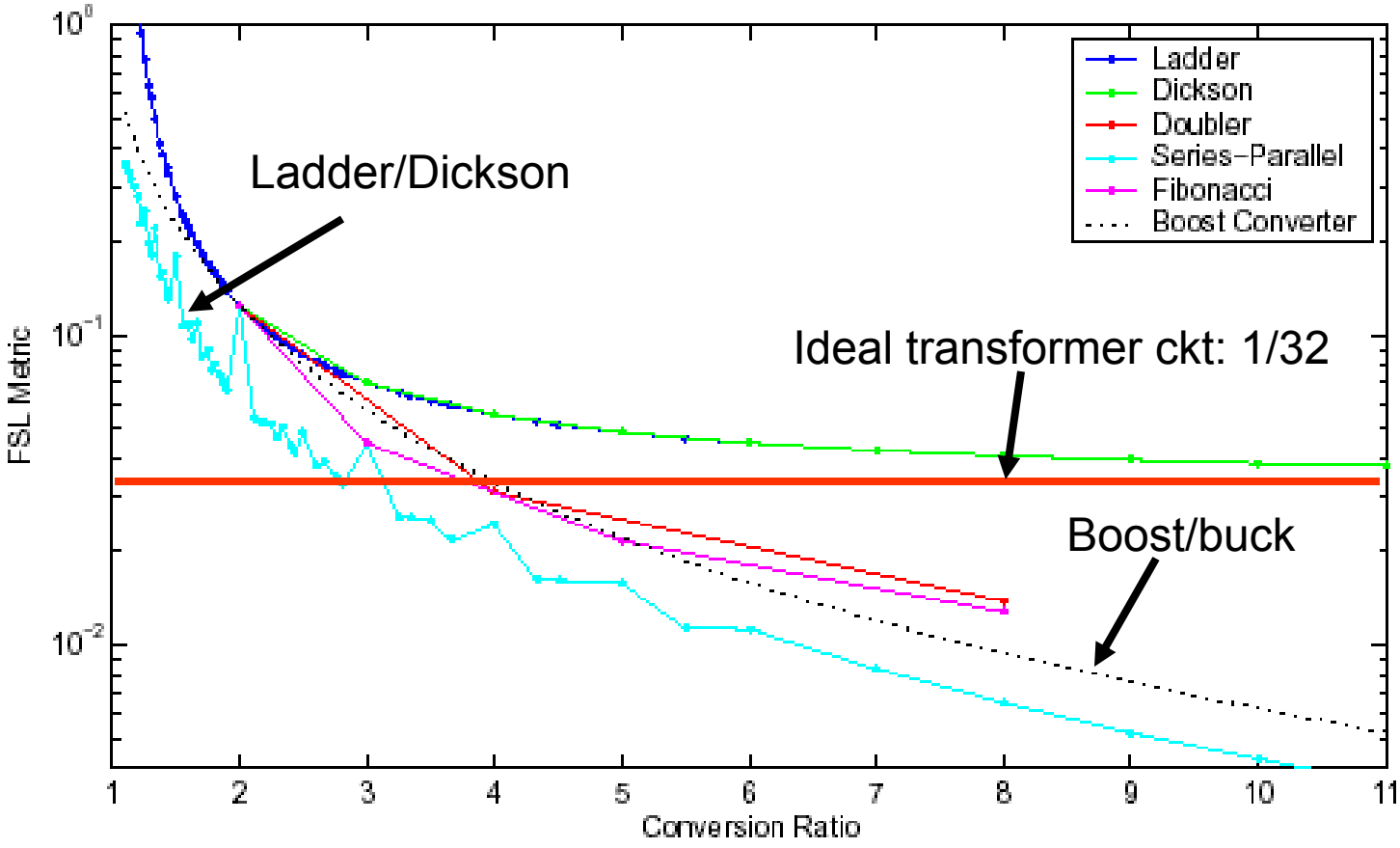
Switch sizes optimized for a given conversion ratio *n* for all converters

Switch Utilization – Conduction Loss Comparison

•Performance compared with switch GV2 metric:

$$\frac{G_{OUT}V_{OUT}^2}{\sum G_i v_{r,i(rated)}^2}$$

•Magnetic components modeled with *zero* conduction loss, and *no* switching loss impact



D.H. Wolaver, PhD dissertation,MIT,1969 proves fundamental thms on dc-dc conv.:

G = voltage or current gain

- Switches (*resistors*):

$$-\sum_{k\in dc-active}\bar{v}_k\bar{i}_k \geq \frac{G-1}{G}P_O \qquad -\sum_{k\in ac-active}\overline{(v_k-\bar{v}_k)\bullet(i_k-\bar{i}_k)} \geq \frac{G-1}{G}P_O$$

- *Ladder/Dickson are optimal*

- Reactive Elements:

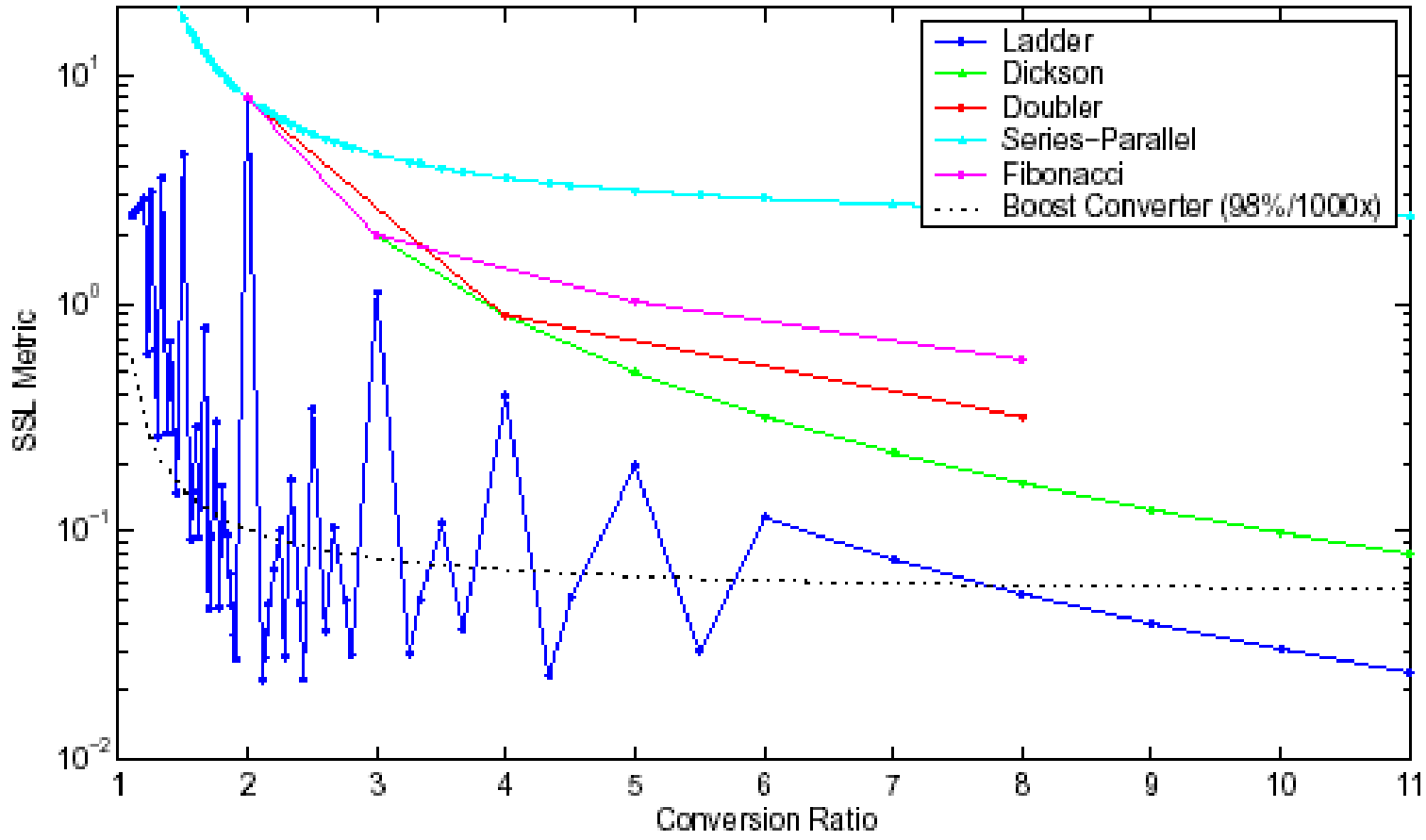
$$\frac{1}{2}\sum_{k\in reactive}\left|\overline{v_k i_k}\right| \geq \frac{G-1}{G}P_O$$

Meaning for 2-phase ckts:

$$\sum_{k\in C}V_k q_k + \sum_{k\in L}I_k\lambda_k \geq \frac{1}{f}\frac{G-1}{G}P_O$$

Utilization of Reactive Elements:

- For boost or buck, derate inductor by 1000x relative to cap due to practical energy density, assert that S-C examples exhibit 2% voltage drop relative to mag ckts



The Submicron Opportunity

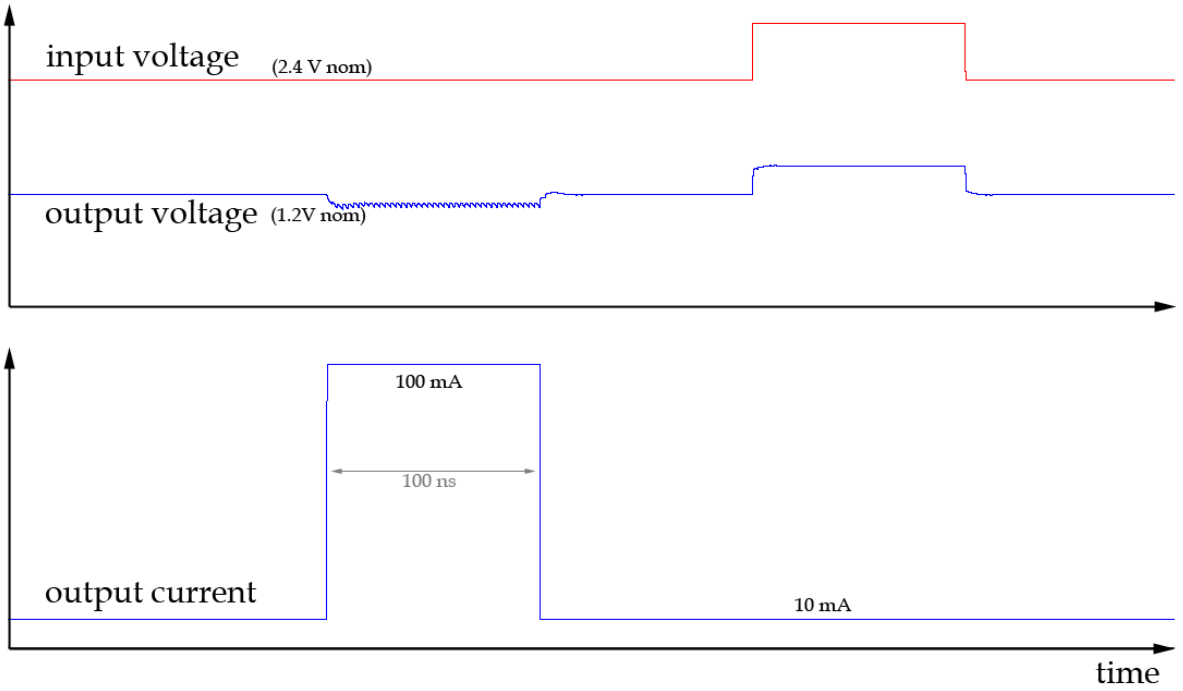
- Rate device by ratio: $G_s V_s^2 / C V_g^2$
  - Essentially an Ft type parameter for a power switch reflecting power gain, exposes opportunity in scaling
- Suggests that we should look for opportunities to build our ckts with scaled CMOS based devices, but:
  - Low voltage rating per device
  - Inadequate metal/interconnect for high current?

Regulation Considerations

- *Open-Loop* Loadline Regulation
  - Droop matching resistive output impedance effective for loadline VR type reg.

Dominant First Order Dynamics

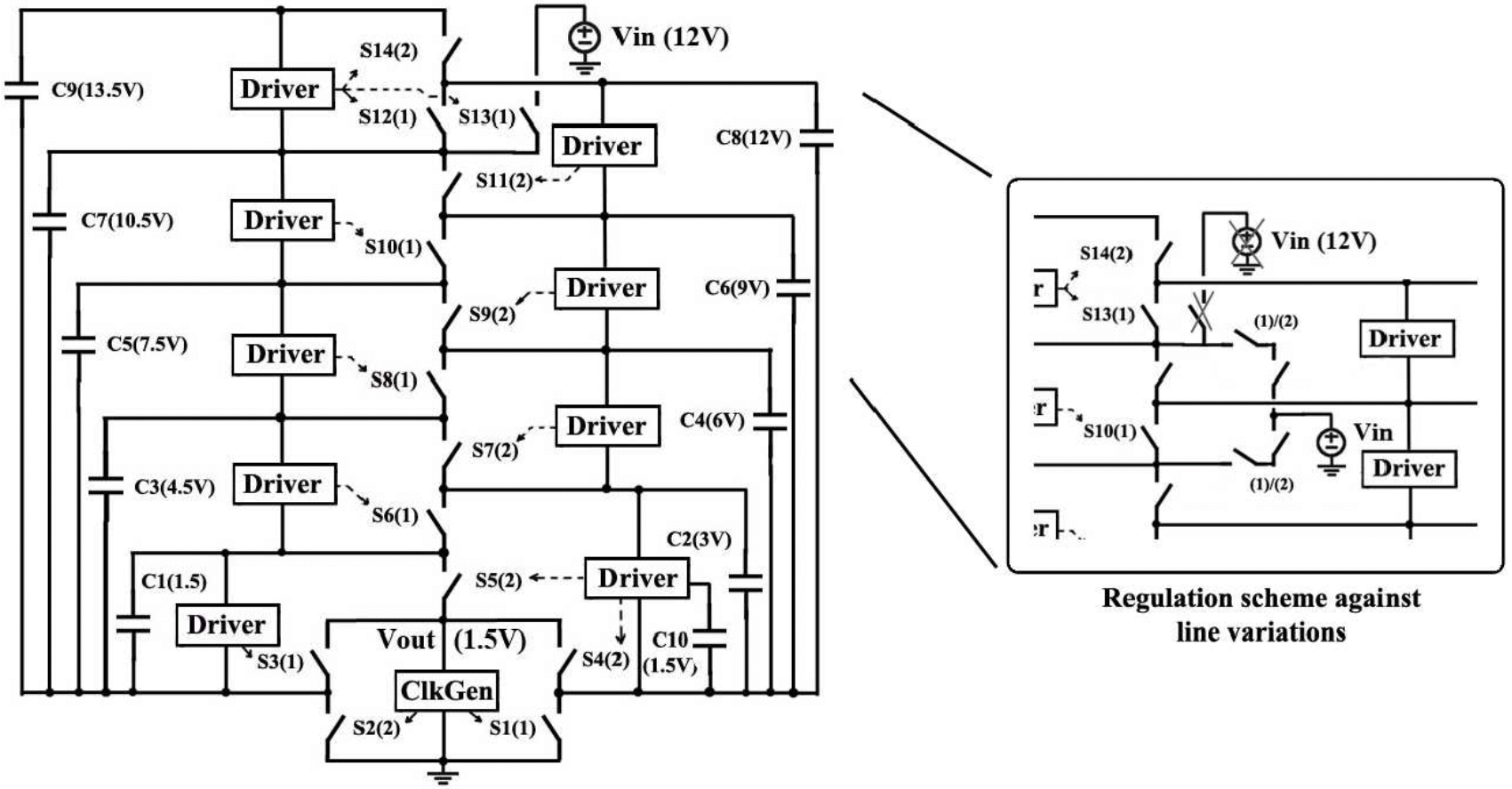
Simulation Example: 8-phase 2-to-1 converter



- Tap Changing for Line Regulation – Feedforward
- Multi-mode Operation for Apps like Voltage Scaling

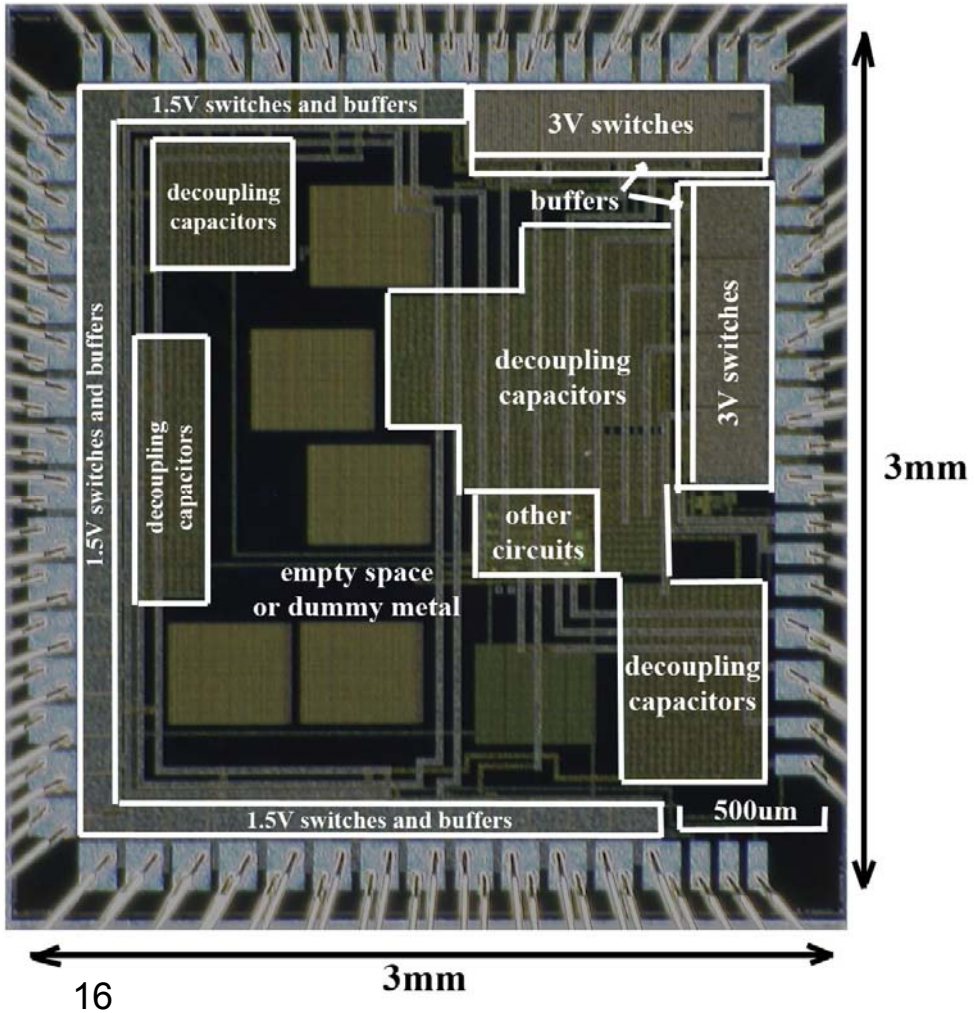
Example 1 – Point-of-Load:12V-to-1.5V Dickson Circuit

Illustrates “tap-changing” technique for line regulation.



V.W. Ng, **A 98% peak efficiency 1.5A 12V-to-1.5V Switched Capacitor dc-dc converter in 0.18 um CMOS technology**, Master Thesis Report, EECS Dept, UC Berkeley, Dec. 2007.

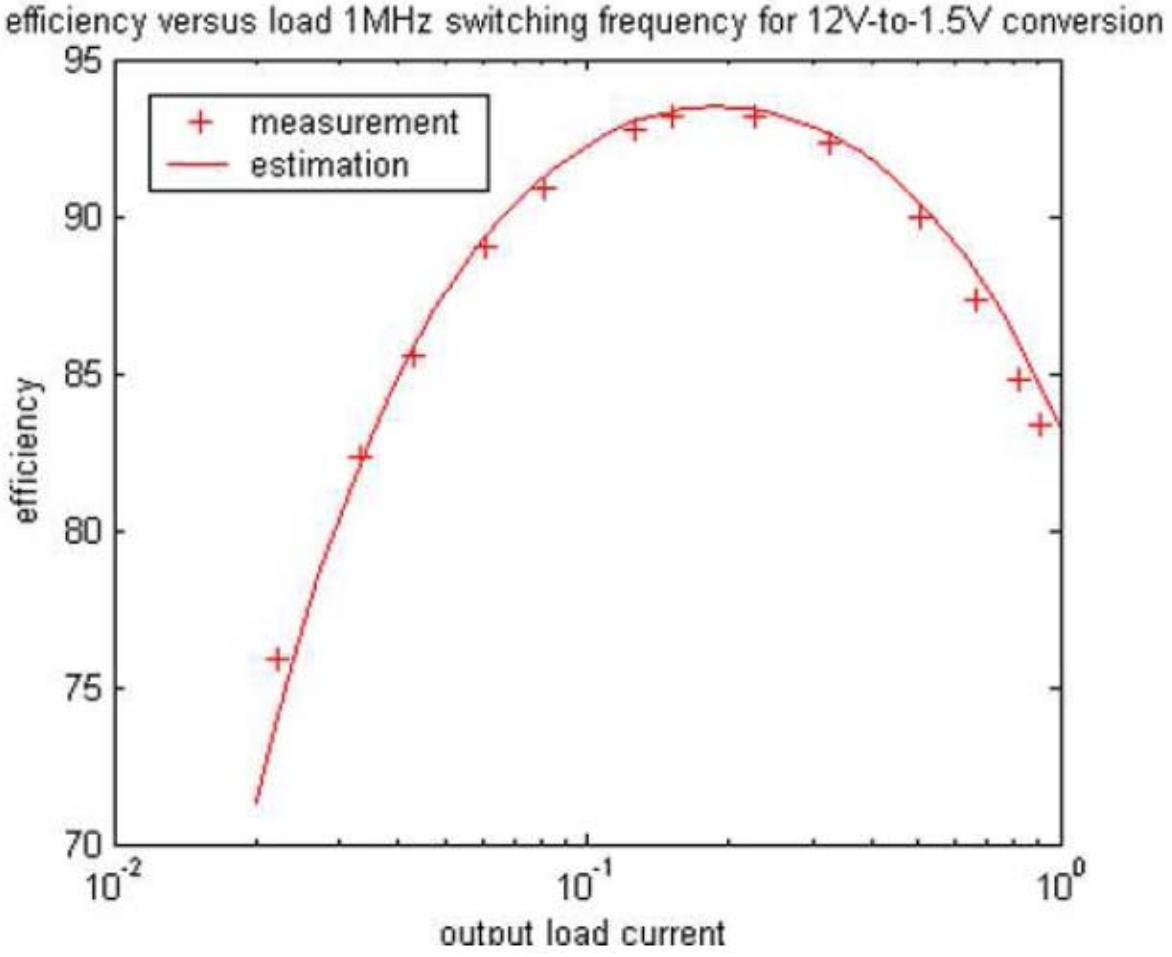
Layout in Triple-Well 0.18 um CMOS



AREA OF DIFFERENT COMPONENTS IN DIE LAYOUT

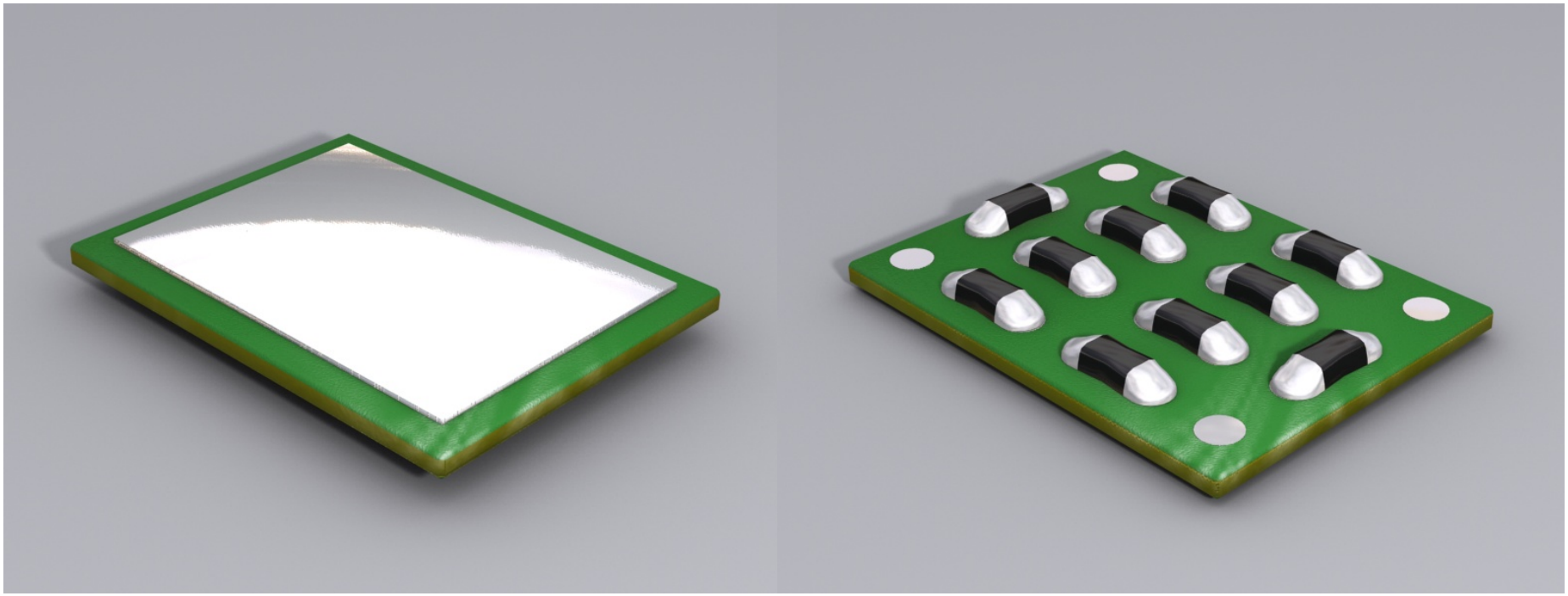
	area in layout
3V switches	$0.57mm^2$
3V switch buffers	$0.1mm^2$
1.5V switches	$0.5mm^2$
1.5V switch buffers	$0.06mm^2$
Other circuits	$0.13mm^2$
decoupling capacitors	$1.56mm^2$
Total active area	$\mathbf{3mm^2}$
Total area excluding pads	$6.7mm^2$
Total area including pads	$\mathbf{9mm^2}$

Design vs. Performance



1.5V cap	$2.2\mu F$
3V cap	$2.2\mu F$
4.5V cap	$1\mu F$
6V cap	$1\mu F$
7.5V cap	$0.68\mu F$
9V cap	$0.68\mu F$
10.5V cap	$0.47\mu F$
3V switch width	$16mm$
1.5V switch width	$75mm$
Contribution to conduction loss	
all switches	$51m\Omega$
onchip metal	$39m\Omega$
capacitor R_{ESR}	$15m\Omega$
bondwire resistance	$65m\Omega$
Fixed loss	1.3mW
Freq-dep switch loss	7mW
R_{OUT}@1MHz	**211mΩ**

POL Design 2: Flip Chip Packaging Scheme

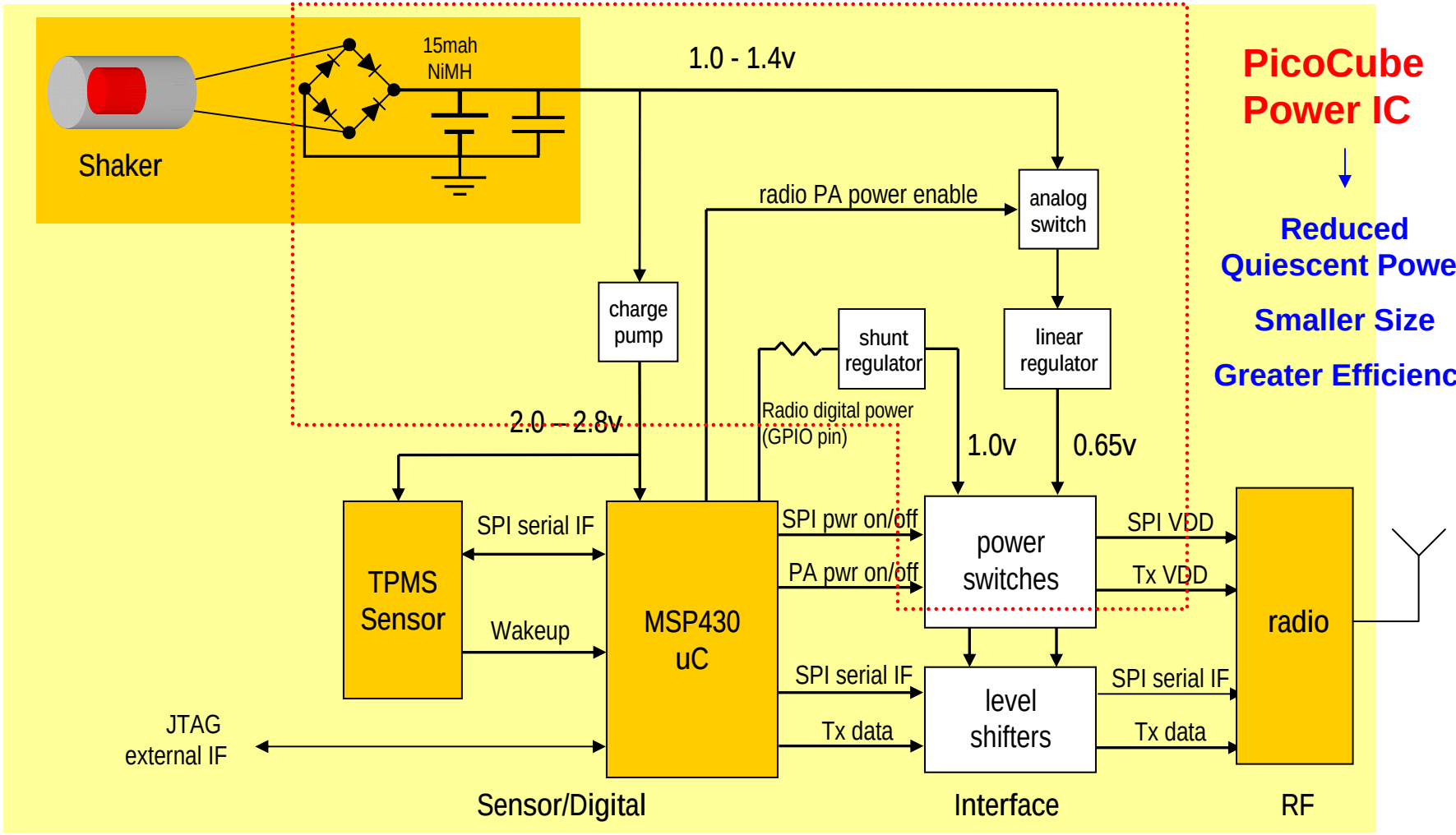


Cost and PCB Area Comparison

COMPARISON WITH OTHER WORKS IN INDUSTRY AND LITERATURE

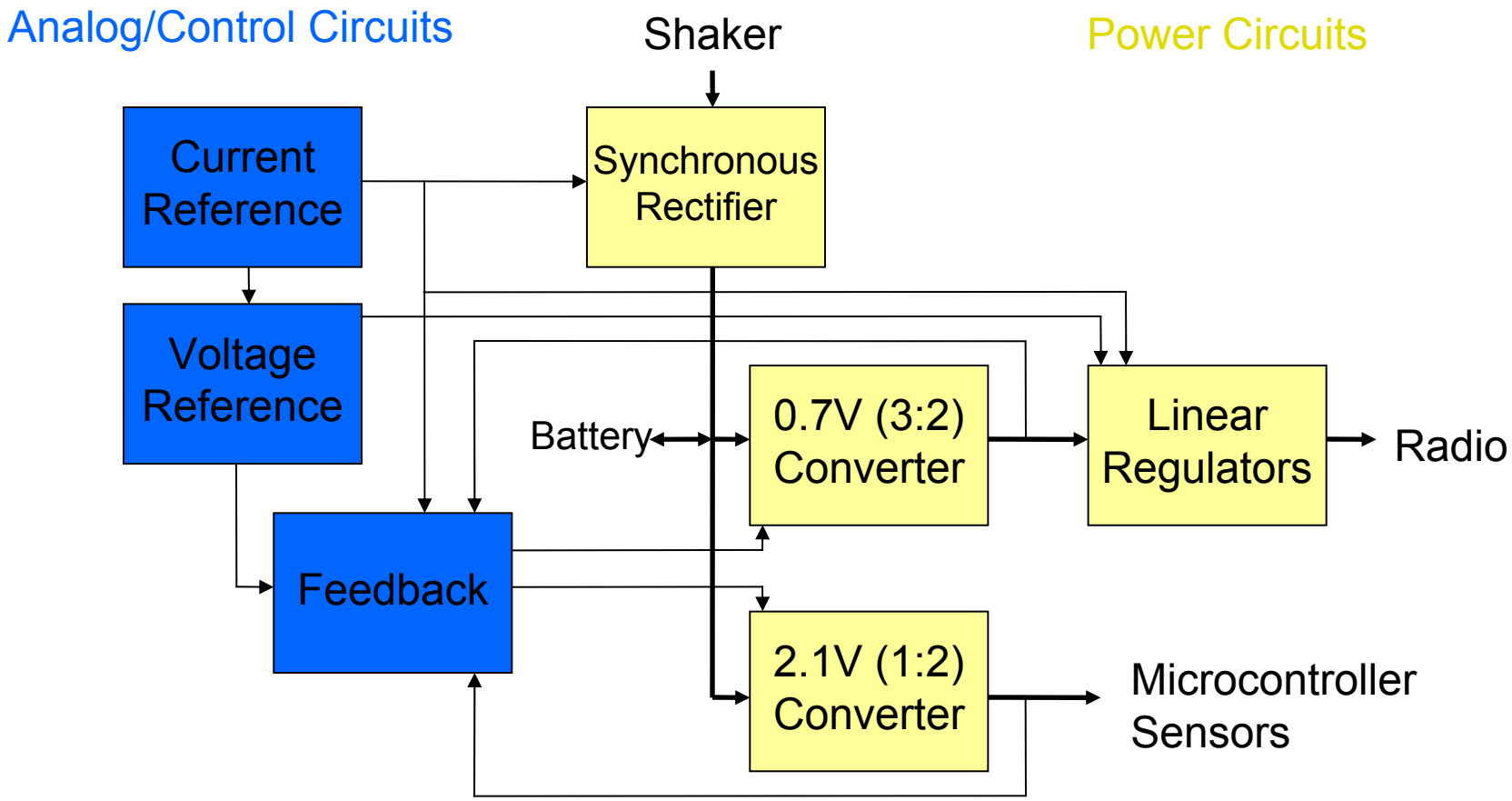
	input	output	peak eff	$> 80\%$ eff	switch area	dominant passive	PCB area	height	L,C cost
1-st design (this work)	12V	1.5V	93% at 200mA	25mA-1A	$1mm^2$	$\sim 1\mu$F caps x10	$13mm^2$	0.8mm	\$0.11
2-nd design (this work)	12V	1.5V	95% at 1 A	100mA-5A	$4mm^2$	$\sim 3\mu$F caps x 8	$11mm^2$	0.8mm	\$0.09
SC converter (TI, [6])	5V	1.5V	85%	2mA-200mA		$\sim 1\mu$F caps x 2	$3mm^2$	0.8mm	\$0.02
buck (National, [7])	12V	0.8V	75%	-		10μH inductor	$34mm^2$	2.8mm	\$0.47
buck (Linear, [9])	12V	3.3V	85%	0.1A-2A		4.7μH inductor	$36mm^2$	2mm	\$0.17
buck (Maxim, [8])	12V	3.3V	86%	3mA-1.5A		10μH inductor	$34mm^2$	2.8mm	\$0.47
buck (Literature, [5])	12V	1.3V	89%	1A-10A	$15mm^2$	2μH inductor	$156mm^2$	6.5mm	\$0.76

Ex. 2 - Ultra-low-power Conversion in PicoCube Wireless Sensor Node



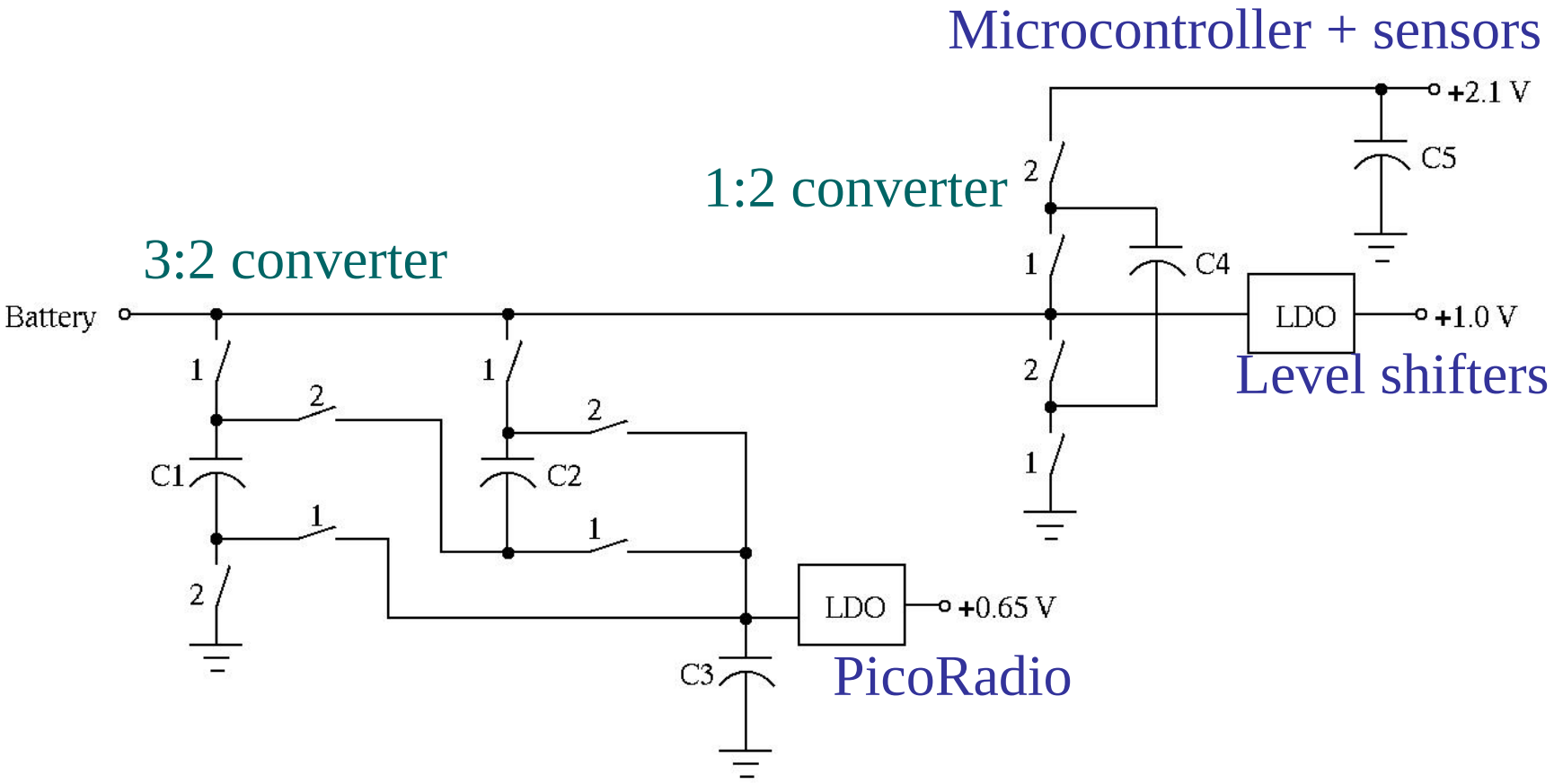
PicoCube: A 1cm3 Sensor Node Powered by Harvested Energy, 2008 DAC/ISSCC Student Design Contest

PicoCube Power Management Chip Block Diagram



Seeman, Sanders, Rabaey, "An Ultra-Low-Power Power Management IC for Wireless Sensor Nodes," *CICC* 2007.

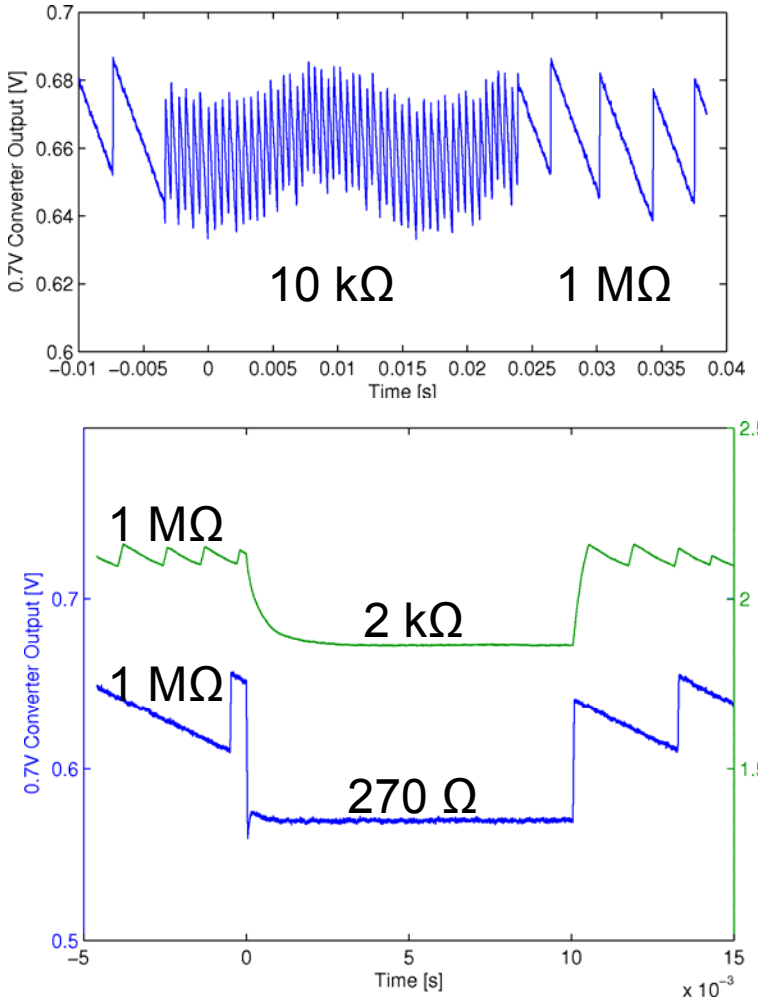
PicoCube Converter Topology



Linear Regulators (LDOs) further regulate and reduce ripple on outputs

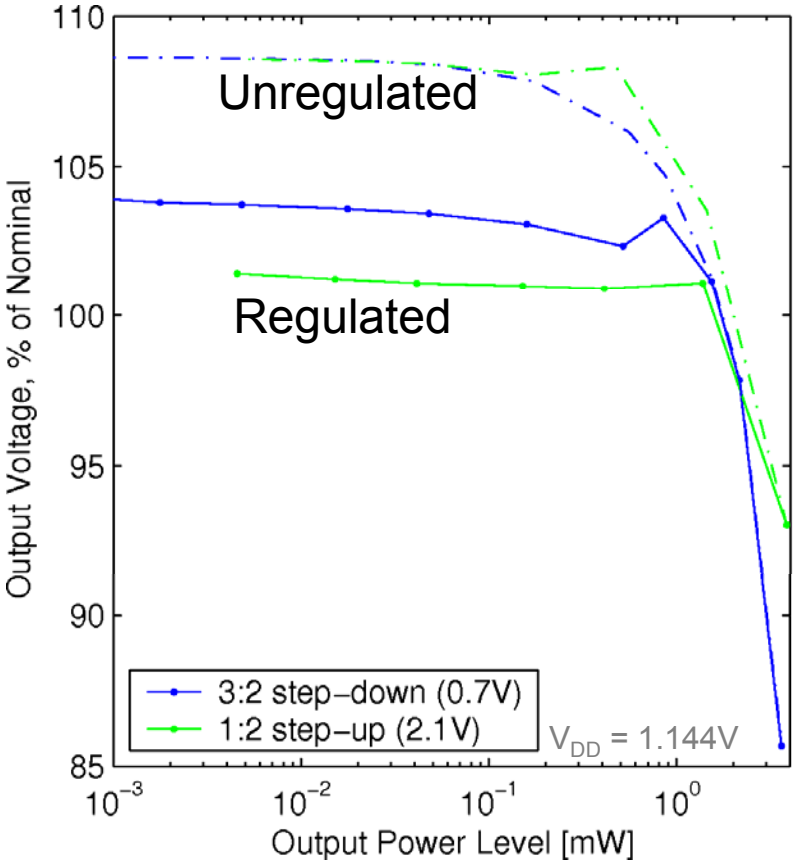
Hysteretic Feedback

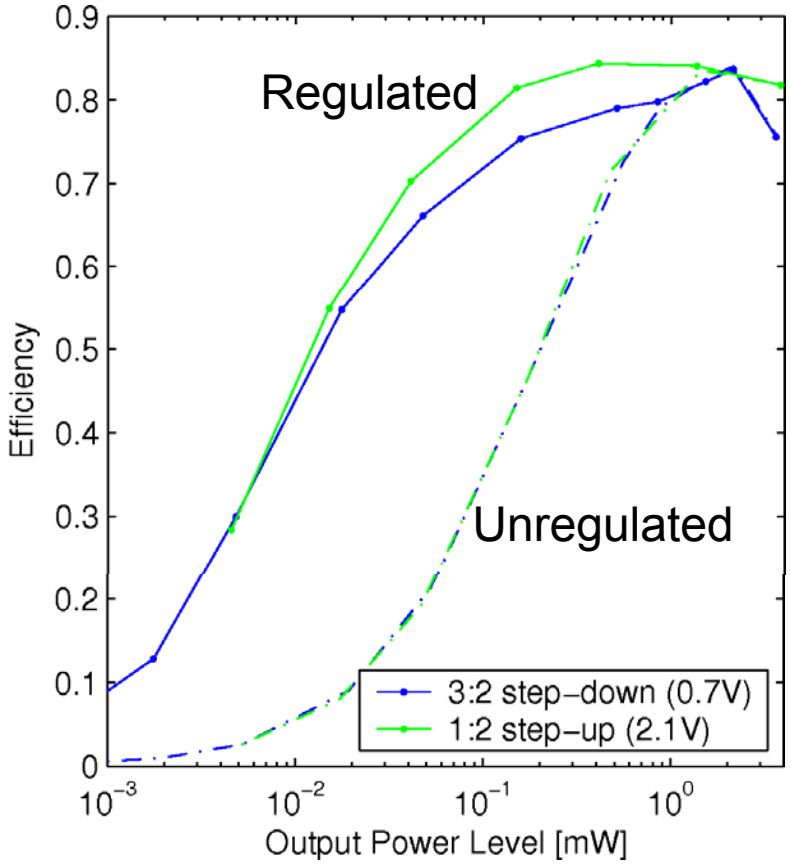
- Regulates output voltage
  - On/off clocking control
  - Thermostat-type control
  - Improves efficiency by reducing f_{sw} for small loads



Converter leaves regulation for only large loads

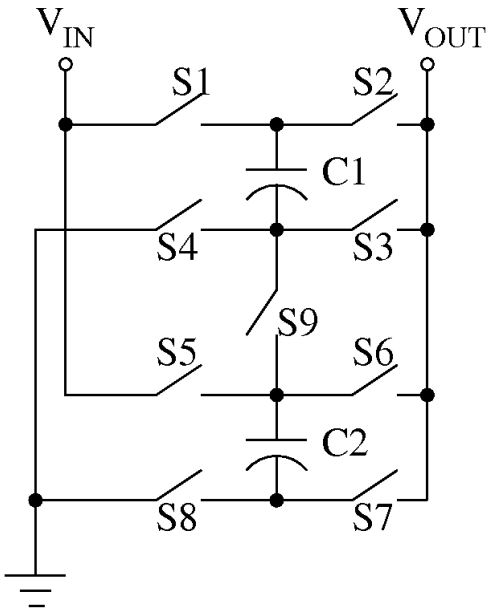
Converter Performance

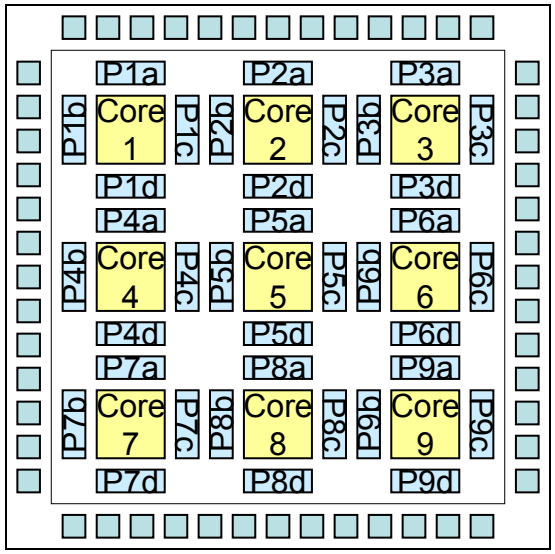


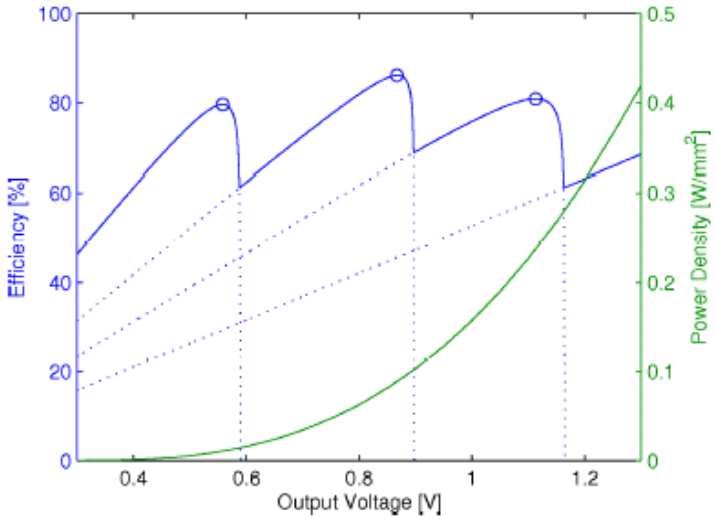


Regulation is effective at controlling output voltage and increasing efficiency at low power levels!

Ex. 3: Microprocessor SC Converter



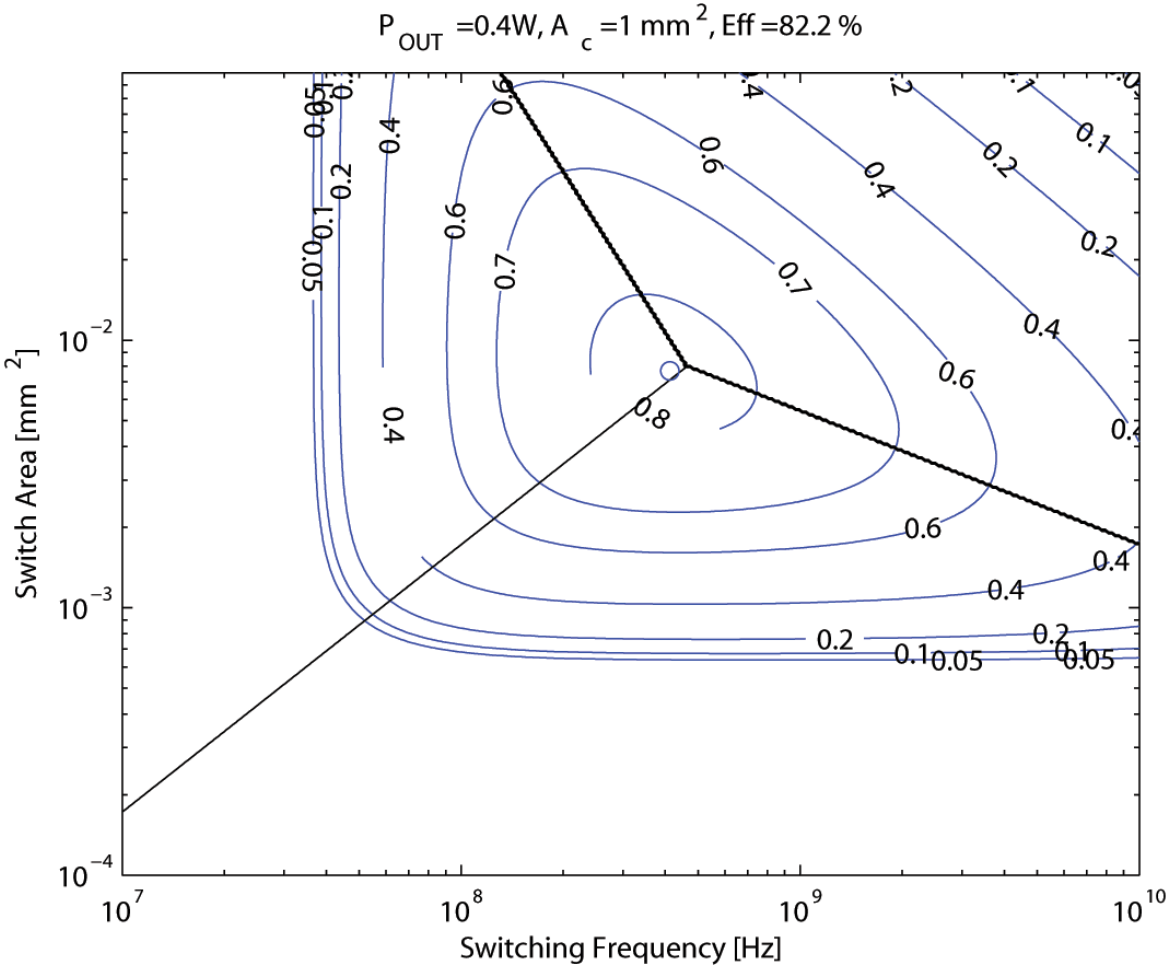




- A power density of 1 W/mm^2 is achievable in 65nm process.
- A tiled design improves output ripple and ESR performance
- Creates a scalable IP platform
- Ideal for microprocessor supplies:
  - Ultra-fast transient response
  - Package I/O at higher voltage/lower current
  - Independent core voltage control

Design Optimization Example: 0.4 W/sq.mm

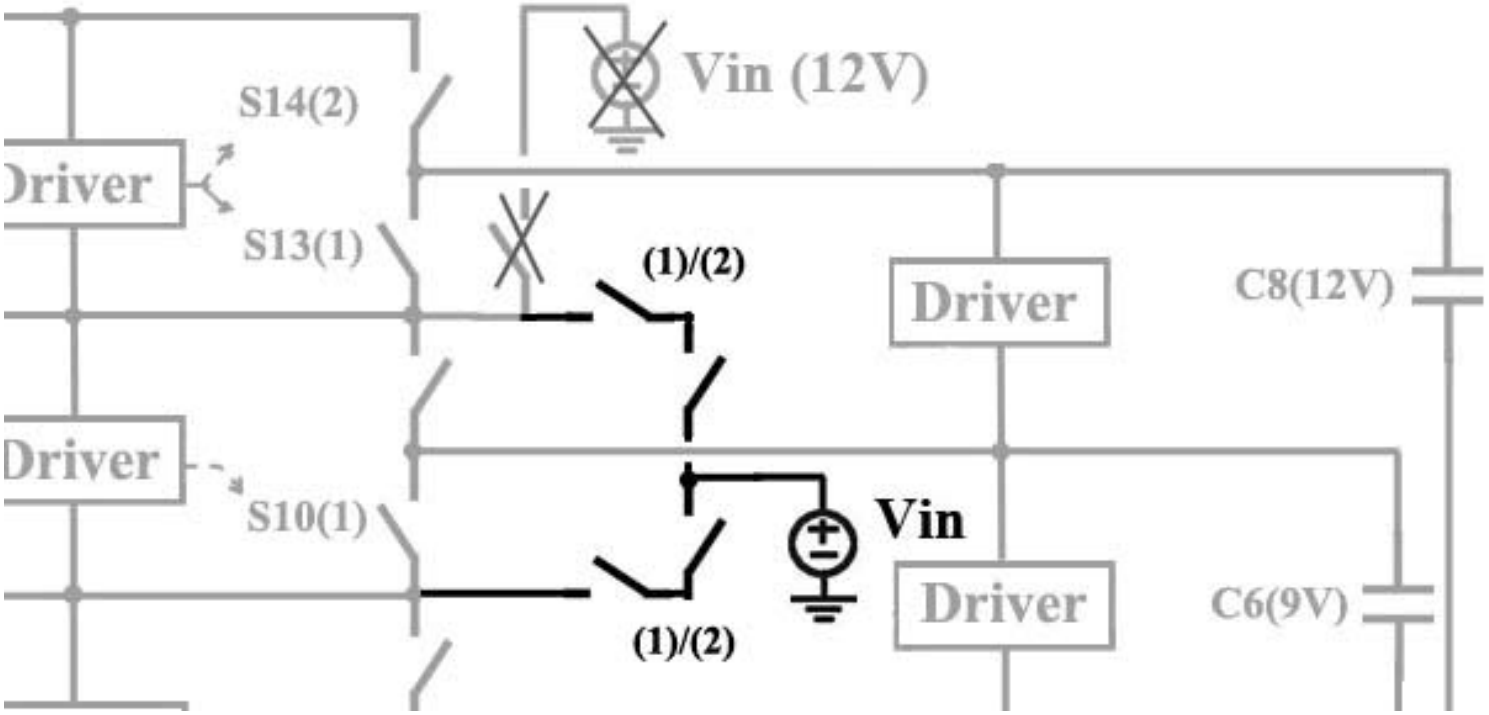
- Representative 0.13um tech
- 2.4-to-1.2V Conversion
- 1 sq mm M-I-M cap (2 nF
- Losses
  - SSL (main caps)
  - FSL (conduction)
  - Gate cap
  - Cap Bottom plate
  - Junction cap



Switched Cap Take-Aways

- Theoretical performance exceeds magnetic-based converters, and this is being realized in research
- Very simple low power operation – reduce clk
- Integration convenient for v. low power app's to v. high current app's
- Moderate (high) voltage capability by stacking devices – triple-well, SOI
- Regulation challenges – nominal fixed ratio, but can operate with multiple Taps
- Further on-chip integration via aggressive clk scaling

- Tap Changing for Line Regulation – Feedforward



- Multi-mode Operation for Apps like Voltage Scaling

Conduction Loss Comparison

M. Seeman, S. Sanders, IEEE T-PELS, March 2008

•Performance compared with switch GV^2 metric:

$$\frac{G_{OUT}V_{OUT}^2}{\sum G_i v_{r,i(rated)}^2}$$

•Since converters are bi-directional, graph applies equally to step-down converters

•Magnetic components modeled with *zero* conduction loss, and *no* switching loss impact