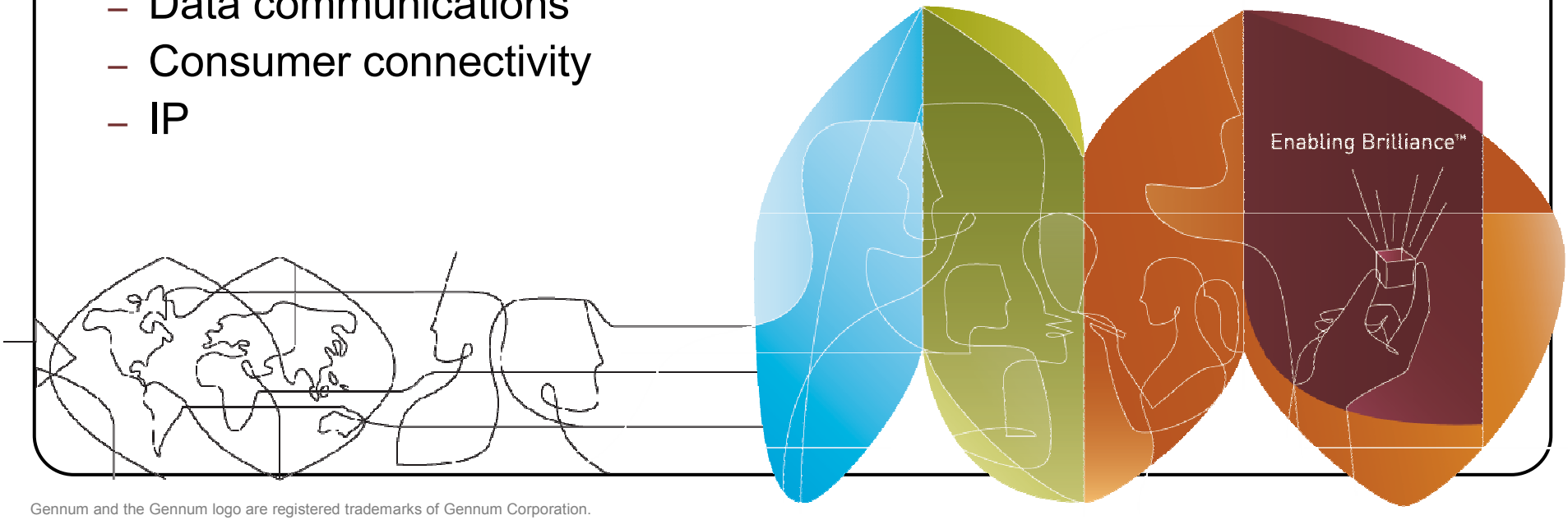
Applications, Processing and Integration Options for High Dielectric Constant Multi-Layer Thin-Film Barium Strontium Titanate (BST) Capacitors

Agenda

- Introduction
- What is BST?
- Unique Characteristics of Thin Film BST Capacitors
- Key Applications
- Device Technology
- Integration Options – SIP / SOC
- Summary

About Gennum

- **Overview**
  - Located in Burlington, Ontario, Canada
  - Total employees ~ 370
  - 2007 Revenue - $110 million CDN
- **Target Markets**
  - Video broadcast
  - Data communications
  - Consumer connectivity
  - IP
- **Global Sales Offices**
  - Canada, Germany, Japan, Korea, Taiwan, U.S.
- **Design Centers**
  - United Kingdom, Canada, Mexico, US, India



About Gennum

Gennum Advanced Technology Group
Areas of Activity

- **Thin Film BST Capacitor Technology (High Density Fixed Capacitors)**
  - *Interested in Partnering Opportunities with Foundries, Module Providers, IDMs and OEMs to Enable Rapid High Volume Commercialization*
- **Thin Film BST Tunable Capacitor Technology**
- **Thin Film BST / MEMS Voltage Controlled (BAR) Resonator Technology**

BST Thin-Film Capacitors

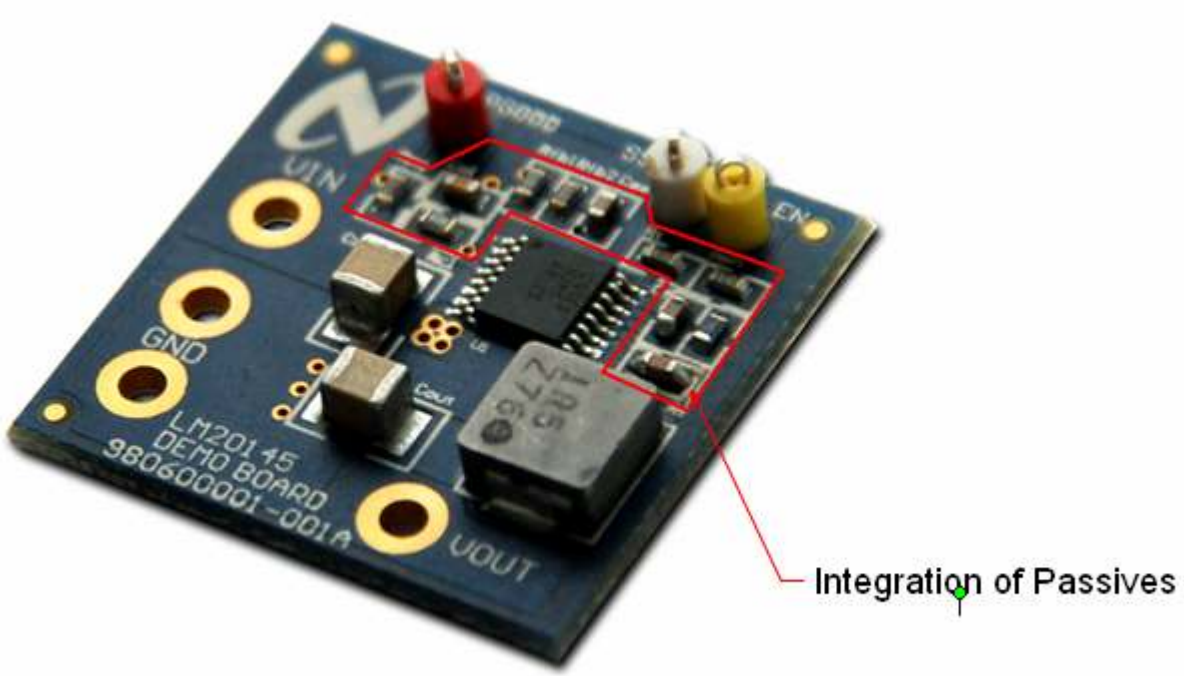
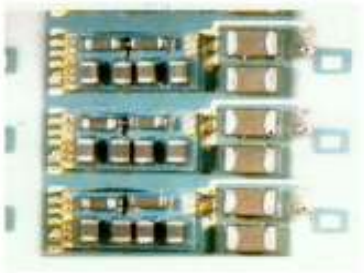
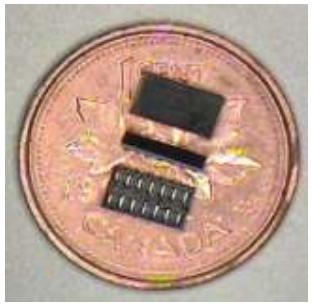


Image – Courtesy of National Semiconductor

Gennum BST History - How did we get here?

- Gennum as a market leading component provider for the Hearing Aid Industry decided to apply advanced technologies to further miniaturize it's product offerings
- Gennum developed
  - Advanced Packaging
  - High Density, Thin Film Capacitor Technology – BST
- Gennum's Fixed Capacitor BST Technology has been in production for 12 years for it's proprietary products.
- In 2007 Gennum decided to actively pursue partnerships and commercialize BST Technology beyond Gennum's proprietary products





BST Thin-Film Capacitors

What is BST?

- **Barium Strontium Titanate $Ba_{1-X}Sr_XTiO_3$**
- **Dielectric – Ferroelectric – Perovskite**
- **High Dielectric Constant (Bulk: 1000)**
  (Thin Films: 100 to 650)

Advantages

- **Integration of Passives (L,C,R)**
- **Miniaturization (x,y,z) – Thinned down to 100um …. 50um**
- **Performance – high quality low inductance de-coupling**
- **Reduced Cost**

BST Thin-Film Capacitors

- Characteristics of Thin Film BST Capacitors
  - **Capacitance Density (4 lyr films) > 100nF/mm2**
    - **Calcination Temp…….. >700C**
    - **Ba/Sr ratio ……. 50/50….60/40….70/30**
    - **Dielectric Thickness**
    - **Deposition Method (MOD – Sputtered)**
    - **Number of layers – up to 6**
  - **Non Linear Dielectric – Voltage Variable**
  - **Capacitance and Tuning Ratio Can Be Tailored (Ba/Sr)**
  - **Integratable With Thin-Film Resistors and Inductors**
  - **Hermetically Passivated….High Reliability**
  - **Low Inductance – Planer Capacitors, Interconnect**
  - **Substrate Options – Si, Al2O3, Sapphire**
  - **Lead Free**

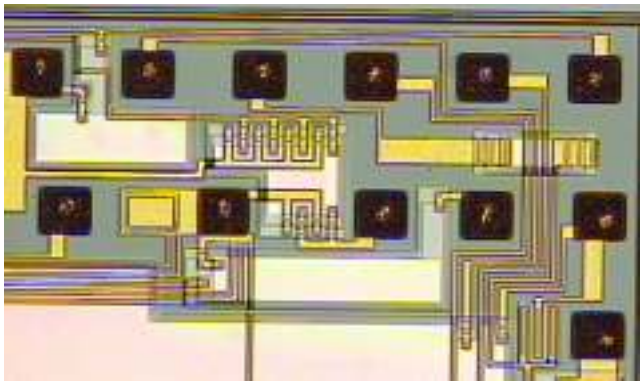
BST Thin-Film Capacitors

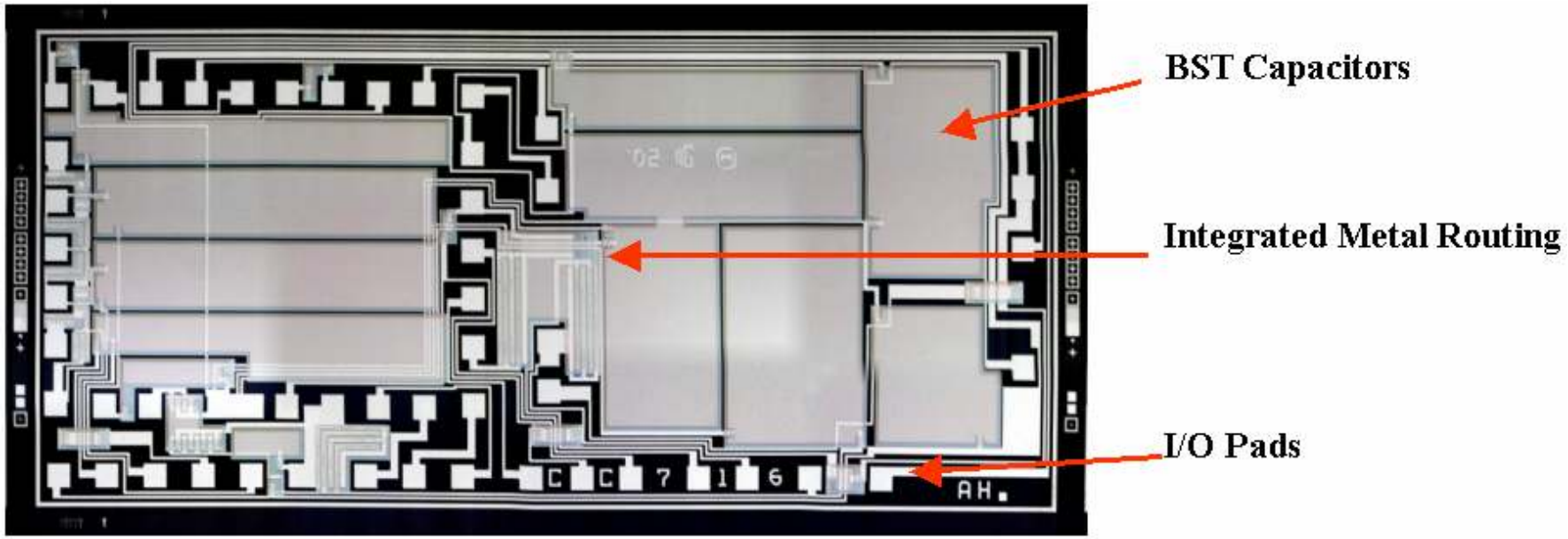
Key Applications

- **Power Supply Applications**
- **Miniature/Thin Form Factor Modules**
- **RF Devices**
- **Portable Devices**
- **Ultra-Thin Displays**
- **High Speed Applications – Microprocessors**
- **Medical – Hearing Aid Modules**
- **Embedded Passives - Laminates**

BST Thin-Film Capacitors

Example Capacitor Chip for DSP Audio System



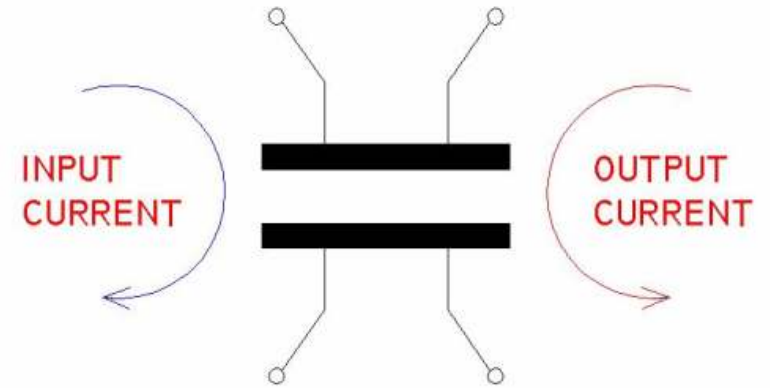


Silicon substrate, 23 capacitors, chip size approximately 3mm x 5mm
Total Capacitance: 740 nF

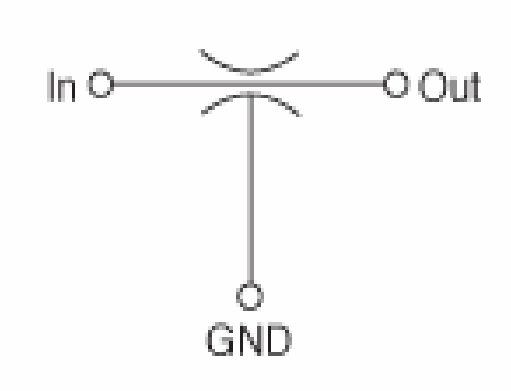
BST Thin-Film Capacitors

Multi-Terminal Capacitors

Switching Noise Isolation



EMI Suppression



BST Thin-Film Capacitors

Electrical Specifications

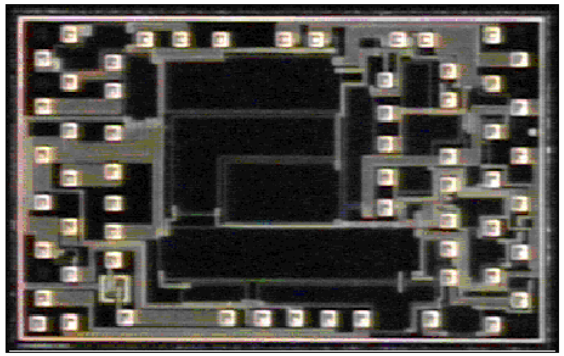
Parameter	High Density Low Breakdown	Units
Capacitance Density @ 0V	117	nF/mm^2
Capacitance Density @ 3.3V	75	nF/mm^2
Capacitance Values (per individual capacitor)	50 pF-350nF	-
Typical Dissipation Factor (1 MHz)	0.015	-
Maximum Leakage Current (per individual capacitor) @ 3.3V	30	nA
Operating Temperature	0 to 55	°C
Operating Voltage	3.3	V
Breakdown Voltage	20	V
Capacitance Change over temp. range	+1 to -2	%
Capacitor Tolerance	10	%
Capacitor Matching	1	%

BST Thin-Film Capacitors

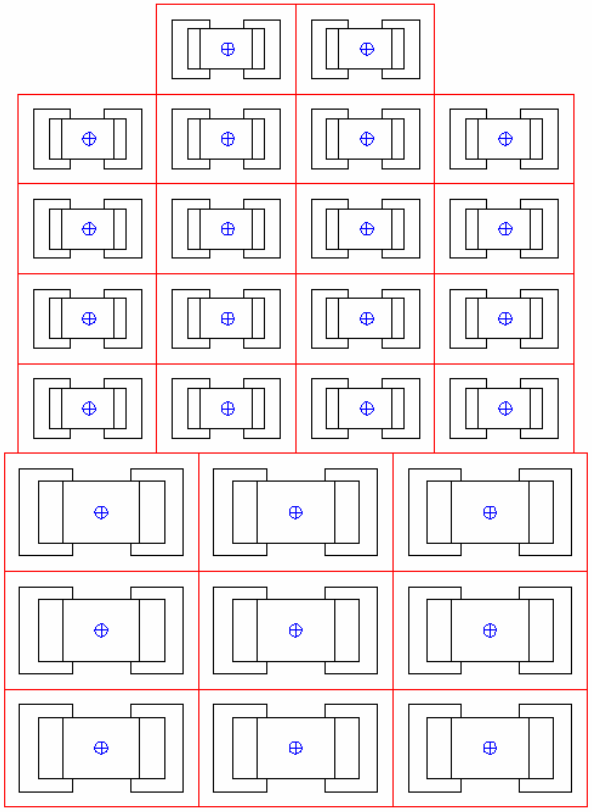
Mechanical Specifications

Parameter	Min	Typ	Max	Units
Die Thickness	100	150	500	um
Chip Size	1x1	-	-	mm
I/O Pad Size	80x80	100x100	-	um
Pad Pitch	150	150	-	um
Gold Bump Height	2	5	25	um
Al interconnect thickness		1.8		um
Gold interconnect thickness		1.5		um
Solder Bump Height	-	125	-	µm
Wire-bond and Flip-Chip	-	Yes	-	-
Alumina Substrate size		4		inches

BST Thin-Film Capacitors



THINFILM
CAPACITOR NETWORK
23 CAPS Ct=600nF



EQUIVELENT TO
14 - 0201's
9 - 0402's

BST Thin-Film Capacitors

Capacitor Construction

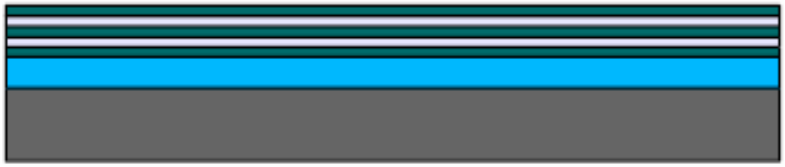
- Substrate Options:
  - Silicon – for low cost general filtering and decoupling
  - Alumina – (under development) for high frequency applications
  - Sapphire – **(under development)** for high power / high temp applications)

- Multi-layer construction – 5Pt electrodes separated by 4 BST dielectric layers forming a 4 layer capacitor – each layer may be connected in series and/or parallel
- Capacitors are patterned, and covered by an Inter-Layer Dielectric (ILD)
- Vias are formed in the ILD to allow connectivity to individual layers
- Aluminum routing layer is applied and patterned to complete interconnect
- Entire structure is hermetically passivated with openings for I/O pads
- Pb Free

BST : Process Steps

A) Oxidized silicon or glazed ceramic substrate

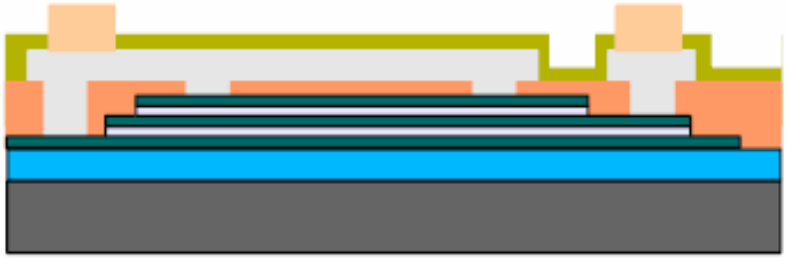
B) Build up 1 to 6 layers of Pt/BST by either MOD or sputtering (2 layers shown)

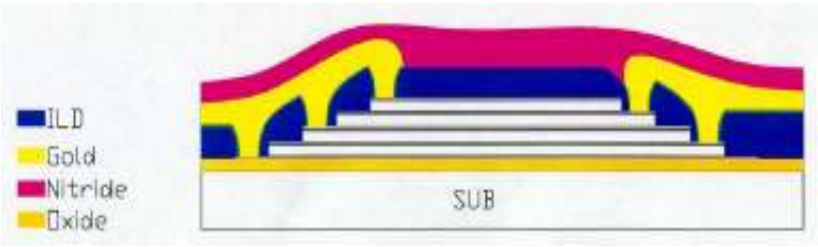


C) Pattern layers to form a mesa structure with access to all electrodes

D) Apply a planarizing and insulating ILD glass layer. Pattern and etch vias.

E) Aluminum metalization, nitride overcoat and gold bump





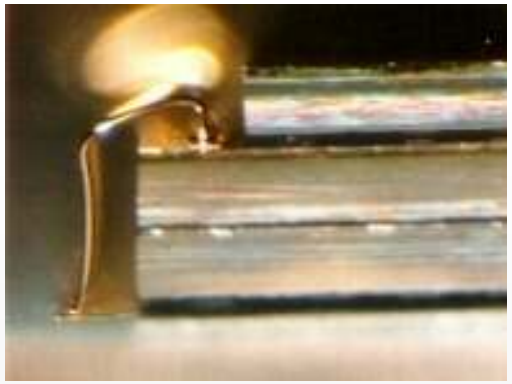
BST : Process Steps

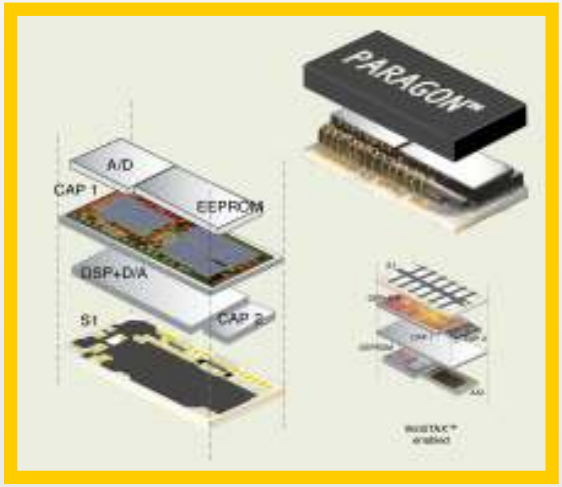
Fabrication Process Overview
Photolith (11-12 mask lyrs)
Pt Deposition (5 lyrs sputtered)
BST Deposition (4 lyrs sputtered)
Patterning (Ion Mill or Etching)
ILD Dep and Patterning
Metal Dep and Pattern
Hermetic Passivation Dep and Pattern
Bump

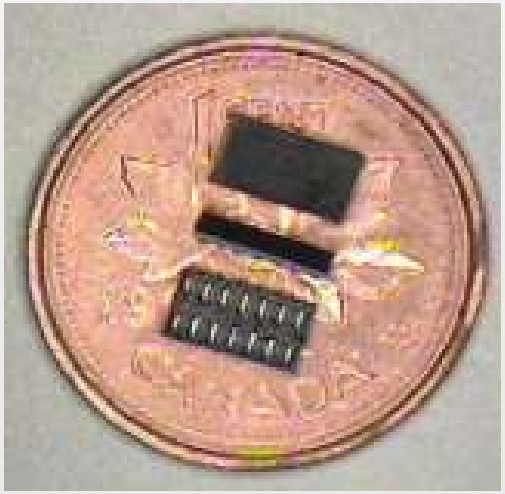
Assembly and Integration Options

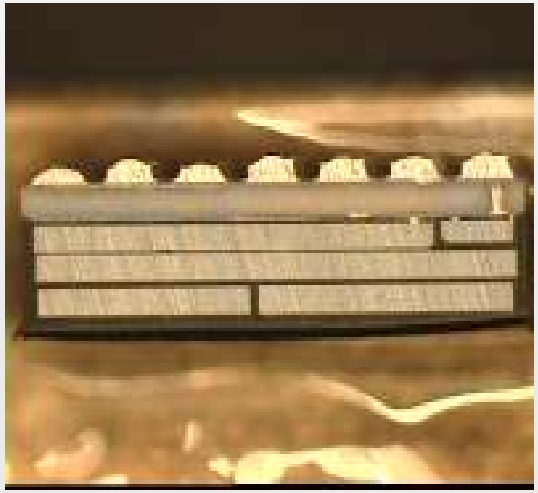
Assembly Options

- Wire bonding, Flip-chip and Surface mountable
- BST capacitors can tolerate reflow temperatures up to 300ºC
- Chip stacking assembly process available at Gennum
    - Flip-Chip On Wafer
    - Cascade Wire bonding
- Available thinned to 100um – can be successfully thinned down to 50um
- Completed and tested devices available on tape or waffle packages

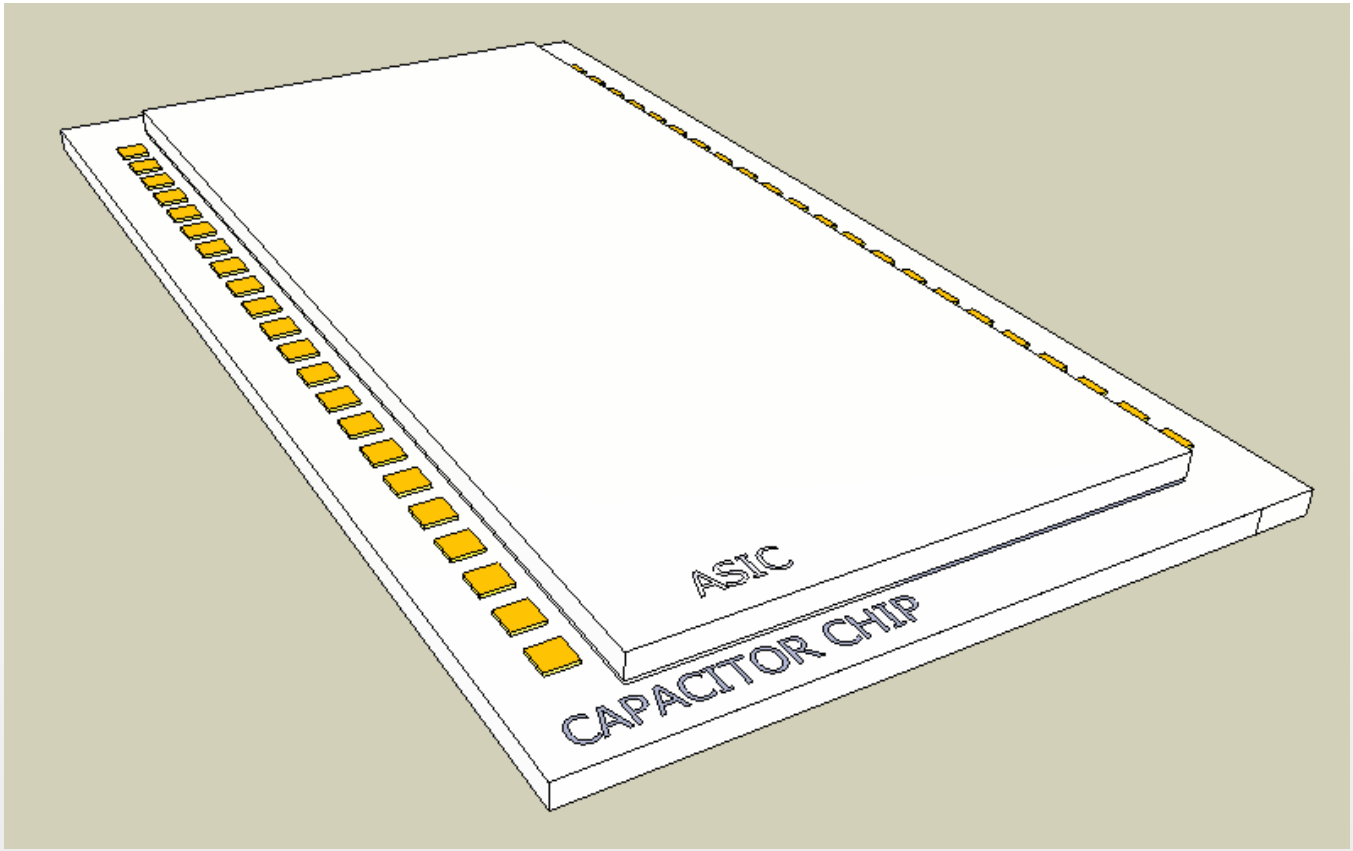








Assembly and Integration Options



Process Steps:

1 – Flip chip attach ASIC onto Capacitor Wafer (solder reflow and clean)

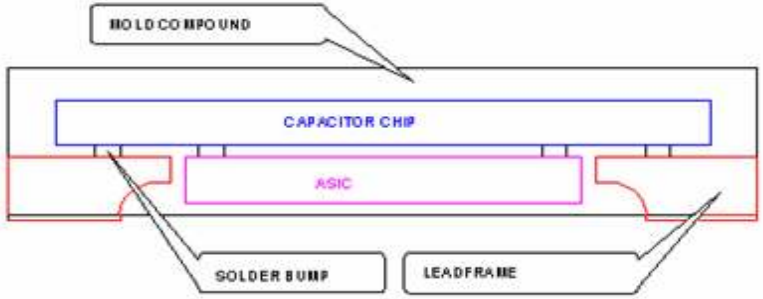
2 – Dice wafer assembly to singulate stacked chip module

3 – Final packaging and test

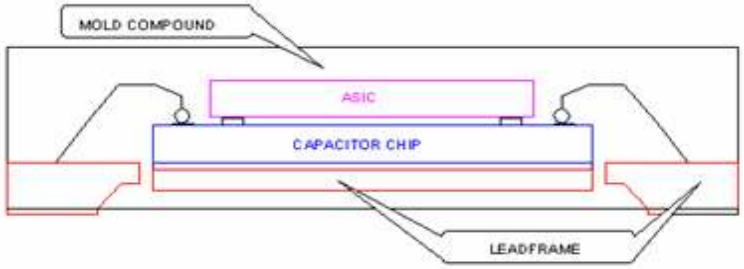
Assembly and Integration Options

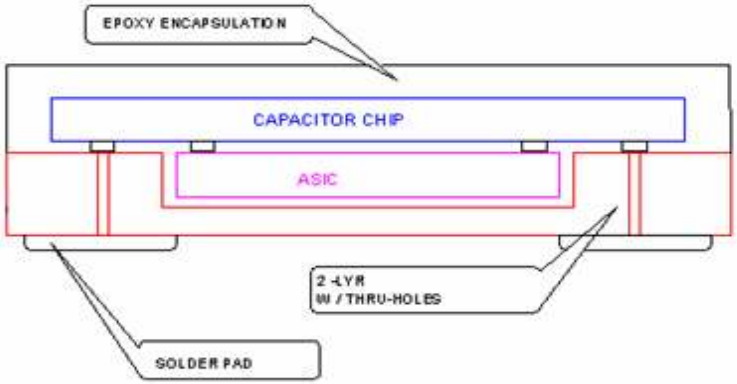
LOW COST PACKAGING OPTIONS

FCOL™ (Flip-Chip on Lead Frame)



MicroLeadframe™ (MLF)



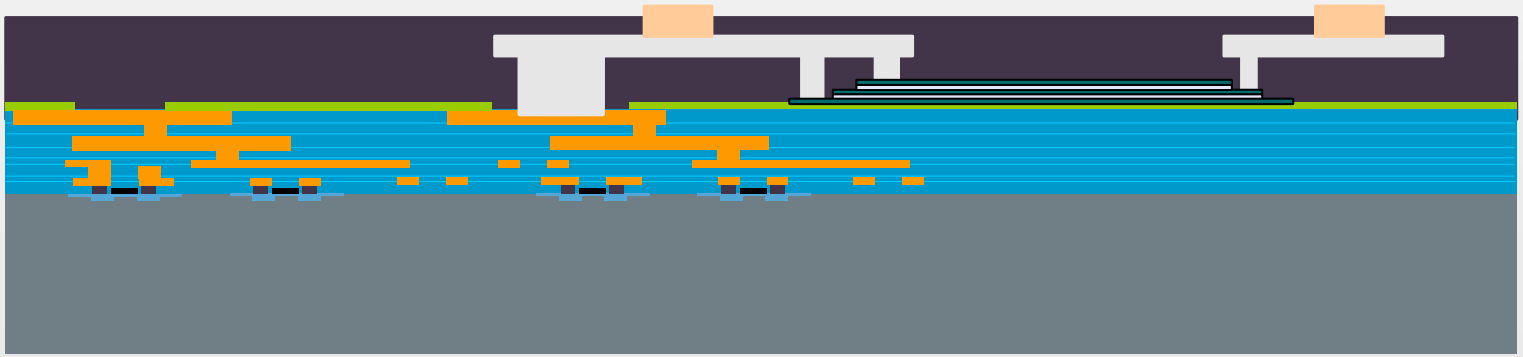


CHIP CARRIER SUBSTRATE

Assembly and Integration Options

Integration before backend processing

Integration after backend processing



BST Thin-Film Capacitors

Summary

BST thin film capacitors…..

…enables integration of passives for SIP and potentially for SOC implementations of DC-DC converters

…makes possible effective high quality on chip “at pad” decoupling

…produced using standard thin film processing tools and techniques

…scaleable for high volume production

Thank-You

BST Thin-Film Capacitors

Thank-you

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