High Efficiency Micro-inductors on Silicon

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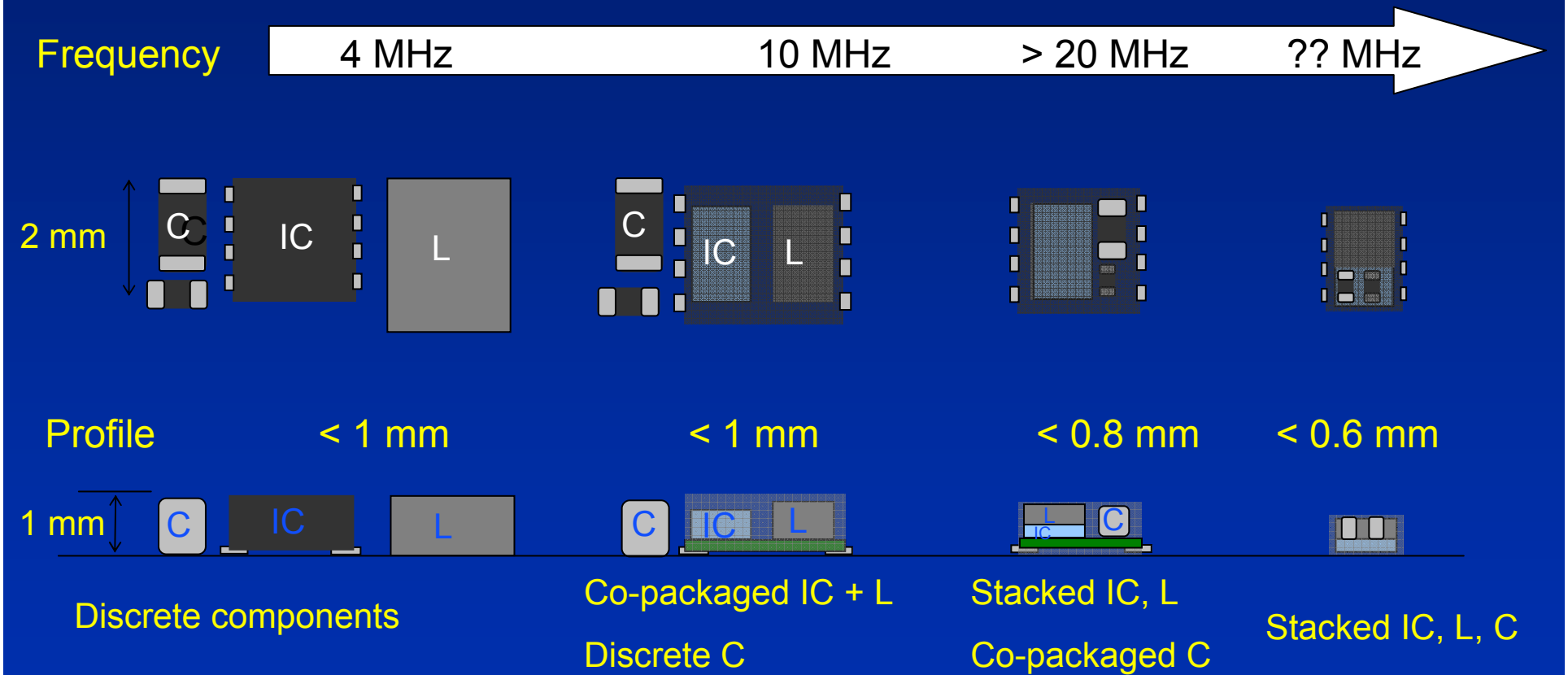
Overview

- Why micro-inductors on Silicon?
- Overview of micro-inductor technology
- Design approach and goals
- Results from fabricated devices
- Summary

Size Reduction with frequency

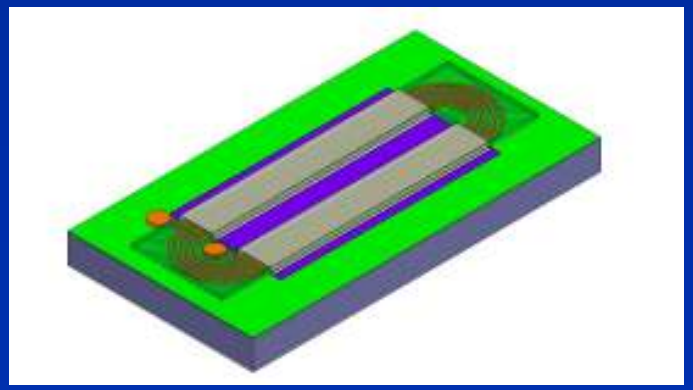


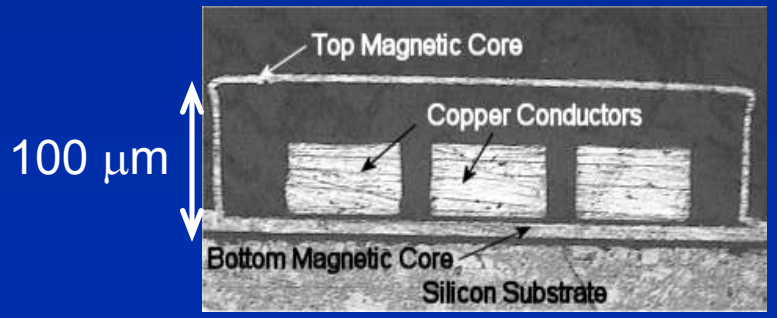
Why Micro-inductors on Silicon?

- Stacked IC and Inductor requires:
  - Inductor operation at high frequency (> 20 MHz)
  - Size & form factor compatibility between IC and inductor (< 4 mm^2)
  - Low Inductor profile (< 0.3 mm)
  - Packaging scheme
- Micro-fabricated inductor can satisfy these requirements

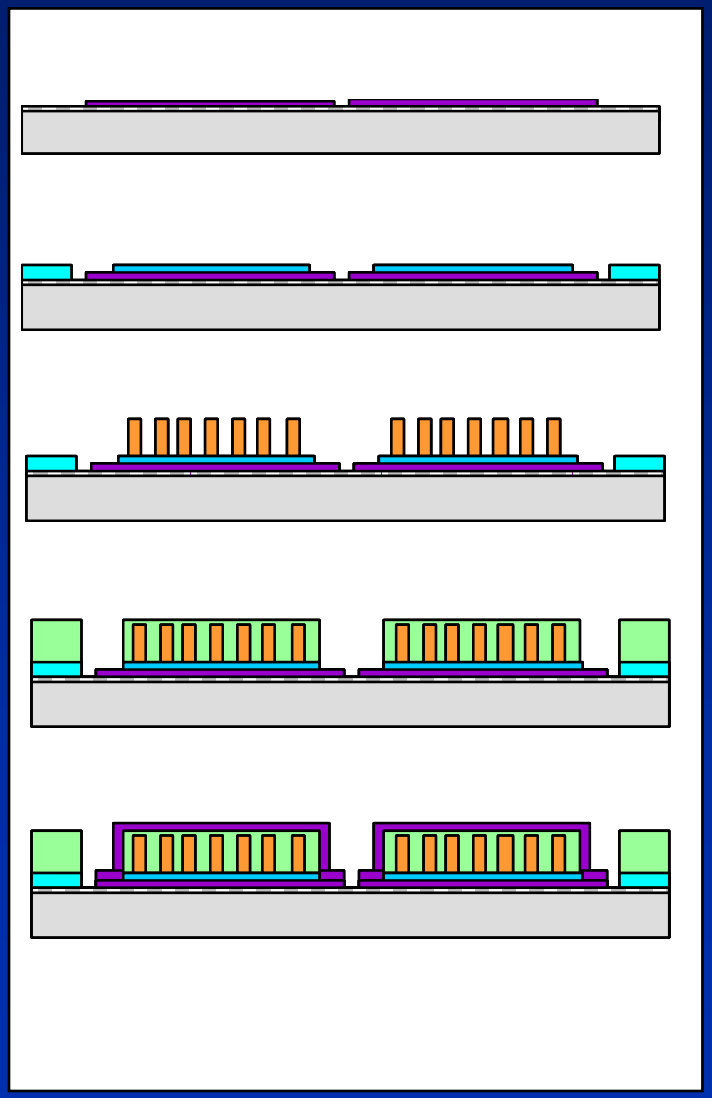
Magnetics on Silicon: Tyndall Approach

- Single layer of racetrack shaped copper coils sandwiched between layers of magnetic material
- Copper coils deposited by electroplating
- Core consists of thin film of NiFe alloy deposited by electroplating





Overview of Fabrication Process



Layer 1: Electroplated bottom core layer

Layer 2: Insulator layer between bottom core and winding

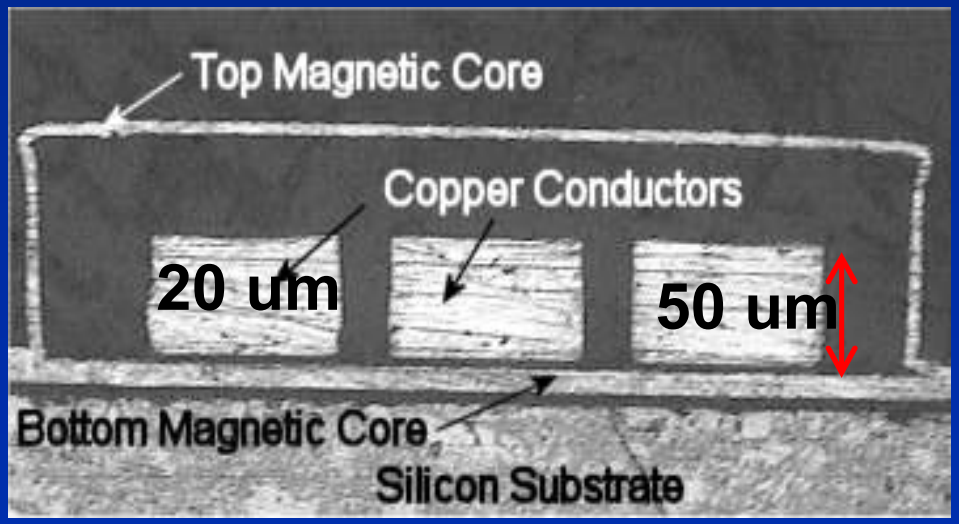
Layer 3: Electroplated copper winding layer

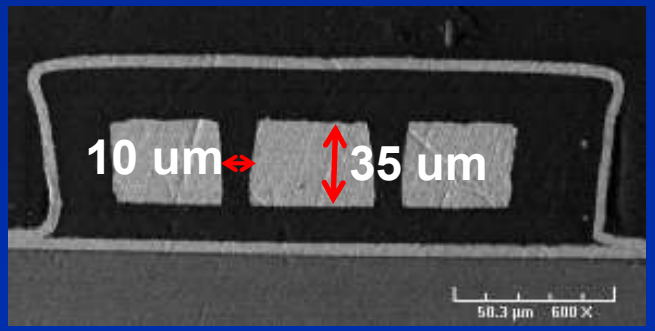
Layer 4: Insulator layer between top core and winding

Layer 5: Electroplating top core layer

Winding Technology

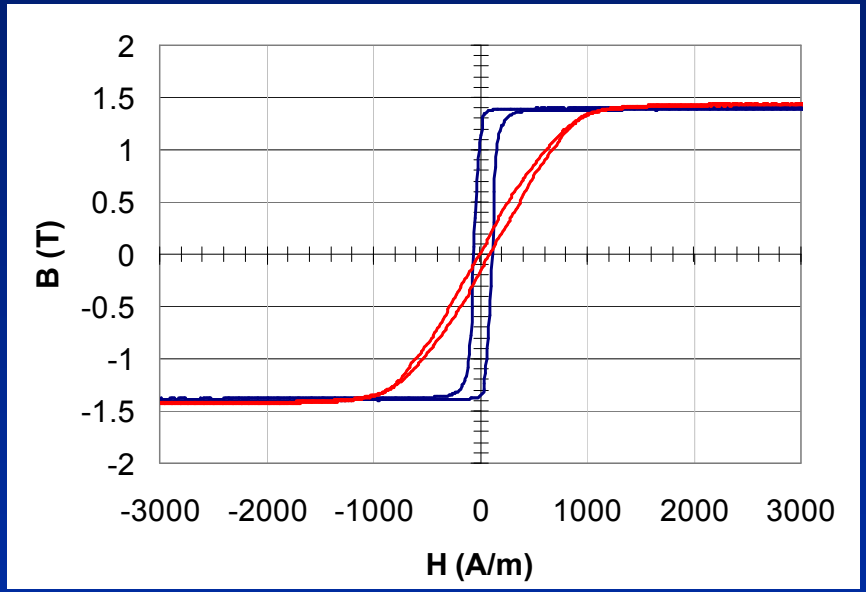
Electroplated copper	
Maximum conductor thickness, t_m	50 μm
Minimum spacing – linked to thickness	$t_m/3$



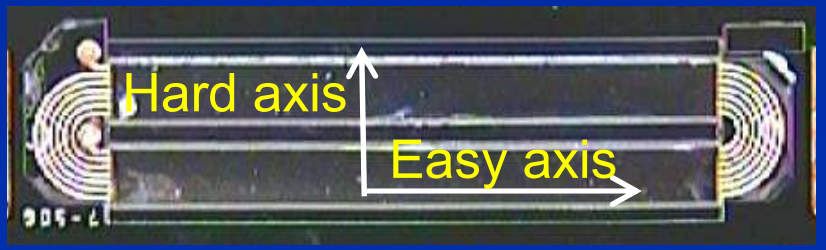


Magnetic Core Material

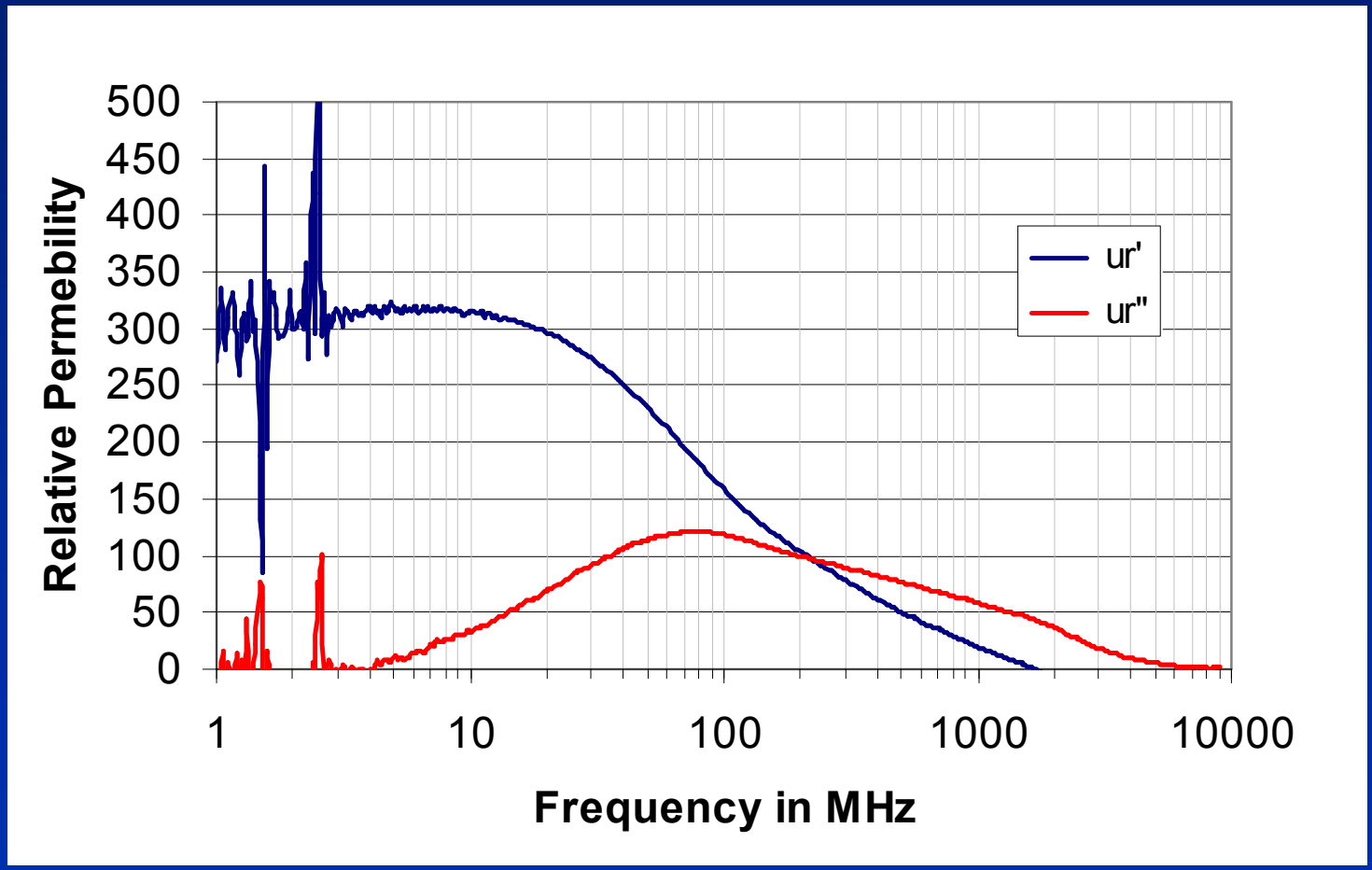
Electroplated $Ni_{45}Fe_{55}$	
Saturation, B_{sat}	1.44 T
Coercivity, H_c	80 A/m
Resistivity, ρ	45 $\mu\Omega$ cm
Anisotropy, H_k	800 A/m



Anisotropy induced in material during deposition



Permeability vs. frequency



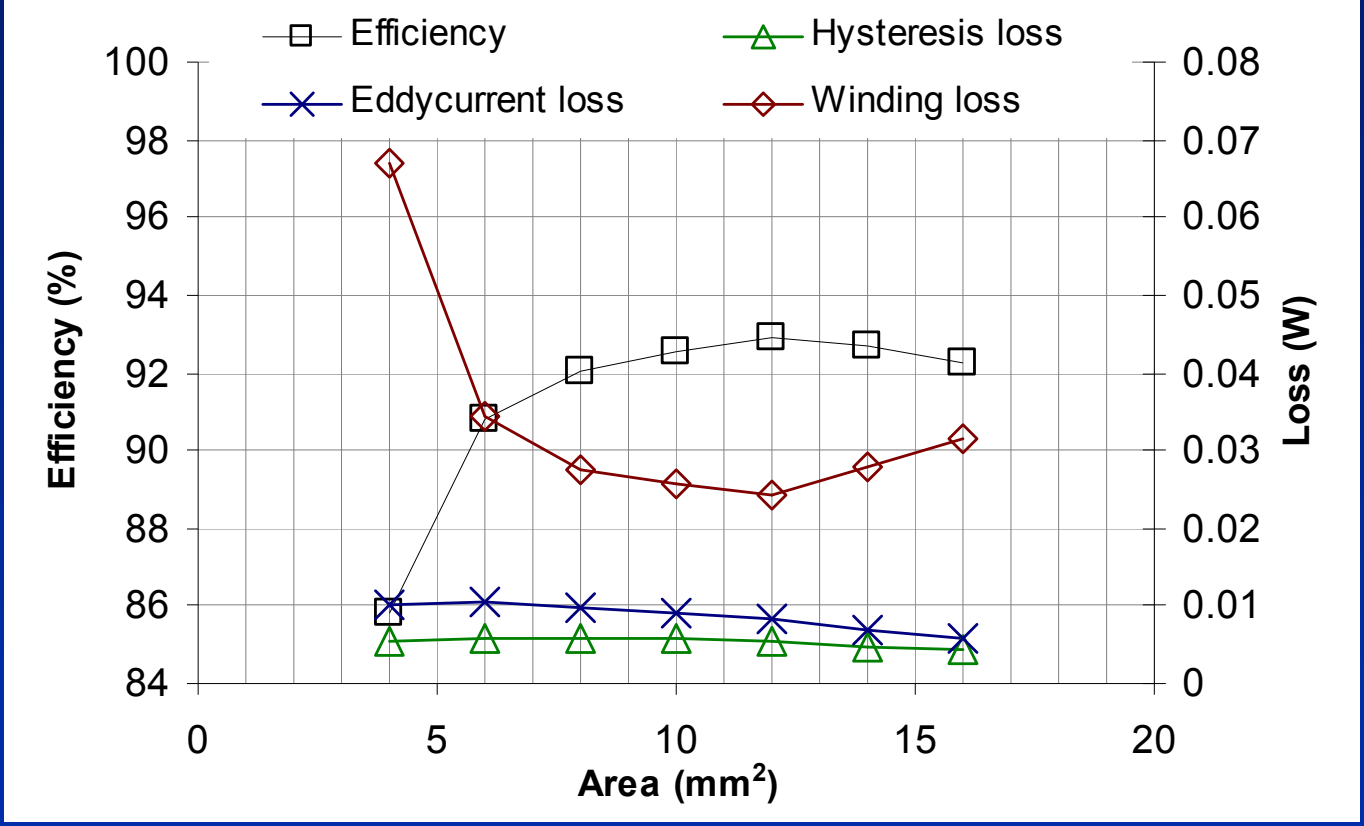
Design Approach

- Size and Efficiency are the key design parameters
- Define Inductor Efficiency as figure of merit

$$Efficiency = \frac{Converter\ Output\ Power}{Converter\ Output\ Power + Inductor\ Loss}$$

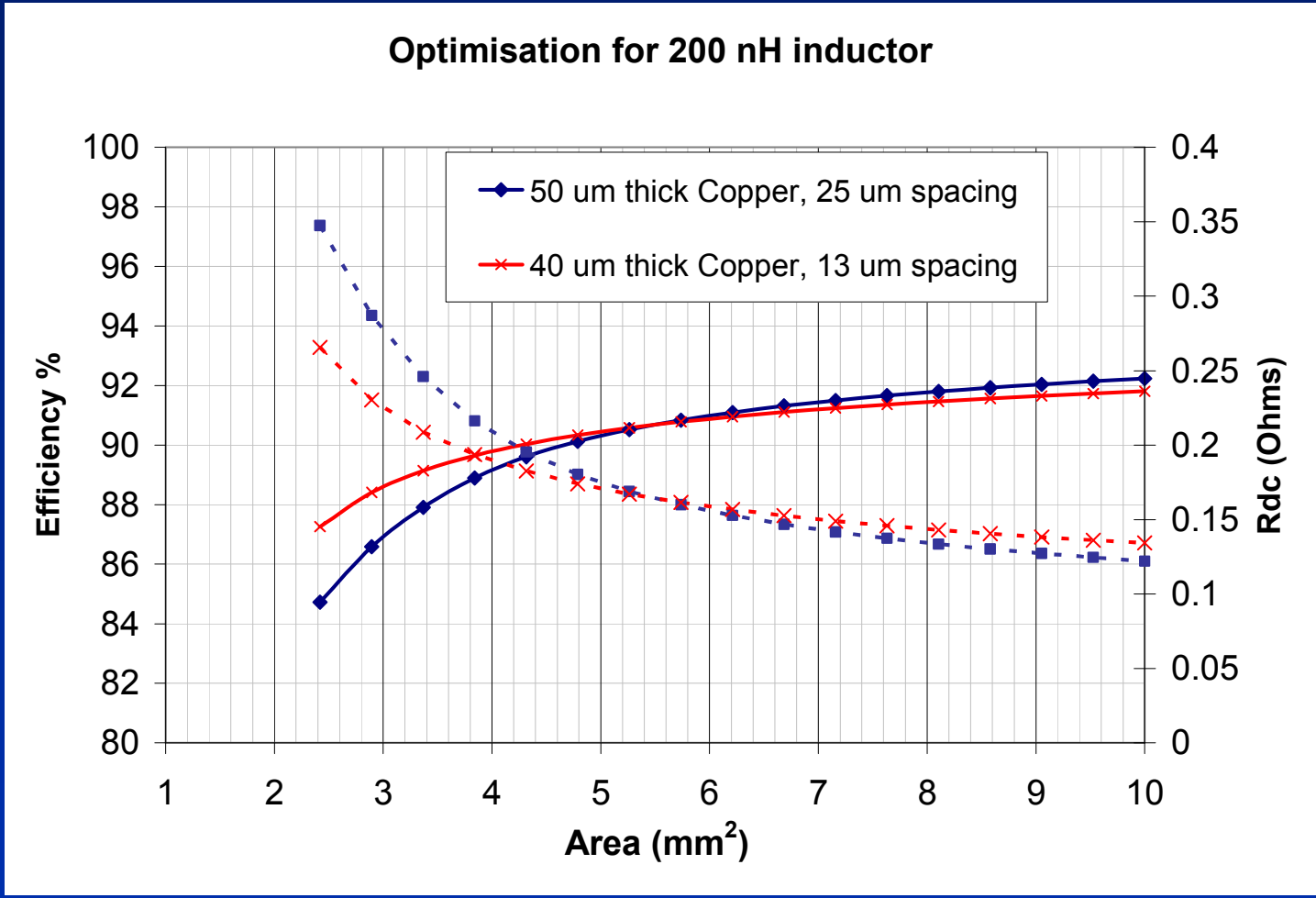
- Optimization based on analytical model for inductor
- Model Includes:
  - Core loss: Eddy currents + Hysteresis
  - Winding loss: DC + AC (6 harmonics)
- Goal of Optimization:
  - Maximize efficiency in any given area

Efficiency-Area trade-off



- Maximum Efficiency vs. Area, L =120 nH
- V_{in} = 3.6 V, V_{out} = 1.2 V, I_{out} = 500 mA, I_{ripple} = 0.6 I_{out} , f=20 MHz

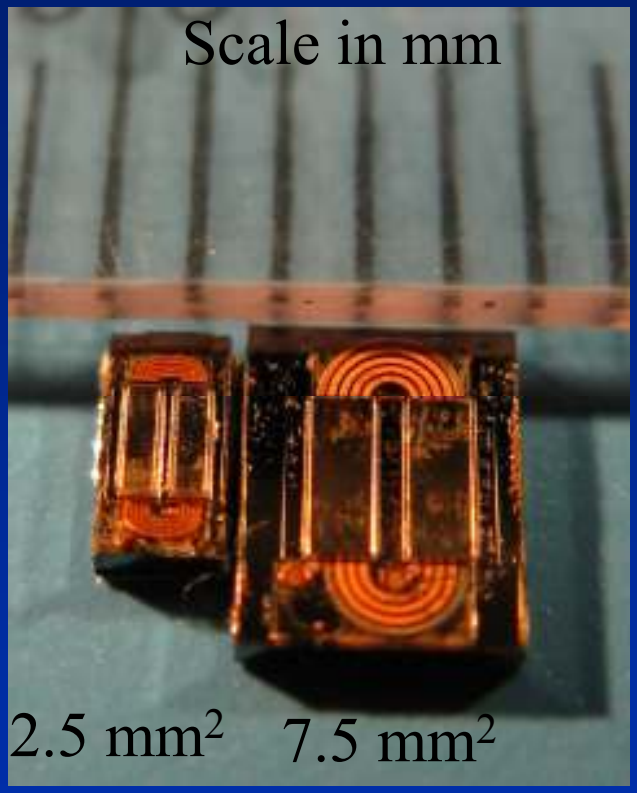
Micro-inductor Optimisation



Fabricated Devices

- Design Inductance range
  - 0.5 $mm^2 \rightarrow$ 10 – 40 nH
  - 1.3 $mm^2 \rightarrow$ 30 – 200 nH
  - 2.5 $mm^2 \rightarrow$ 30 – 200 nH
  - 5.5 - 10 $mm^2 \rightarrow$ 100 – 300nH

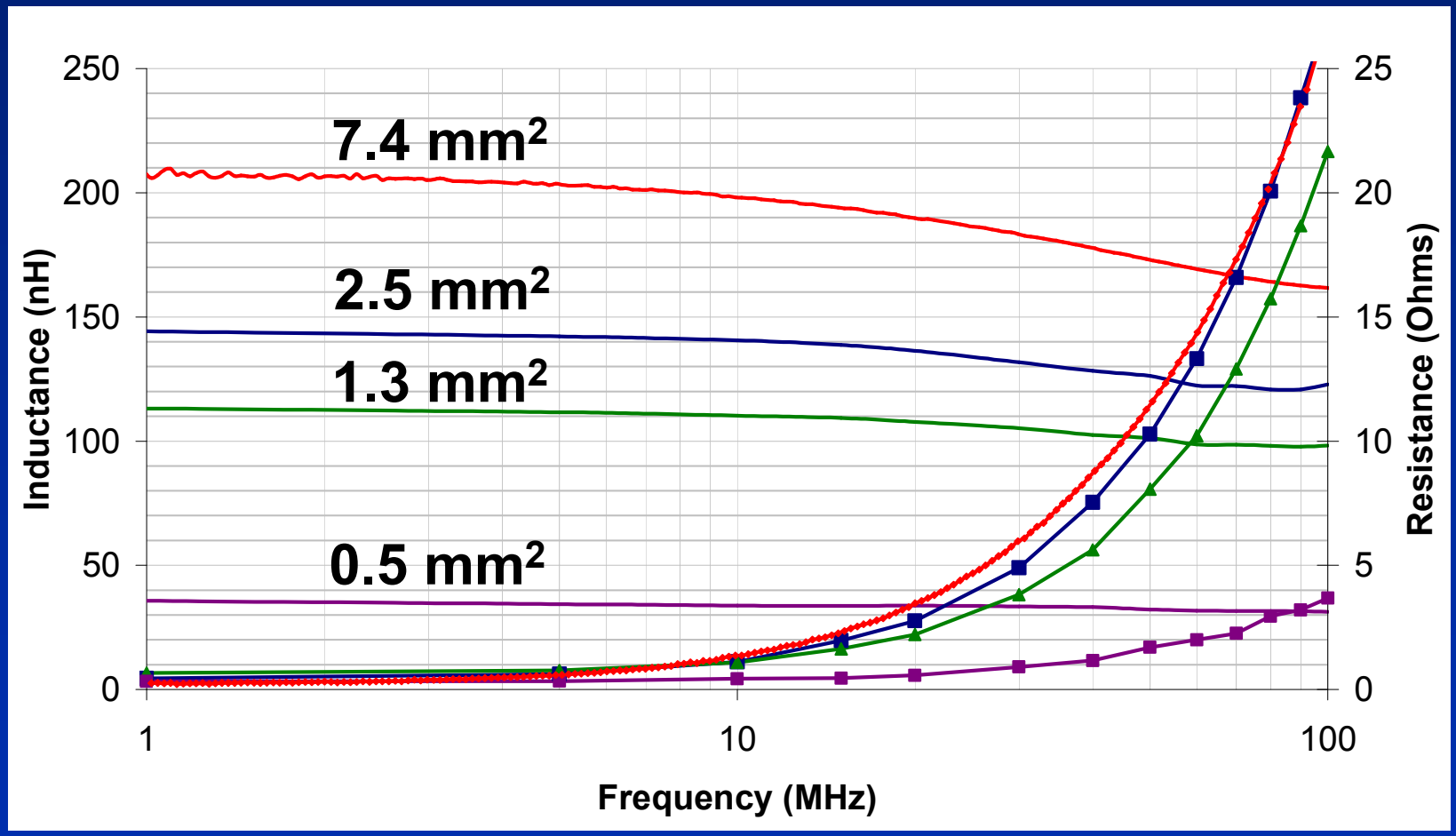
– Designed to maximize efficiency for:
  - Vin = 3.6 V, Vout = 1.2
  - f = 20 Mhz



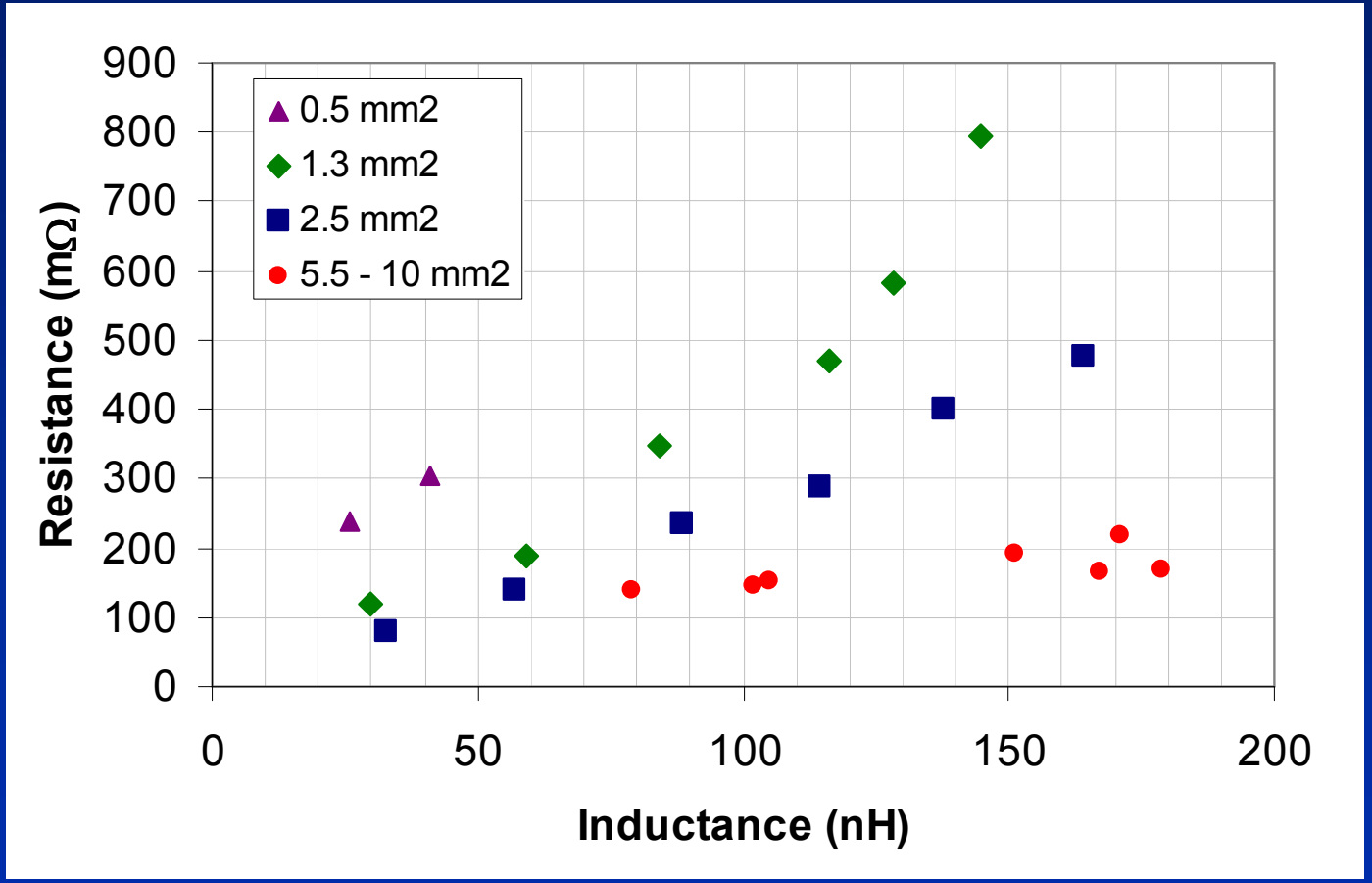
Two 140nH inductors

Typical L and R vs. f

- Inductance and resistance vs. frequency



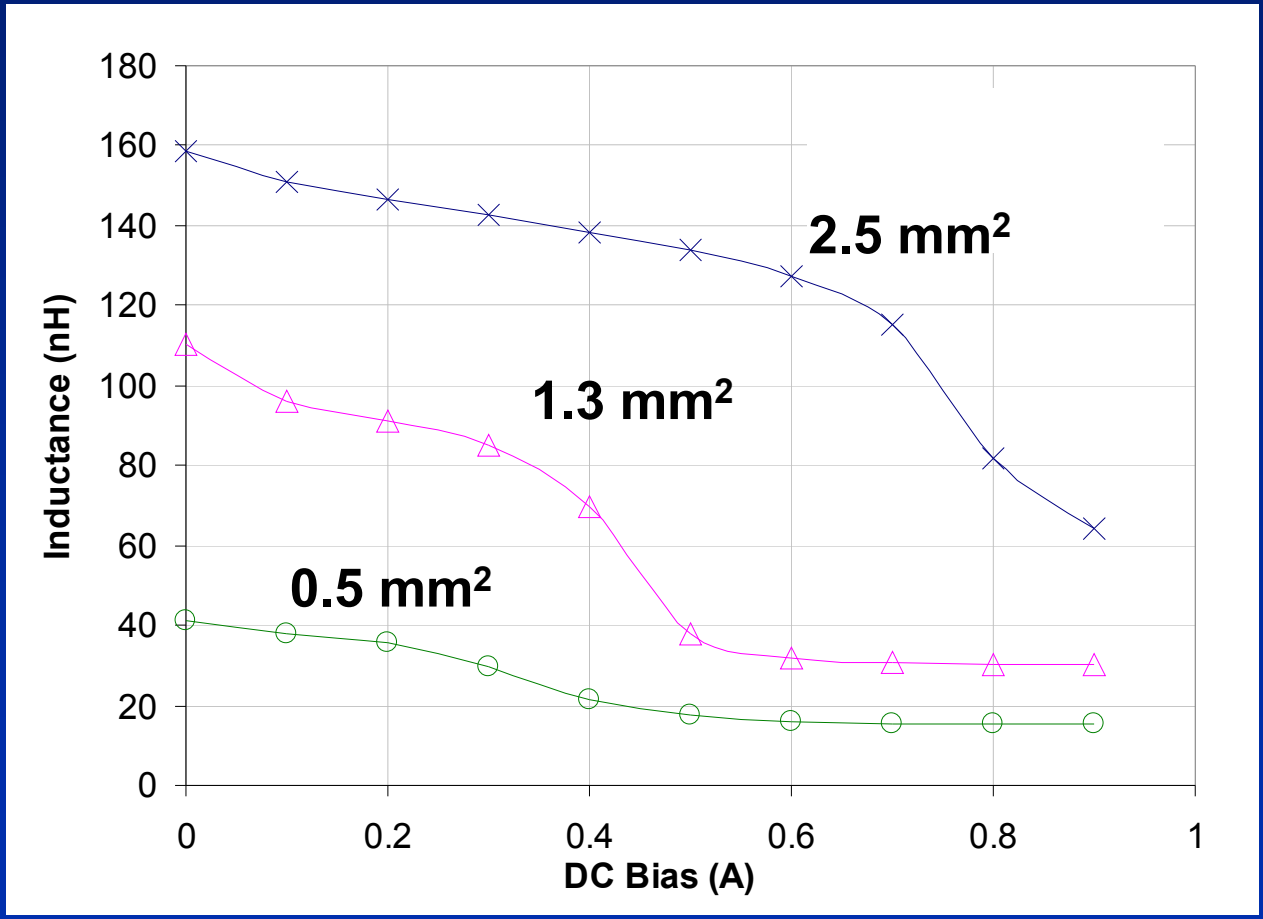
Inductance & DC resistance



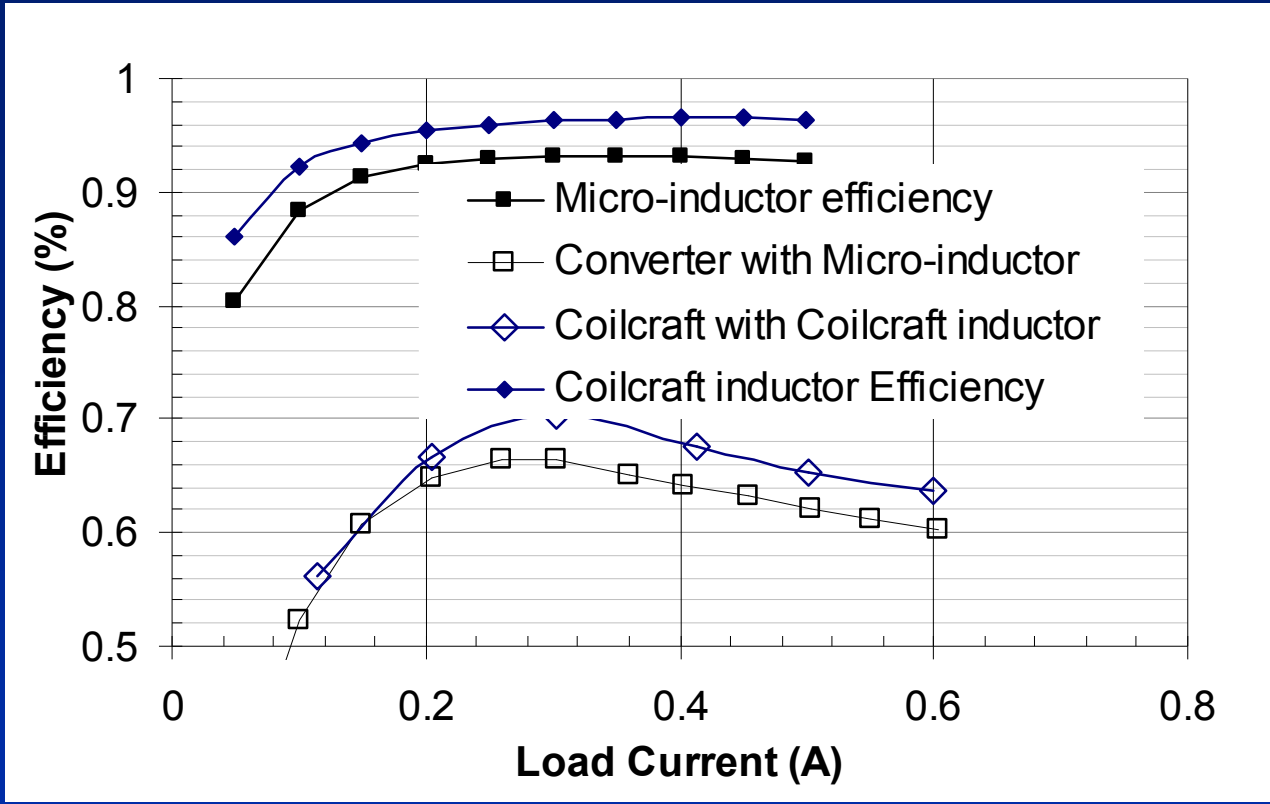
- Measured inductance vs Rdc vs. area achieved to-date

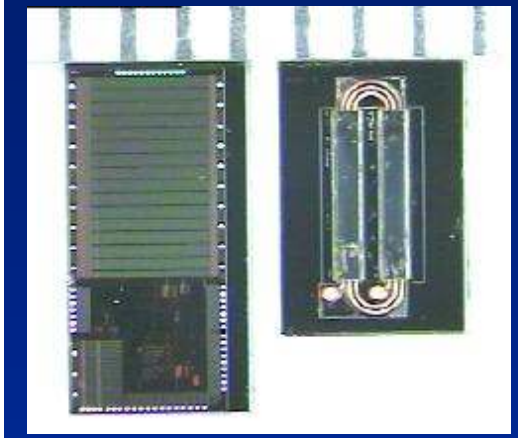
Typical DC Bias Characterization

- Inductance at 20 MHz vs DC bias current



Efficiency in Converter

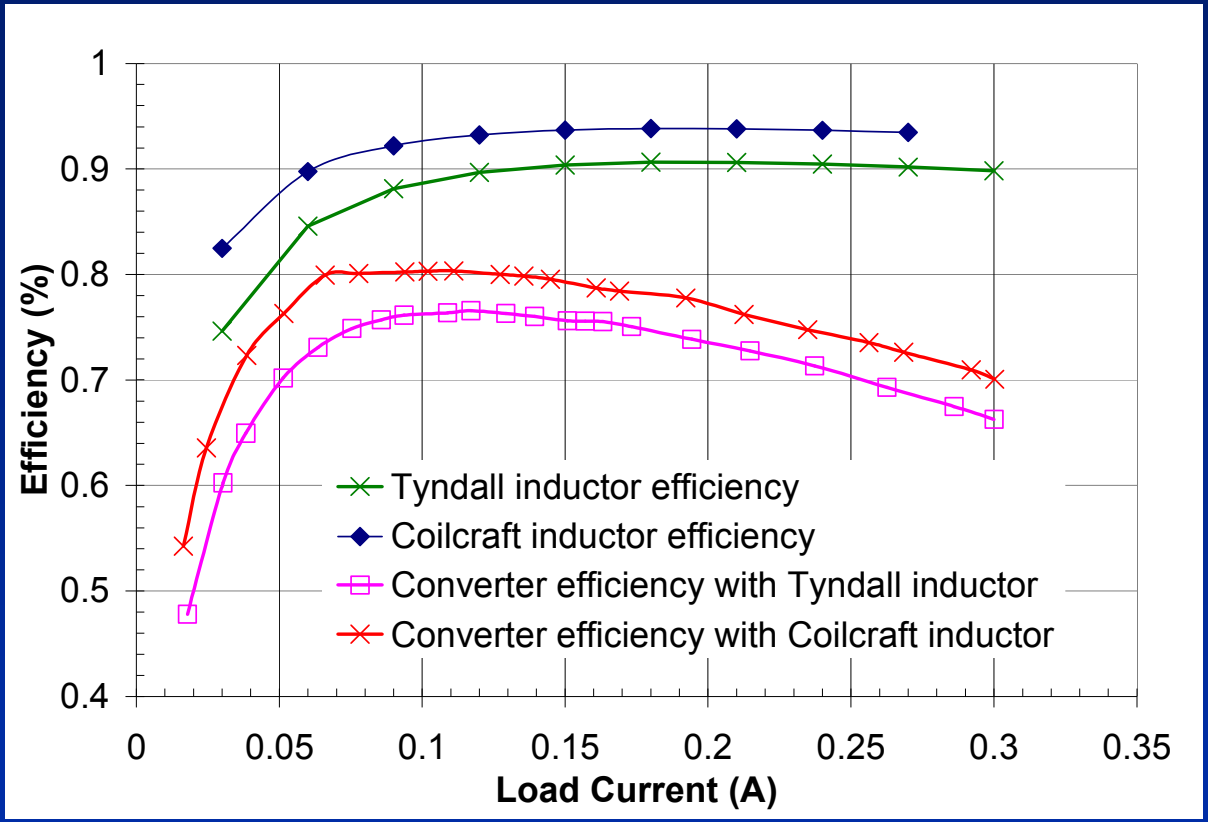




110 nH micro-inductor & converter IC

- 110 nH micro-inductor (5.5 mm^2) compared to 110 nH wire-wound inductor in a 20 MHz dc-dc converter
- First generation 20 MHz converter designed by PERL group in University College Cork, Vin = 2.6 V, Vout = 1.2 V

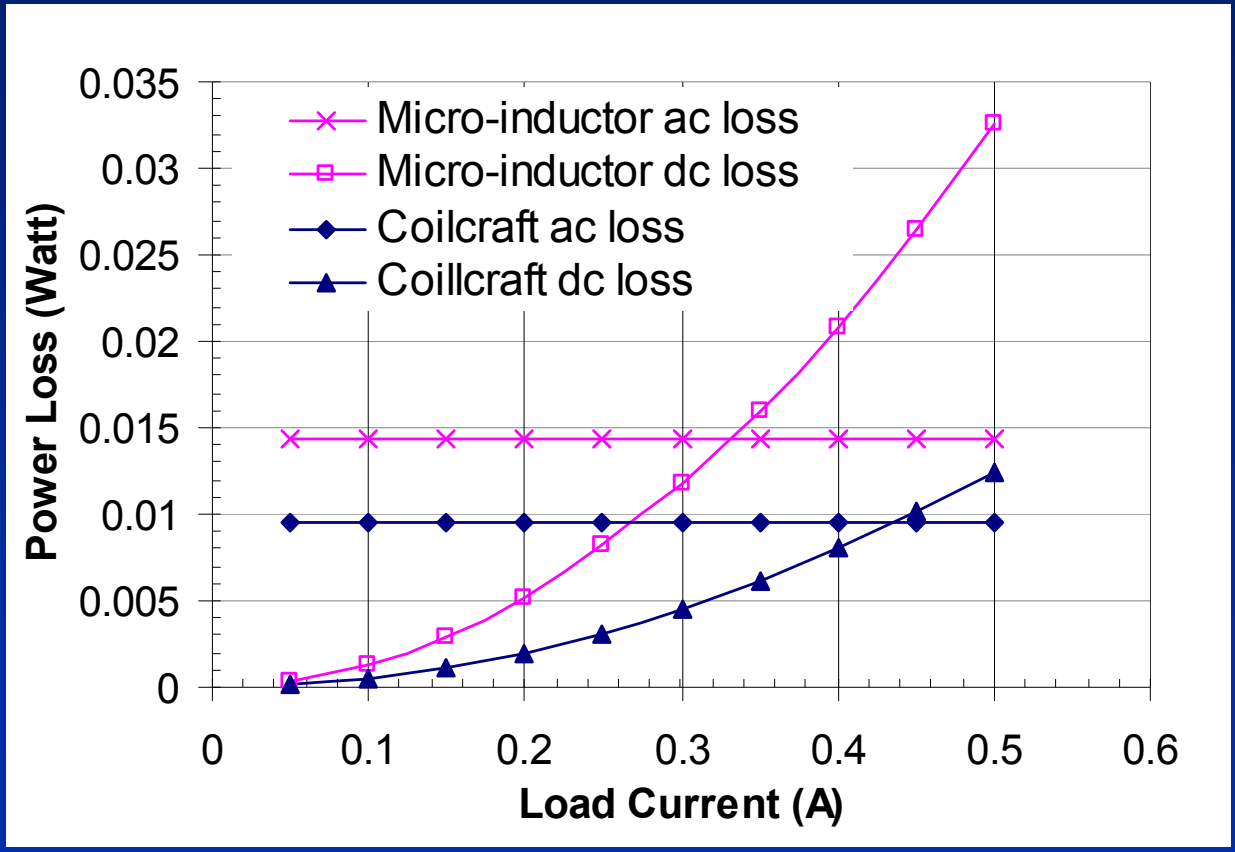
Efficiency in Converter



- 160 nH micro-inductor (2.5 mm^2) compared to 140 nH wire-wound inductor (Coilcraft 0402_AF141) in a 20 MHz dc-dc converter
- Second generation 20 MHz converter designed by PERL group in University College Cork, Vin = 3.0 V, Vout = 1.5 V

Comparison of losses

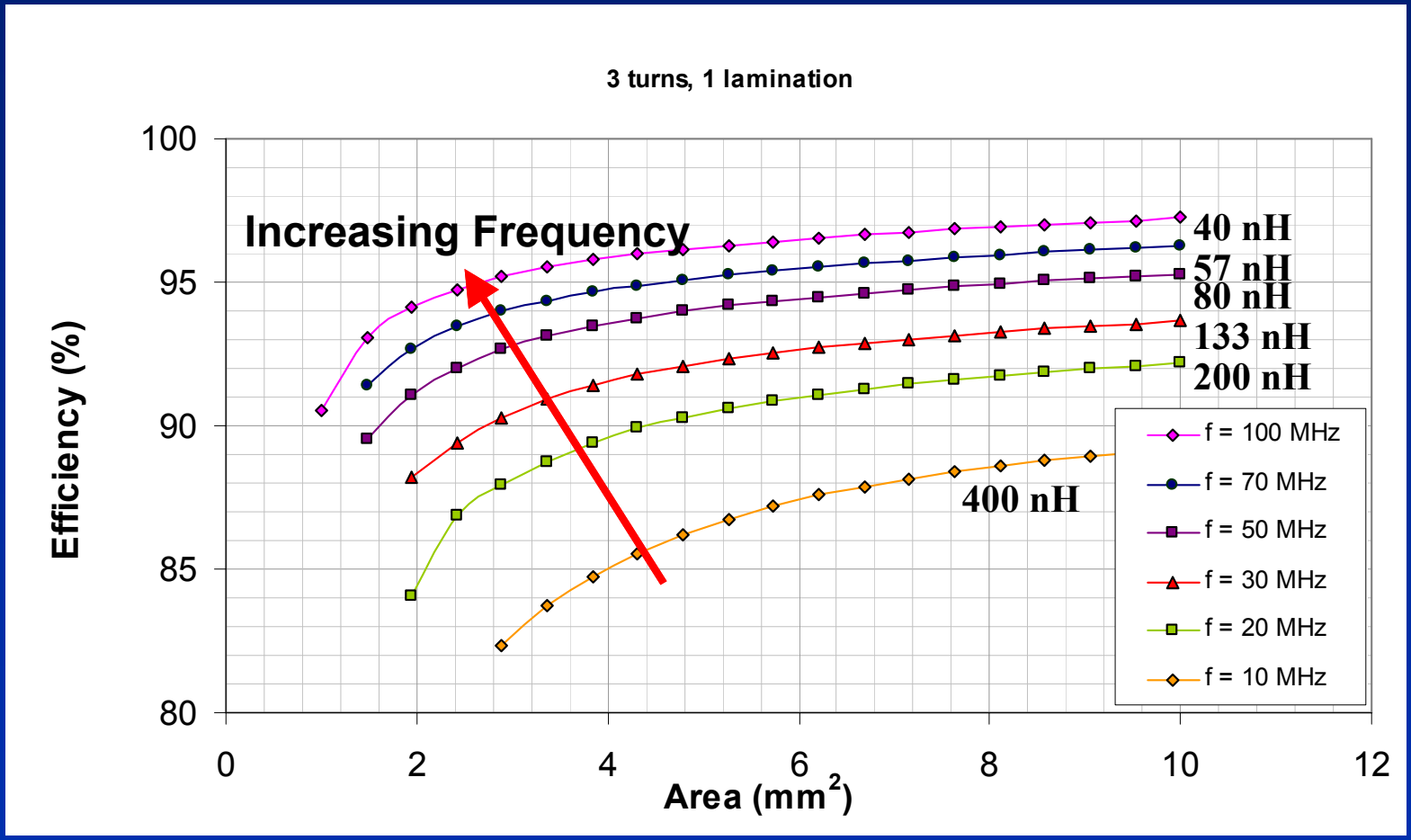
- Comparison of losses in micro-inductor to wire-wound inductor



- Further reduction in DC resistance of micro-inductor required

Beyond 20 MHz ?

Efficiency vs. area vs. frequency for present technology



Summary

- Extremely low profile inductor technology
- Allows stacking of inductor and converter IC
- Inductor efficiency of approximately 93% achieved at 20 MHz
- Higher efficiency and smaller size possible at higher frequencies

Acknowledgements

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Thank you for your attention!

Questions?