High Efficiency Micro-inductors on Silicon


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Overview

• Why micro-inductors on Silicon?
• Overview of micro-inductor technology
• Design approach and goals
• Results from fabricated devices
• Summary
Size Reduction with frequency

Frequency
- 4 MHz
- 10 MHz
- > 20 MHz
- ?? MHz

Profile
- < 1 mm
- < 1 mm
- < 0.8 mm
- < 0.6 mm

Discrete components
- IC
- L

Co-packaged IC + L
- Discrete C

Stacked IC, L
- Co-packaged C

Stacked IC, L, C
Why Micro-inductors on Silicon?

• Stacked IC and Inductor requires:
  – Inductor operation at high frequency (> 20 MHz)
  – Size & form factor compatibility between IC and inductor (< 4 mm²)
  – Low Inductor profile (< 0.3 mm)
  – Packaging scheme

• Micro-fabricated inductor can satisfy these requirements
Magnetics on Silicon: Tyndall Approach

- Single layer of racetrack shaped copper coils sandwiched between layers of magnetic material
- Copper coils deposited by electroplating
- Core consists of thin film of NiFe alloy deposited by electroplating
Overview of Fabrication Process

Layer 1: Electroplated bottom core layer

Layer 2: Insulator layer between bottom core and winding

Layer 3: Electroplated copper winding layer

Layer 4: Insulator layer between top core and winding

Layer 5: Electroplating top core layer
## Winding Technology

<table>
<thead>
<tr>
<th>Electroplated copper</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Maximum conductor thickness, $t_m$</strong></td>
</tr>
<tr>
<td><strong>Minimum spacing – linked to thickness</strong></td>
</tr>
</tbody>
</table>

![Diagram of winding technology](Image)
### Magnetic Core Material

**Electroplated Ni$_{45}$Fe$_{55}$**

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Saturation, $B_{\text{sat}}$</td>
<td>1.44 T</td>
</tr>
<tr>
<td>Coercivity, $H_c$</td>
<td>80 A/m</td>
</tr>
<tr>
<td>Resistivity, $\rho$</td>
<td>45 $\mu\Omega$ cm</td>
</tr>
<tr>
<td>Anisotropy, $H_k$</td>
<td>800 A/m</td>
</tr>
</tbody>
</table>

Anisotropy induced in material during deposition
Permeability vs. frequency

![Graph showing relative permeability vs. frequency in MHz.](image)
Design Approach

• Size and Efficiency are the key design parameters
• Define Inductor Efficiency as figure of merit

\[ \text{Efficiency} = \frac{\text{Converter Output Power}}{\text{Converter Output Power} + \text{Inductor Loss}} \]

• Optimization based on analytical model for inductor
• Model Includes:
  – Core loss: Eddy currents + Hysteresis
  – Winding loss: DC + AC (6 harmonics)
• Goal of Optimization:
  – Maximize efficiency in any given area
Efficiency-Area trade-off

- Maximum Efficiency vs. Area, $L = 120 \, \text{nH}$
- $V_{\text{in}} = 3.6 \, \text{V}, \; V_{\text{out}} = 1.2 \, \text{V}, \; I_{\text{out}} = 500 \, \text{mA}, \; I_{\text{ripple}} = 0.6 \, I_{\text{out}}, \; f = 20 \, \text{MHz}$
Micro-inductor Optimisation

Optimisation for 200 nH inductor

Area (mm$^2$)

Efficiency %

Rdc (Ohms)

- 50 um thick Copper, 25 um spacing
- 40 um thick Copper, 13 um spacing
Fabricated Devices

- Design Inductance range
  - 0.5 mm$^2$ → 10 – 40 nH
  - 1.3 mm$^2$ → 30 – 200 nH
  - 2.5 mm$^2$ → 30 – 200 nH
  - 5.5 - 10 mm$^2$ → 100 – 300nH

- Designed to maximize efficiency for:
  - Vin = 3.6 V, Vout = 1.2
  - f = 20 Mhz
Typical L and R vs. f

- Inductance and resistance vs. frequency
Inductance & DC resistance

- Measured inductance vs Rdc vs. area achieved to-date
Typical DC Bias Characterization

- Inductance at 20 MHz vs DC bias current
Efficiency in Converter

- 110 nH micro-inductor (5.5 mm²) compared to 110 nH wire-wound inductor in a 20 MHz dc-dc converter
- First generation 20 MHz converter designed by PERL group in University College Cork, Vin = 2.6 V, Vout = 1.2 V
• 160 nH micro-inductor (2.5 mm²) compared to 140 nH wire-wound inductor (Coilcraft 0402_AF141) in a 20 MHz dc-dc converter
• Second generation 20 MHz converter designed by PERL group in University College Cork, Vin = 3.0 V, Vout = 1.5 V
Comparison of losses

• Comparison of losses in micro-inductor to wire-wound inductor

• Further reduction in DC resistance of micro-inductor required
Beyond 20 MHz?

Efficiency vs. area vs. frequency for present technology

Increasing Frequency

3 turns, 1 lamination

Efficiency (%) vs. Area (mm$^2$)

- $f = 100$ MHz
- $f = 70$ MHz
- $f = 50$ MHz
- $f = 30$ MHz
- $f = 20$ MHz
- $f = 10$ MHz
Summary

• Extremely low profile inductor technology
• Allows stacking of inductor and converter IC
• Inductor efficiency of approximately 93% achieved at 20 MHz
• Higher efficiency and smaller size possible at higher frequencies
Acknowledgements
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Thank you for your attention!

Questions?