Integrated Power Delivery for High Performance Server Based Microprocessors

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Agenda

• Where Processor Loads Occur
• Multi-core Server Based Processors
  • Reasons for fine grain power management
• MCP Power Delivery Constraints
• Silicon Based Power Delivery Design
• Conclusions
MICROPROCESSOR LOADS

Where they occur on the processor
Processors General

Processors functioning...
- Fetch, Decode, Execute, Write
- Power burned in discrete units often non-sequentially
- Load concentrates in active logical units

Execution Cycle

Load currents can concentrate in regions thru-out the execution of a process
Multi-Core Processors

Loading occurs in smaller regions - current funnels-in both statically and dynamically
- Loads can occur in separate cores at different times -

Example: Power Density in Dual-Core

Current is focused into small region of load

This causes current flow into load to concentrate from source thru package

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Modeled Results – Package Static Analysis - Example

Package Planes
- Funneling can occur into load where current density is highest
MULTI-CORE SERVER BASED PROCESSORS

Justification for Fine-Grain Power Management
Server MBVR Today

• Caps distributed around socket but static current comes from inductor ‘nodes’
• Distribution typically looks good for *uniform* loads
• However, for multi-core, this results in large impedance as discussed.

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Power in Distribution – LF

Static power distribution is determined from current density distribution in path J(r,z) predominately determines impedance.

\[ \int_S (E \times H) dS = \left\{ \int_V H \cdot \frac{\partial B}{\partial t} dV + \int_V E \cdot \frac{\partial D}{\partial t} dV + \int_V E \cdot J dV \right\} \]

Determination of power loss in plane structures dominates.

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Movement in Server Microprocessors

• Industry Direction is now towards multiple cores rather than fewer cores

2 Core Example

Multiple Core Example

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Multi-Core Server Processors

- For multi-core operation, MBVR Distribution may result in higher loss and impedance due to larger parasitics, distance, and current density increase.

Z(f) Profiles

Large Load region

Small Load region
Processor Activities

• Generic Multi-threaded processors activity can overlap in time-windows for server processors – *speeds & feeds*
  • Activity Factors are key
  • Load overlap is key

• Performance and Power metrics are key
  • Process quickly // shut down fast

• Power Density has increased
  • Control power at load – not at source

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Simple Transistor Operations...

– At low-level current is drawn both ‘statically’ and dynamically

\[ I_{\text{leak}}(V,T) \approx I_{\text{leak}}(B) \cdot 10^\frac{V-V_{\text{leak(B)}}}{M} \cdot 10^\frac{T-T_{\text{leak(B)}}}{K} \]

\[ I_{\text{dyn}}(V) = I_{\text{dyn(base)}} \cdot \frac{V}{V_{\text{dyn(base)}}} \]
Potential Power Savings Estimated - Leakage

Power Savings estimated from both leakage current reduction in thermal and $V_{dd}$ as well as set-point.

- Sub-threshold currents tend to dominate in leakage equation

- Reductions may also occur due to thermals – not estimated here.

$$\Delta P = \left( P_{MBVR} - P_{PSOC} \right) / P_{MBVR}$$

$$\Delta P / P \approx \left( \frac{V_{dd} k 10^{V_{low}} - V_{dd} ' k 10^{V_{low}}}{V_{dd} k 10^{V_{low}}} \right) = \left( \frac{V_{dd} 10^{V_{low}} - V_{dd} ' 10^{V_{low}}}{V_{dd} ' 10^{V_{low}}} \right)$$

approximations

$$I_{off} \approx k 10^{V_{low}}$$
Loadline = Representation of impedance between power source and load

When close to load, power may be saved due to lowering voltage at source

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Leakage Power Revisited

Leakage (drain-source)
- Leakage current dominated by sub-threshold dimensions and DIBL.
- Threshold voltage lowering
- Dependent upon internal state $q$ and input vector $v$.
- Temperature dependence estimation
- Other leakage components exist – e.g. gate leakage – not evaluated here.

Standard NMOS sub-threshold current equation

\[
P_{\text{Leak}} = V_{DD} \cdot I_{\text{Leak}}(v, q) \quad [1]
\]

\[
I_N = \mu_N C_{ox} \frac{W}{L} V_t^2 e^{\frac{V_{GS} - V_{THN}}{nV_t}} \left(1 - e^{\frac{-V_{DS}}{V_t}}\right) \quad [2]
\]

\[
P_{\text{new}} \approx \left(\% P_{\text{leak}} \cdot P_{\text{old}}\right) 10^{\frac{\Delta T}{TH}}
\]
Multi-Core Processors

If power delivery does not change

– Power to load will increase
– Cost of power delivery solution will increase

Requirements

– Shallower Loadline
– Segment power delivery to each load
– Smaller power delivery implying Power SOC technology on or near package
MULTI-CHIP PACKAGE POWER DELIVERY CONSTRAINTS

Power delivery where the load is
MCP Power Delivery

• To combat the emerging issues of multi-core, power delivery must get closer to the load. This requires delivery on package.

• Many rails requires many VR’s
• Reliability is key metric
• Size is key metric
• Cost is key metric.

Example large die on package
Example Power SOC Device next to die

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Constraints of MCP

• Package
  • Must be compatible with manufacturing design rules (spacings, Cu layers, etc.)
  • Must be able to use current capacitor technology
  • Must be compatible with manufacturing rules for existing silicon.

• System
  • Must be compatible with VR’s on platform for higher input voltages
  • Must be cooled with existing thermal solutions and not impact thermal of microprocessor.
  • Must be cost effective over existing platform designs and reduce cost at platform.
Many Rails, Many VRs

• Architecture Requirements
  • Power SOC device must be able to have many rails to supply the many loads
  • Number of phases must be high – activity of load modulates from off to full on – efficiency must be flat thru range.
  • Response must be very fast (change in impedances requires less local cap [and different!] thus, loop response in > 5 MHz.)
SILICON BASED POWER DELIVERY DESIGN

Power SOC Design Considerations
If a Power SOC

- **Integration of Magnetics, Capacitors**
  - Low resistance vertical connections an advantage
  - Backend compatibility with Silicon CMOS process required.
  - Power Density – must meet manufacturing requirements
  - Must be compatible with Assembly manufacturing

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**Physics Requirements**

- Power SOC  Energy Storage
  - Energy Density
  - Power Loss
  - Dimensional Constraints

\[ W_M = \frac{1}{2} \iiint \vec{B} \cdot \vec{H} \, dV \approx \frac{B^2 \nu}{2 \mu_r \mu_0} \]

\[ \frac{W_M}{W_A} \approx \mu_r \]

\[ W_a \approx W_m \Rightarrow \nu_m \mu_r \approx \nu_a \]

\[ \frac{R_a}{R_m} = \frac{P_a}{P_m} \approx \frac{l_m \sqrt{\mu_r}}{l_a} \]
Performance

• Efficiency of Power SOC must be high to combat extra stage.
• Speed of Power SOC must be better than MBVR due to less energy storage near die.
• Size of Power SOC must be much smaller to allow getting closer to load.
Silicon Design Constraints

• Integration is key
  • Integrate everything!
  • Passives should be integrated – magnetics, capacitors, etc. – to ensure parasitics are reduced.
  • Layout constraints of bridges, drivers, bias circuitry is key to limit noise generation on die.
  • Cannot affect operation of the load– emissions, thermals, electrical noise to PLL’s is extremely important – thus location of these devices on Power SOC is critical.

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Silicon Design Constraints

- Bridge Design
  - Routing thru to metal stack and bumps
  - Current densities
- Driver Design
  - Proximity to segmented bridges
- Bias Control Circuitry Design
  - Noise immunity
  - Isolation
  - speed
Silicon Design Constraints

• High Volume Manufacturing Design

Things to consider...

• manage your transistor sizes for different functions

• Key analog circuits (BW range is typically 5-400 MHz) – keeping gain, low noise and HF is key here.

• PSRR’s & CMRR’s
  • Need high rejection on sensitive op-amps and references (bandgaps).
Other Considerations

• Digital Control
  • Bias power in digital control can often exceed 10x that of analog control for similar BW. Breakthru’s needed here.

• Materials
  • Compatibility with silicon manufacturing is important.

• System
  • Compatibility with existing infrastructure on platforms

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Conclusions

• Architecture and technology in microprocessors drives multiple rails
• There is justification for moving closer to load in server based microprocessor designs
• Power SOC architecture must support multiple rails, phases, and be quick
• Need to match packaging constraints of load
• Cost drives CMOS implementation
• Architecture for Power SOC Silicon design must take into account inter-system analog/digital design constraints.

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